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Simulation of Unified Power Flow Controller Closed Loop and Interline Power Flow Controller For Closed and Open Loop Using Pspice

[1]Kavitha Kumari KS [2]Pravina P [3]Reena Joshi Vince V [4]Ashly Mary Tom
[1]Department of Electrical and Electronics Engineering ,Assistant Professor, Jeppiaar Engineering College
Chennai, Tamil Nadu 600119, India
[1]kavitha_eee2005@yahoo.co.in [2]smppravi@gmail.com [3]reenajosh@gmail.com
[4]ashlymtom@gmail.com

Abstract

The Unified Power Flow Controller (UPFC) is a versatile controller which be able to be used to manage the vigorous in addition to reactive power in the line independently. The solid state controllers are used to practically handle problems involving compensation of transmission lines and power flow control problems with the concept of UPFC. To improve power quality in the distribution systems, various solutions were developed and implemented, namely active filters, unified power flow filters(UPFC) , Interline power flow controllers. An Interline Power Flow Controller is a series or series-parallel filters applied to several independent lines with a common DC element. Basically an interline power Flow Controllers a VSC-based Flexible AC grid System(FACTS) controller intended for series compensation with the distinctive capacity of power flow administration amongst multi-lines of a substation. In this project basic characteristics of IPFC are discussed. By this scheme maximum system asset is utilized. Initially modeling and simulation of SSSC (UPFC) is done, since the IPFC is series parallel combination of converter and line. Then the modeling and simulation of IPFC is done using Pspice software package. The performance characteristics of the IPFC are studied and the results are presented.

Keywords: Flexible AC grid System, Unified power flow Controller (UPFC), Interline power flow controller

Introduction

As a consequence of Flexible AC transmission initiative, significant endeavor has been exhausted in last years on the improvement of power flow Controllers based on power electronics. Synchronous voltage sources can be used with help of self commutated inverters. Without using reactors and capacitors reactive power can be internally absorb and generated by using power electronics based voltage sources. Reactive and real power can be provided with independent control as they can make possible reactive and real power compensation.

The Interline Power Flow Controller (IPFC) scheme Proposed provides, line compensation individually for each line with independent controllable reactive series compensation, Based on the above feature it is possible to balance reactive and real power between lines and it is easy to transfer the power demand to under loaded from overloaded lines, compensated beside resistive line voltage drops in addition to the corresponding reactive power requirement; raise the efficiency of on the whole compensating structure for energetic dynamic disturbances. It can provide potentially an effectual method for power transmission administration at a substation with multi-lines.

Literature Review

A. Basic Circuit of UPFC

The UPFC primarily inject a voltage, in series with the line, whose phase angle can vary between 0 to 2π with respect to the terminal voltage and whose magnitude can be varied from 0 to a defined maximum value(depending on the rating of the device). Thus the mechanism must be able of generate and absorbing both real and reactive power. This checker can be realize by using two Voltage Sources Converters (VSCs) as shown in fig.1

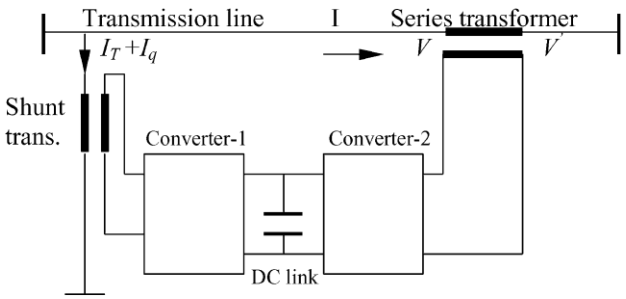

Figure 1: Basic UPFC Configuration

The two converters are operated from a common dc link provide by a dc storage capacitor. VSC_2 is used to inject the required series transformer which is transformed by the converter into DC power which appears at the capacitor link as positive or negative real power demand. This dc link power is converted back to ac and coupled to

the transmission line via a shunt transformer by VSC_1. Thus, the basic function of VSC is to produce the demanded real power by VSC_2 at the common dc link.

The internally generated reactive power by VSC_2 is exchanged at the AC terminal of the series transformer.VSC_1 can be able to produce or take in controllable reactive power .It can be represented as a two port device with a controllable voltage source V_{se} in series with the line and a Controllable shunt current source I_{sh}

B. Interline Power Flow Controller

There are a number of Direct Current to Alternating Current inverters each of them provides series reimbursement for dissimilar lines as depicted in fig.2 with the help of Interline Power Flow controller. Static Synchronous Series Compensators(SSSC) provide the series compensation mechanism.

The DC terminals are used to link the compensating DC to AC converter. There are many types of compensators which has a added functionality of providing series reactive compensation used for controlling real power exchanges in transmission line through the DC link. The underutilized line power available with be utilized by other lines.

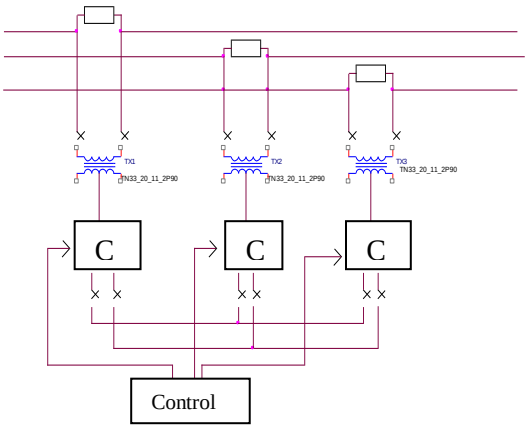

Figure 2: Block Diagram of an Interline Power Flow Controller

The above figure explains block diagram of an interline power flow controller. On the whole suitable control action is taken at the common dc terminal for accurate power balance mechanism. This is done by means of the general rule with the intention of providing the appropriate real power to under loaded lines from the overloaded lines.

In the basic IPFC schemes there are two back to back Direct Current to Alternating Current inverters, with series voltage injection each compensate a transmission line as shown in Fig.2. The two back to back Direct Current to Alternating Current inverters represent two series transmission lines 1 and 2 with two synchronous potential source with phasors V_{1pq} and V_{2pq}. The two voltage sources between real power exchange is a common link and it is represented by a bidirectional link (P_{12}).Voltage phasor V_{1r} is the receiving end bus with Transmission line 1 which is represented by reactance X_1, Voltage phasor V_{1s} is the distribution end bus. reactance X_2 representation phase of line

2 at the sending end is indicated as V_{2s} and receiving end voltage phasor is represented as V_{2r}.

Proposed Work

All the receiving end and distribution end voltages are constant with set amplitudes and they are equal to 1 per unit and they are represented as V_{1s} ,V_{1r} ,V_{2s}, V_{2r} ,with resultant in transmission angles $\partial_1=\partial_2$ and fixed angles. The rating of line impedances and two compensating voltage sources are indistinguishable, that is V_{1maxpq} = V_{2maxpq} and $X_1=X_2=0.5$p.u.

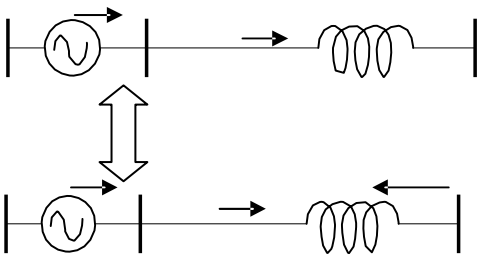

Figure 3: Basic Two Inverter IPFC

In Fig.3 System 1 is selected to be the major system for which controllability of both reactive power and real power is stipulated. The following Fig.4 explains about the inserted phasor voltage V_{1pq} and connection between V_{1s}, V_{1r},V_{x1} .The effective sending end voltage V_{1seff} is produced by adding insert voltage phasor V_{1pq} with fixed end voltage phasor V_{1s} .

$$V_{1seff}= V_{1s}+V_{1pq} \quad (1)$$

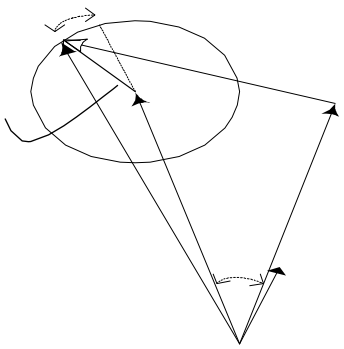

Figure 3.1: Phasor Diagram of Prime System

The compensated voltage V_{x1} is calculated as the difference of V_{1r} and V_{1seff} . the end of phasor V1pq moves along a circle with it´s centre at the end of V_{1s} as ρ_1 is varied over its full 360˚ range. The rotation angle ρ_1 of the phasor V_{1pq} modulates both the

magnitude and angle of phasor V_{x1} therefore both reactive power Q_{1r} and real power P_{1r} vary with ρ_1 in a sinusoidal manner as shown in Fig.3.1.The sinusoidal functions of angle ρ such as real power P_{1pq} and reactive power Q_{1pq} are supplied or absorbed by voltage source inverter V_{1pq}

Results and Discussion

A.Modelling of Static Synchoronous Series Compensator (SSSC)

An IPFC is nothing but a number of SSSC employed for each line with a common dc bus. This has been into consideration taken and the SSSC for the line is modeled and the circuit diagram is shown in Fig 4. The power transfer capability is being verified by varying the phase angle of source of SSSC .The voltage magnitude injected into the line is equal to the voltage difference between the sending end and receiving end voltages.

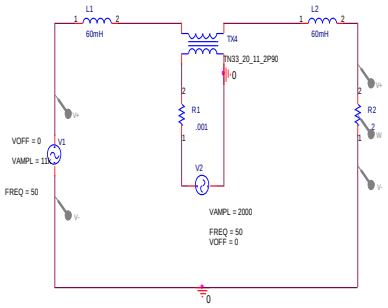

Figure 4: Voltage Source Injection at the midpoint of the Transmission Line

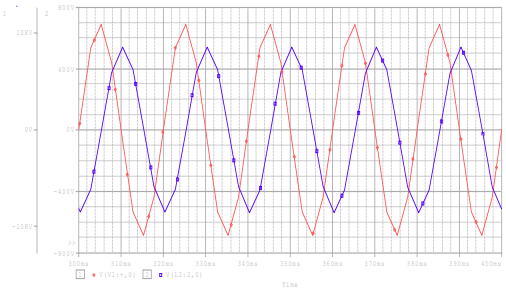

Figure 4.1: Angle of Injection: 60º

The above fig4.1 describes the angle of injection 60º. The following fig describes about Sending & Receiving end voltage with δ=90º.

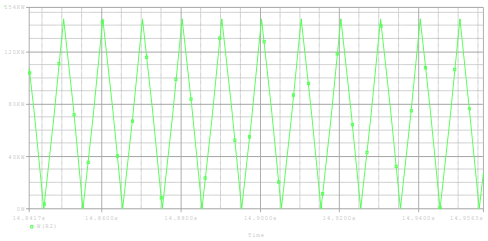

Figure 4.2: Sending & Receiving end voltage: δ=90º

Table 1: Values With Real Power

SNO	Angle of Injection in degrees	Angle δ in degree	Power in KW
1	60	90	145
2	120	99	195.26
3	210	72	177.86

The above table I gives tabulated values with real power as 145°, 195.26° and 177.86°, angle of injection in degrees and angle δ in degrees got as output.

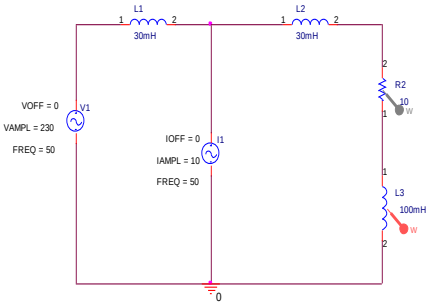

Figure 4.3: Current source at the midpoint

The following fig4.4. is the output for current source at the midpoint with source current 5A.

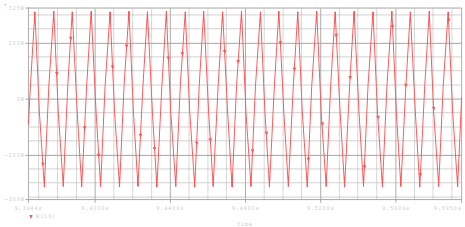

Figure 4.4: Reactive Power is 312.9W for 5 A

The following table II illustrates output for various values of source current 3,4,5,6 with real power values and Reactive power. In Table II Power and reactive power is very less for Source current as 3 and power and reactive power is very high for source current as 6A. Those values are illustrated in Table II given as follows

Table 2: Values With Source Current Outputs

Source Current(A)	Real Power(W)	Reactive Power(VAR)
6	192.53	317.55
5	189	312.9
4	185.39	304.5
3	166.5	244.4

The transformer TX1 connected in series injects the voltage into the line. The line is modeled into the two equal segments with X/2 reactance at each segment i.e., the voltage is fed at the mid-point of the transmission line. The power across the load resistor and the load inductor is measured for this combination at various phase angles of the series compensator.

Modelling of IPFC

Simulation provides the opportunity to have prior knowledge in a meaningful context. Students are actively engaged in problem solving in an environment where their actions dynamically modify progression and outcomes. Rapid investigation of the design space by simulation representation is important for eminence hardware system research and improvement. Even though remarkable commonalities across hardware systems, designers habitually fail to attain high levels of reuse across models constructed in existing and domain-specific and general-purpose language This lack of reuse unfavorably impacts hardware system design by slowing the rate at which thoughts are evaluated. These aspects has been considered and in this chapter the simulation of the circuits associated with the interline power flow control has been described.

A. Transmission Line Model

The transmission line is designed with the resistance of the line and with the reactance. The transmission line is imitation for 11KV and 10.5 KV of ac source. The circuit diagram is given in Fig 5.1. The voltage at the sending end and receiving end are observed . The power across the load resistor and load inductor are also taken for an uncompensated line.

B. Modelling Interline Power Flow Controller(IPFC)

The IPFC is modeled for a two-line system. The model is simulated and the results are taken. The converter elements are modeled as a switch. The output of each converter is fed by the corresponding line through a series insertion transformer. The input voltage

magnitude of the converter is varied. The switching of the switch is controlled by the voltage pulse source. The pulse generated is of square wave nature. The output power is measured across the load resistor and load inductor. By injecting the voltage to the line it is observed the power transfer between the two lines is maximum. The circuit diagram describing this is given in Fig.5.

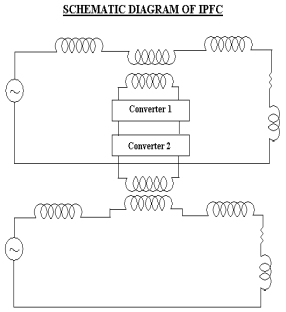

Figure 5: Schematic Diagram of IPFC

C. Basic Transmission Line Model

The basic transmission line model for 10KV is shown in Fig.5.1

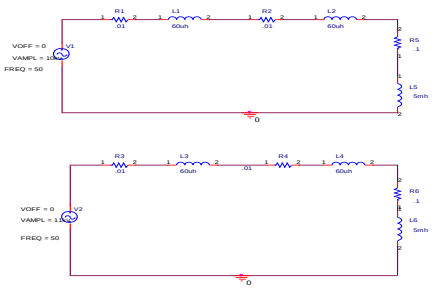

Figure 5.1: Model of Transmission Line for 10KV and 11KV

The reactive power flow in the load inductor L3, 23 Mvar is shown in Fig. This power flow is obtained without any interlink. By introducing the IPFC controller this power flow should be improved.

D. Model of Grid Line With Interlink

The model of IPFC with primary line input 11KV and the secondary line input is 10 KV is shown in Fig.5.2. The primary line input is 11KV and the secondary line input is 10KV. The interlink is employed by current dependent voltage source and voltage dependent current source. Since secondary line is of lower potential power flows from upper line to lower line. The power has been increased from 23 Mvar to 44 Mvar as shown in Fig.5.2 The gain in the prime line is 2.5 and the gain in secondary line is 0.5. The model of IPFC with primary line input is 10KV and the secondary line is 0.5 . The

model of IPFC with primary line input is 10KV and the secondary line input is 11KV is shown in the Fig.5.3. The interlink is employed by current dependent voltage source and voltage dependent current source.

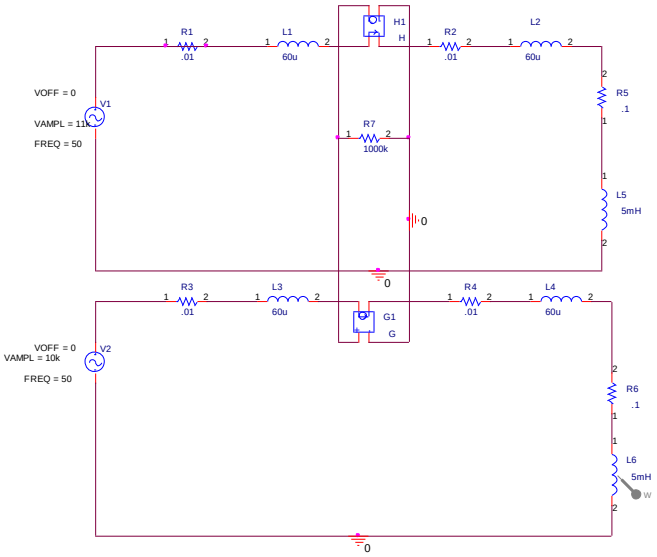

Figure 5.2: IPFC with Interlink

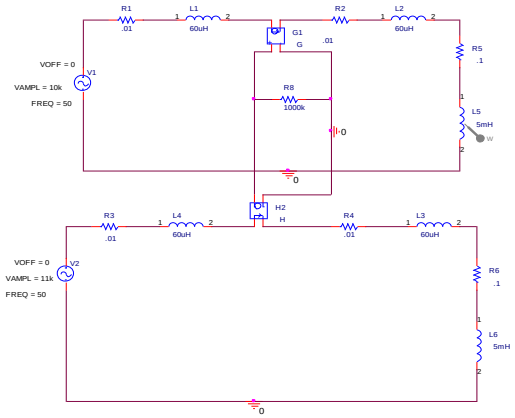

Figure 5.3: IPFC with Interlink

Since secondary line is of higher potential, power flows from upper line to lower line. The power has been increased from 23 Mvar to 44 Mvar as shown in Fig.5.3. The gain in lower line is 2.5 and the gain in the upper line is 0.5.

E. Model of Transmisssion Line With Phase Difference

In Fig 5.4 we have both the primary and secondary line input voltages are equal i.e., 10KV each. The secondary line voltage has a 30˚ phase difference with respect to primary line. The real power in the load resistor R12 of primary line is 5.8 MW as

shown in the Fig and the real power in secondary line resistor is 3.4MW as shown in Fig. 5.4. From this we infer that the real power flow depends upon the phase difference.

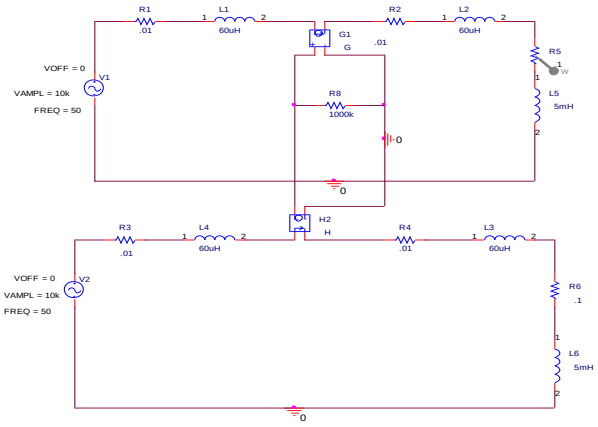

Figure 5.4: IPFC with 30º Phase of Secondary Line Sending End Voltage

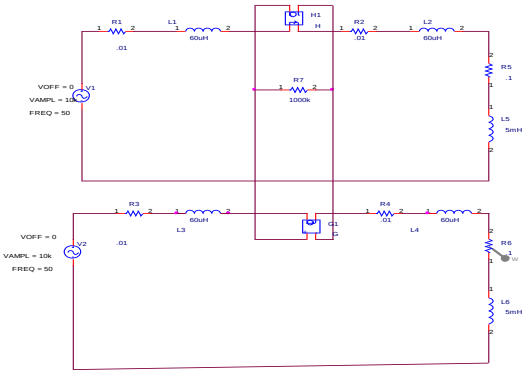

Figure 5.5: IPFC with 30° Phase in Prime Line Sending end voltage

Fig 5.5 shows the model of IPFC with equal primary and secondary line input voltages i.e 10 KV each. The primary line voltage has a 30˚ phase difference with respect to primary line. The real power in the load resistor R8 of secondary line 5.8 Mvar and the real power in primary line resistor R5 is 3.4 Mvar. From this we infer that power flows the real power flow depends upon the phase difference.

Conclusion

This paper describes the control strategy for real power and reactive power of the transmission line using Controller (UPFC-IPFC). The circuit models for UPFC and IPFC are developed and the respective results are simulated successfully using Pspice. By controlling real power and reactive power in transmission lines we can maintain the constant frequency and voltage within the limit during power transmission.By using

UPFC frequency and voltage of single transmission line is maintained within the limit and by using the IPFC voltage profile and frequency of the two line is maintained constant through out the power transmission.

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