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Design of 10 Bit R/2r Digital To Analog Converter In 180nm CMOS Technology

[1]Dr. D. Nageshwar Rao [2]K. Rama Krishna Reddy [3]N. Himashailaja [4]G.Amulya
[1]Prof. In Ece Dept., Tkrcet [2]asst.Prof. In Ece Det.,Tkrcet [3,4]m.Tech Scholars, Tkrcet

Abstract

R-2R ladder networks provide a simple means to convert digital information to an analog output. Although simple in design and function, applying an R-2R resistor network to a real application requires attention to how the device is specified. Output errors due to resistor tolerances are often overlooked in the design of the digital to analog conversion (DAC) circuit and in the selection of the R/2R ladder itself.

Resistor ladder networks provide a simple, inexpensive way to perform digital to analog conversion (DAC). The most popular networks are the binary weighted ladder and the R/2R ladder. Both devices will convert digital voltage information to analog, but the R-2R ladder has become the most popular due to the network's inherent accuracy superiority and ease of manufacture.

This paper proposes an approach for designing an R-2R 10 bit Digital to Analog Converter (DAC) which could be made to operate at low voltage supply by efficiently exploiting the two stage Operational Amplifier (Op-Amp) architecture and analyse the effect of various parameters on the characteristics of op-amp which operates at 2.5v power supply in 180nm CMOS technology. In this paper trade-off curves are computed between all characteristics such as gain, phase margin. The OPAMP is designed in 180nm technology and exhibits a gain of 53.6db with a phase margin of 179 degrees where the operating point is 1.49v.R/2R DAC operates at a 2.5V power supply and simulation results are verified using virtuoso and are presented in the paper.

Introduction

In electronics, a digital-to-analog converter is a function that converts digital data (usually binary) into analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse function. Unlike analog signals, digital can be transmitted, manipulated, and stored without degradation. But a DAC is needed to convert the digital signal to analog to drive an earphone or loudspeaker amplifier in order to produce sound. DACs and their inverse, ADCs, are part of an enabling technology that has contributed greatly to the digital revolution. There are several DAC architectures. The suitability of a DAC for a particular application is determined by six main parameters. They are physical size, power consumption, resolution, speed, accuracy, cost. Digital-to-analog conversion can degrade a signal, so a DAC should be specified that has insignificant errors in terms of the application.

DACs are commonly used in music players to convert digital data streams into analog audio signals. They are also used in televisions and mobile phones to convert digital video data into analog video signals which connect to the screen drivers to display monochrome or colour images. These two applications use DACs at opposite ends of the speed/resolution trade-off. The audio DAC is a low speed high resolution type while the video DAC is a high speed low to medium resolution type. Discrete DACs would typically be extremely high speed low resolution power hungry types, as used in military radar systems. Very high speed test equipment, especially sampling oscilloscopes, may also use discrete DACs.

Implementation

Operational Amplifier is the most common building blocks of most of the electronics system. Op-Amps are one of the basic and important circuits which have a wide application in several analog circuits such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc.

Circuit Operation:

It comprised of three subsections of circuit, namely differential gain stage, second gain stage and bias strings. It was found that this topology was able to successfully meet all of the design specifications.

Differential Gain Stage:

Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier. Transistors M1 and M2 are N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the trans conductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage.

Second Gain Stage

The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M6 and M7, this stage takes the output from the drain of M2 and amplifies it through M6. Again, similar to the differential gain stage, this stage employs an active device, M7, to serve as the load resistance for M6. The gain of this stage is the trans conductance of M6 times the effective load resistance comprised of the output resistances of M6 and M7. M7 is the driver while M5 acts as the load.

Bias String

The biasing of the operational amplifier is achieved with only four transistors. Transistors M8 form a simple current mirror bias string that supplies a voltage between the gate and source of M5. Transistors M7 and M8 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 connected to ensure they operate in the saturation region. Proper biasing of the other transistors in the circuit (M1-M6) is controlled by the node voltages present in the circuit itself. Most importantly, M6 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2. It is assumed that all transistors are in saturation for the above relationships.

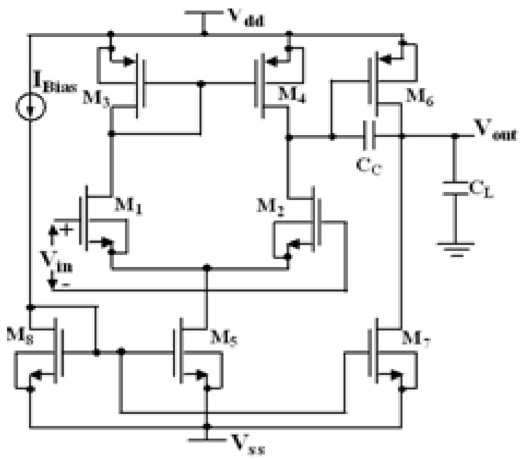

Figure 1: Design of two stage op-amp

Table 1: Design parameters

Parameter	**Value**
M1=M2	W=0.54u,L=0.18u
M3=M4	W=2.7u,L=0.18u
M5=M8	W=0.81u,L=0.18u
M6	W=16.92u,L=0.18u
M7	W=2.52u,L=0.18u
I_{BIAS}	30uA
C_c, C_L	3pF,10pF
V_{DD}	2.5v

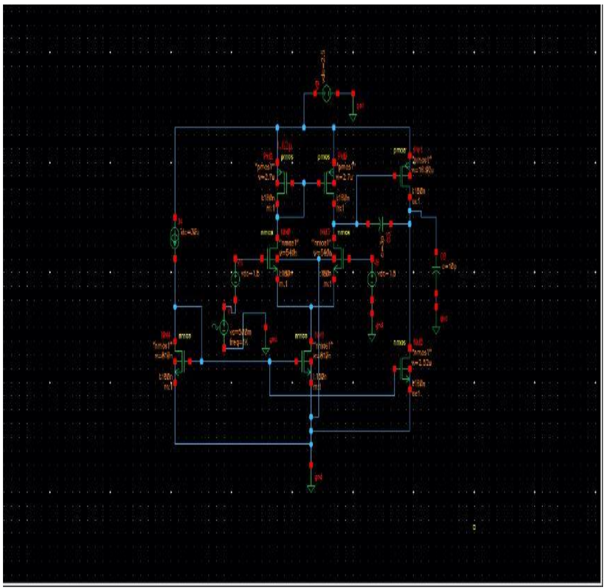

Figure 2: Two stage op-amp schematic

R/2R Digital to Analog Converter

The R/2R network is build by a set of resistors of two values, with values of one sets being twice of the other. In all of the circuits sets of 1K and 2K resistors are used, which is near to the R/2R ratio. Accuracy or precision of DAC depends on the values of resistors chosen, higher precision can be obtained with an exact match of the R/2R ratio.

The use of R-2R ladder architecture is very useful for binary-weighted currents. However, the R-2R based converter is easy to implement and the resistance ratio is independent of the number of bits the precision of the resistor is significant. One of the most common DAC building-block structures is the R-2R resistor ladder network. It uses resistors of only two different values, and their ratio is 2:1. An N-bit DAC requires 2N resistors, and they are quite easily trimmed. There are also relatively few resistors to trim.

The inputs to the ladder are fed from an N-bit input. The input voltages range from 0V to 2V. Here R- 2R network is also converted in to the CMOS equivalent circuits. This configuration consists of a network of resistors alternating in value of Rand 2R.Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R.Each node voltage is related to V_{ref}, by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from V_{ref} is constant, since the potential at the bottom of each switched resistor is always zero volts. Therefore, the node voltages will remain constant for any value of the digital input. The output voltage, V_{out} is determined.

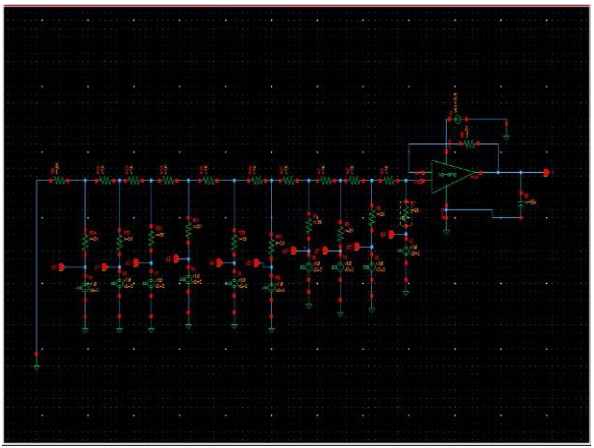

Figure 3: 10 bit R/2R DAC schematic

Simulation Results

To analyze the behaviour of R/2R, first discuss the results of basic design of two stage CMOS Op-amp. Two stage Op-amp operates at 2.5v power supply in 180nm CMOS technology. In this paper results are computed between characteristics such as gain, phase margin. The OPAMP is designed in 180nm technology and obtained a gain of 53.6db with a phase margin of 179 degrees in ac analysis with a start frequency from 100 and stop frequency of 1000 MHz where the operating point is 1.49v resulted from dc analysis.

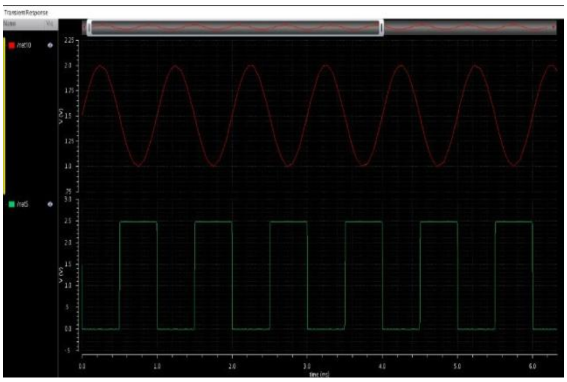

Figure 4: Transient Response

Figure 5: Two stage op-amp DC response

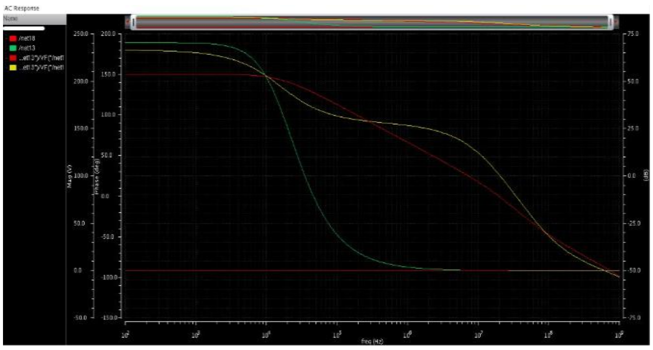

Figure 6: Two stage op-amp ac response

The simulation result for 10 bit R/2R DAC, the DAC is operated at a power supply of 2.5v.DAC is designed in 180nm CMOS technology and its transient analysis is presented.

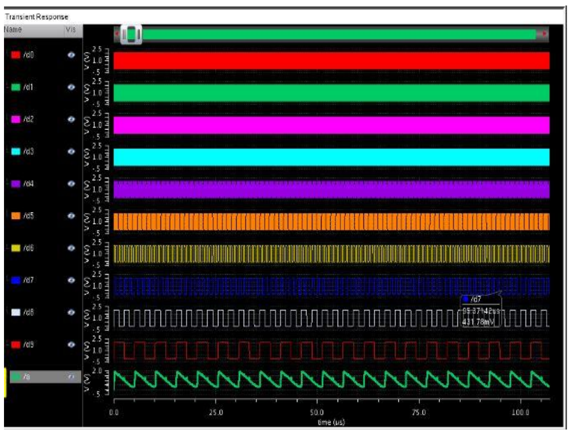

Figure 7: 10 bit R/2R transient response

Conclusion

This paper presented design of a two stage CMOS Op-Amp and analyzed its behaviour. Design technique for this Op-Amp, its calculations is given in detail. The results show that the designed amplifier has successfully satisfied all the parameters.

With an increasing trend to a system-on-chip, DAC has to be implemented in a low-voltage submicron CMOS technology in order to achieve low manufacturing cost while being able to integrate with other circuits. Experiments were performed on 10 bit R2R DAC. From this results could conclude that conversion is performed for all combination successfully and a low-power 10-bit R-2R DAC in a 180nm CMOS technology with a 2.5V supply voltage is designed.

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