International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 10 (2015) pp. 27079-27092

http://www.ripublication.com

A Statcom Based on Neutral Point Clamped Multi Level Inverter Using Multi Carrier Pwm Techniques

Arulmozhi. N[1], Gowri shankar. J [2]
[1]*M.Tech(Power Systems), SASTRA University, Thanjavur*
arulengineer.11@gmail.com
[2]*Assistant Professor, Department of EEE, SASTRA University, Thanjavur*
gowrishankar@eee.sastra.edu

Abstract

In the Recent years Power Quality issues have become important in practise as well as research. Power quality can be considered as proper characteristics of the supply voltage, reliable and effective process of delivering electrical energy to consumers. Many customers may experience severe technical and economical consequences of bad power quality disturbances such as voltage fluctuations, flicker, harmonics and unbalance leads to improper operating of appliances and some industrial process shutdown. On the other hand such phenomena appear in the power system more often because of the systematic growth in number, power of non linear and frequently time variable loads. In the condition for the technical and economical reasons ensuring good power quality is necessary. hence application of compensating equipment has increased. The evolution of power electronic devices implements the use of FACTS devices.

FACTS devices are used for upgrading Power quality and reactive power compensation of high voltage AC transmission lines. In this project, Three Level Neutral point clamped voltage source inverter based STATCOM are connected to the Power system network. Neutral point clamped (NPC) multilevel inverter(MLI) is now proven technology for high-power, medium/high voltage applications. Despite its several advantages such as harmonic reduction, reduced stress across switching devices, and achieving high-voltage and high-power capabilities without problematic series–parallel connections of switching devices, NPCMLI has an inherent problem of voltage fluctuation across dc-link capacitors due to load unbalancing, nonuniform distribution of charges, and nonidentical properties of dc-link capacitors and switching losses. Unbalanced dc-link voltage results in distortion in the inverter output and also require large size capacitance .

To maintain constant dc link voltage and achieving voltage regulation at the point of common coupling, Hysteresis controller (Non Linear Controller) is

implemented and Multi carrier PWM Technique is used for STATCOM based on NPC-VSI.
Various carrier-based PWM techniques are presented using MAT lab Simulink , which can minimize the THD and enhance the output voltages and the results are analysed.

Keywords: *Power Quality, STATCOM, Multilevel invertor , PWM technique, NPC inverter.*

Introduction

Static Synchronous compensator (STATCOM) is a shunt connected flexible AC Transmission system (FACTS) device that can regulate line voltage at the point of common coupling (PCC), balance loads, compensate load reactive power by adjusting the amplitude and phase of inverter output voltage. Different control strategies such as Linear Controller (proportional-integral controller, State feedback controller etc) and nonlinear controller(Hysteresis, Ramp, Fuzzy, Neural etc) have been proposed to control STATCOM. Recently Multi Level Inverters (MLI) have received more attention for implementation of STATCOM. STATCOM based on MLI have some advantages including higher power quality, better electromagnetic compatibility, lower switching losses, higher voltage capability and provide transformer less connection at the distribution voltage level, thereby reduction in the costs. THD minimization is an efficient method, by which the switching angles are determined so as to minimize the voltage waveform THD while the desired fundamental component is generated.

Power Quality

Power Quality (PQ) is the key to successful delivery of quality product and operation of an industry. The increased application of electronic loads and electronic controllers which are sensitive to the quality of power makes serious economic consequences and of revenues loss each year. Poor PQ can cause malfunctioning of equipment performance, harmonics, voltage imbalance, sag and flicker problems, standing waves and resonance are some of the issues that adversely affect production and its quality leading to huge loss in terms of product, energy and damage to equipment. Thus, it becomes imperative to be aware of quality of power grid and the deviation of the quality parameters from the norms / standards such as IEEE-519 standard to avoid breakdown or equipment damage.

Literature Review

Josep Pou [1] provide an idea of to include zero sequence voltage in modulation and reference signal to improve carrier based pwm technique. Diode Clamped Multi level invertors are widely spoken by Xiaoming Yuan [6] who provide solution of indirect clamping for the problem of dc link unbalancce.various Control methods of

STATCOM are widely discussed by Fangxing Li [9] who presents adaptive PI control for STATCOM. Jing Zhao, Xiangning [2] who provide a efficient novel PWM control for efficient operation. Javier Chivite-Zabalza[3] deals about FACTS application using traiangular carrier PWM modulation for the same NPC. High Power Application devices devices are dealt by N. N. V. Surendra Babu [5], he also deals with cascaded two level inverters and also multilevel techniques. Amit Kumar Gupta [8] gives a better idea on space vector modulation. PWM inverter is modelled optimally by Thomas Brückner [10]

Muliti level inverter (MLI)

Classification of Multi Level Inverter :

The multilevel voltage source inverter can be classified into three major circuit topologies.

1. Neutral Point Clamped MLI (NPC)
2. Flying Capacitor MLI (FC) .
3. Cascaded H-bridge MLI. (CHB).

Basic operating principle of Multilevel Inverters

(a) Neutral Point Clamped - MLI

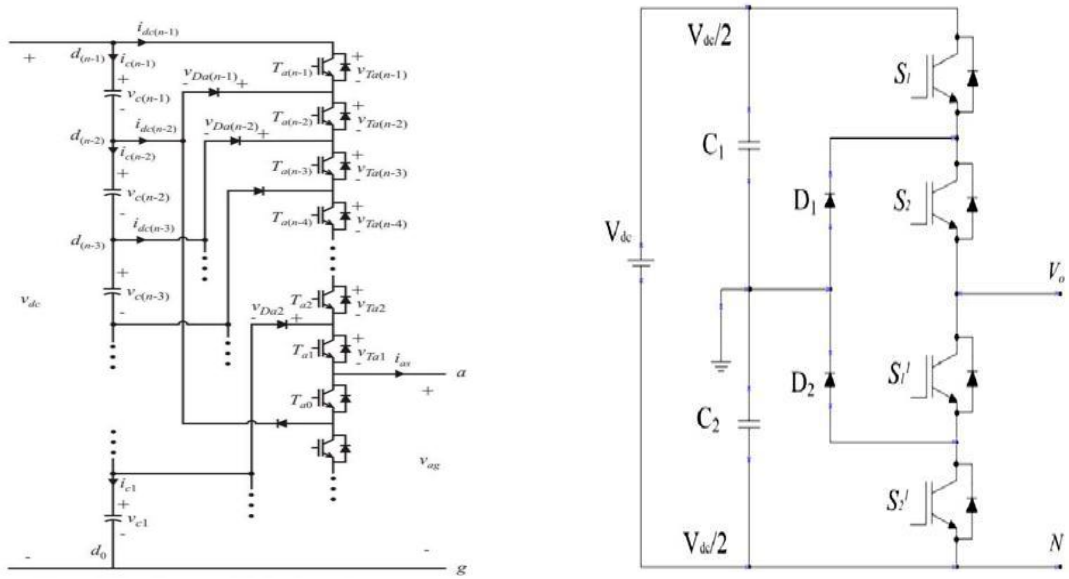

Figure 1: (a) General structure of n-level NPC inverter **(b)** 3-level NPC inverter

An m-level diode-clamp converter typically consists of (m-1) capacitors on the dc bus and produces m levels of three phase voltage. Fig.3.1.b shows a single-phase full

bridge three level diode-clamp converter in which the dc bus consists of two capacitors, C1 and C2. For a dc bus voltage *Vdc.* the voltage across each capacitor is **Vdc/2,** and each device voltage stress will be limited to one capacitor voltage level **Vdc/2,** through clamping diodes.

To explain how the staircase voltage is synthesized, Using the 3-level converter shown in Fig.1b as an example, there are three switch combinations to synthesize three level voltages across ***a a***nd ***0.***

1. For voltage level Va0 = Vdc/2 turn on all upper switches (S1 & S2)
2. For voltage level Va0 = 0, **turn** on one upper switch and one lower switch (S2 & S1')
3. For voltage level Va0 = Vdc/2, **turn** on all lower switches (S1' & S2')

Flying Capacitor Multilevel Converter

Fig. 2b illustrates the fundamental building block of a single-phase full-bridge flying-capacitor based 3-level converter**.** Each phase-leg has an identical structure. Assuming that each capacitor has the same voltage rating, the series connection of capacitors in Fig. is to

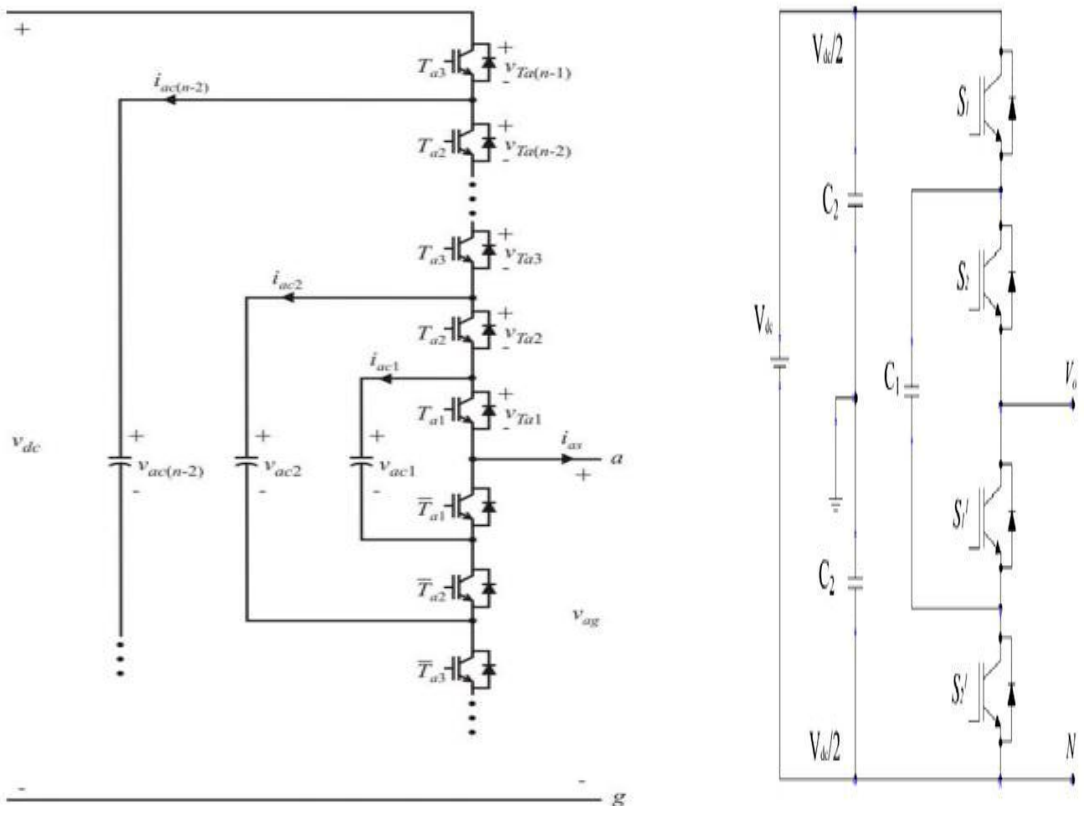

Figure 2: (a) General structure of n-level NPC inverter **(b):** 3-level FC inverter (per phase)

indicate the voltage level between the clamping points. Three inner-loop balancing capacitors for phase leg a***,*** *Ca,, Ca2,* and *Ca3* are independent from those for phase leg *b.* All phase legs share the same dc link voltage Vdc.The voltage level defined in the flying-capacitor converter is similar to that of the diode-clamp type converter. The phase voltage of an m-level converter has m levels including the reference level, and the line voltage has **(2m-1)** levels. Assuming that each capacitor has the same voltage rating as the switching device, the dc bus needs ***(m-I)*** capacitors for **an** m-level converter.The voltage synthesis in a flying-capacitor converter has more flexibility than a diode-clamp converter. But this MLI topology requires large capacitance.

Cascaded H-Bridge Multi Level Inverter

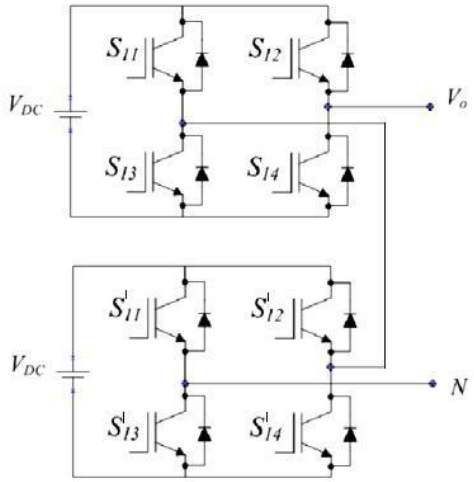

Figure 3: Structure of 5-level CHB MLI

A relatively new converter structure, cascaded-inverters with separate **dc** sources (SDCs) is introduced here. This new converter can avoid extra clamping diodes or voltage balancing capacitors. Fig.3 shows the basic structure of the 5 level cascaded-inverters with SDCs, shown in a single-phase configuration. Each SDC is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series.

The single phase 5-level Cascaded Multilevel Inverter consists of simple two H-bridge modules, whose AC terminals are connected in series to obtain the output waveforms. shows the power circuit for a five level inverter with two cascaded cells. Through different combinations of the four switches of each cell, the inverter can generate FIVE different voltage outputs, +2 Vdc, +Vdc, 0, -Vdc, -2 Vdc .

The number of voltage levels in a CHB inverter can be found from n =(2B+1) where B represents number of H-Bridge cells per phase leg. The voltage level n is always an odd number for the CHB inverter. The total number of active switches (IGBT'/GTO) used in the CHB inverters can be calculated by SW = 6(n-1) for 3 phase.

Neutral Point Clamped Multi Level

The three-level neutral-point-clamped voltage source inverter (NPC VSI) is the most popular among the multilevel converter topologies for high voltage, high power applications. the NPC VSI is supplied by pair of capacitors (C2 and C1) which are in series arrangement, where

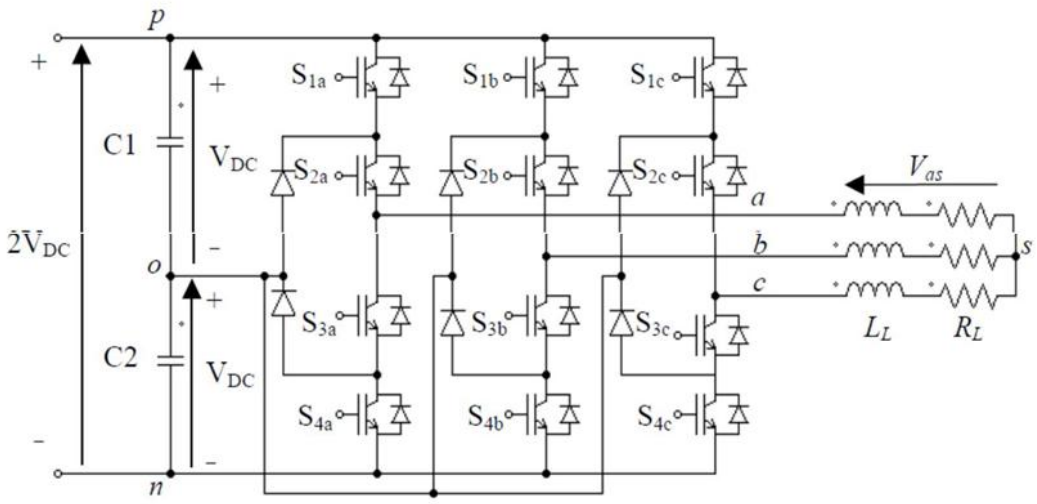

Figure 4: Three Level NPC-VSI

The three-level neutral-point-clamped voltage source inverter (NPC VSI) is the most popular among the multilevel converter topologies for high voltage, high power applications. the NPC VSI is supplied by pair of capacitors (C2 and C1) which are in series arrangement, where both capacitors are charged to an equal potential VDC, with the DC-link middle point '*o'* as a zero DC voltage neutral point(un biased point). Each phase leg of the 3 level NPC VSI consists of four switching devices which are in series arrangement and two diodes. These diodes clamp the middle switches' potential to the DC-link point '*o'* hence called clamping diodes.

The switching devices in each phase leg are controlled according to the switching combinations given below In order to generate the three-level output (Phase Voltage)

1. For Va0 = Vdc all upper switches (S1 & S2) are in on position
2. For Va0 = 0, one upper switch and one lower switch (S2 & S3) are in on position.
3. For Va0 = -Vdc, all lower switches (S1 & S2) are in on position.

Only two of the four switching devices are turned on at any time and the output terminal can be connected to any of the DC-link points , which can be represented by a switching state (P, O or N); the NPC VSI is able to generate three distinct voltage levels at the output terminal of each phase leg, *Vxo*, which can be determined using the following equation:

$Vxo = VDC(mx1 - mx3)$ ---------- (1)

The variables *mx1* and *mx3* represent the switch combinations (S1x & S2x) and (S3x & S4x) in each phase leg (x ∈{a, b, c}), which is one when both switches in the combination are 'on' and zero otherwise.

Switching Combination	Mx1	Mx2	Vox=(Mx1−x2)*Vdc
S1x & S2x	1	0	Vdc
S2x & S3x	0	0	0
S3x & S4x	0	1	-Vdc

An m-level NPC inverter consists of (m-1) capacitors on the DC bus, 2(m-1) switching devices per phase leg and 2(m-2) clamping diodes per phase. Fig 5.1 shows the structure of 3-level NPC. the DC bus voltage is split into 3 levels by using 2 DC capacitors, C1 and C2. Each capacitor has Vdc volts and voltage stress on each switching device will be limited to one capacitor level through clamping diodes. Clamping diode balances out the voltage sharing between switching devices

Multi Carrier Pwm Technique (Mc-Pwm)

The main objective of modulation technique for MLI is to get the output voltage like smooth sinusoidal waveform. Many modulation technique have been evolved for loss minimization and harmonic reduction. The wide spread method in industrial application is Sinusoidal PWM. (SPWM).

Phase Disposition (PD),

phase disposition (PD) where all carriers are in phase

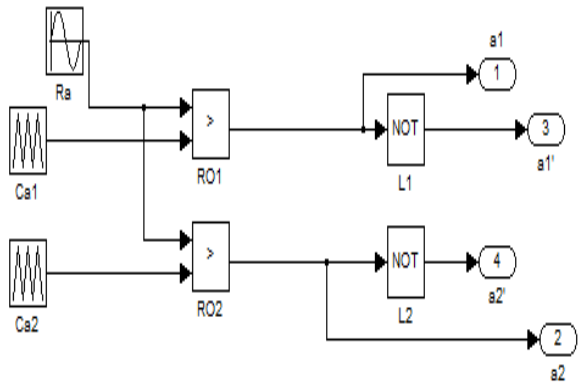

Figure 5: (a) Pulse Generation using PD-PWM Technique For Phase A Switching devices

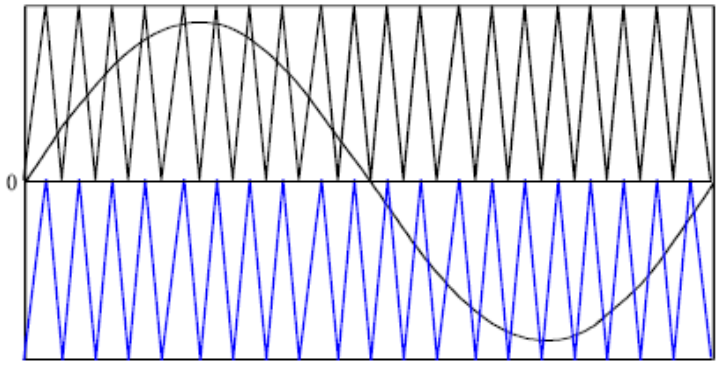

Figure 5: (b) Carrier Arrangement

Phase Opposition Disposition (POD)

In phase opposition disposition (POD) PWM, all the carriers above the reference zero point are π radian out of phase with those below the zero point

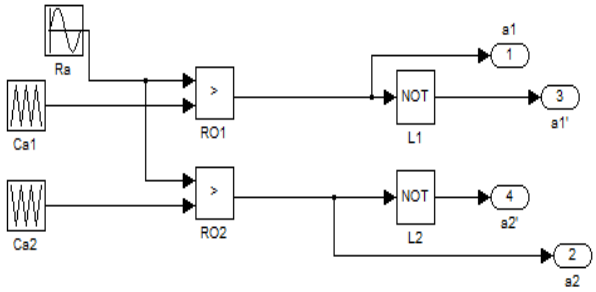

Figure 6: (a) Pulse Generation using PD-PWM Technique For Phase A Switching devices

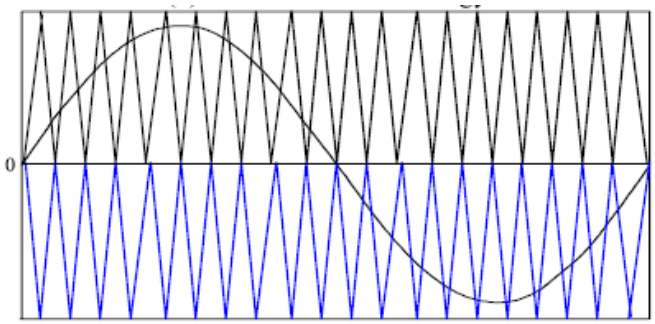

Figure 6: (b) Carrier Arrangement

Power System With NPC Statcom

Open Loop Condtion :

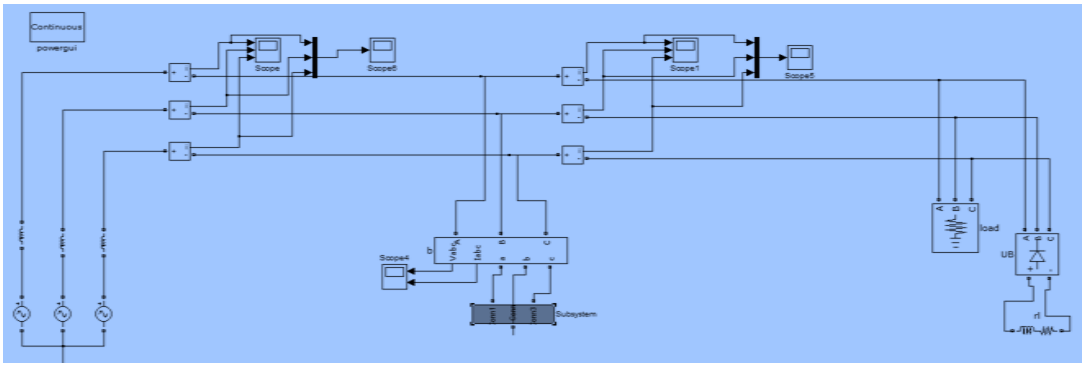

Figure 7: STATCOM Based on NPC-VSI Is Connected With The Distribution System

Closed Loop:

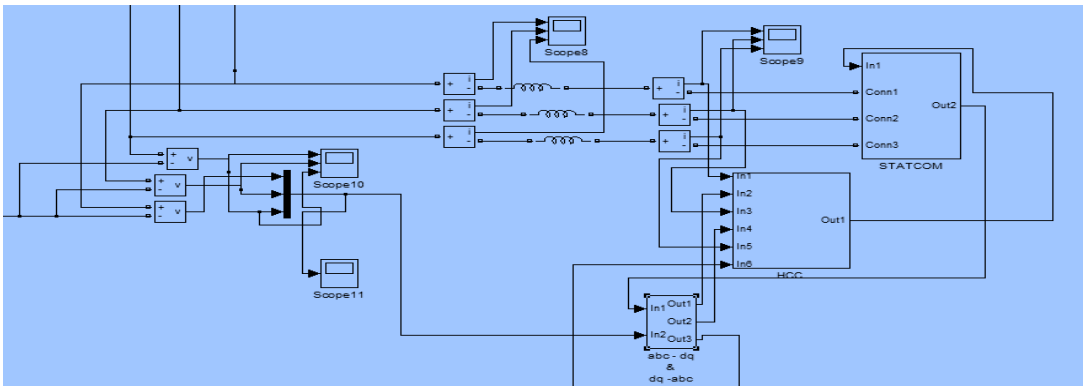

Figure 8: STATCOM based on NPC- VSI with closedloop controller is connected with power system

To maintain constant voltage across capacitor which is inside the STATCOM and connected across the VSI and to track the voltage regulation at the point of common coupling (PCC), closed loop controller circuit is designed and implemented for STATCOM. Hysteresis Current Controller (Non Linear Controller) is used to achieve the controlling objectives. In fig 8 Hysteresis current controller is implemented for STATCOM for proper operation.

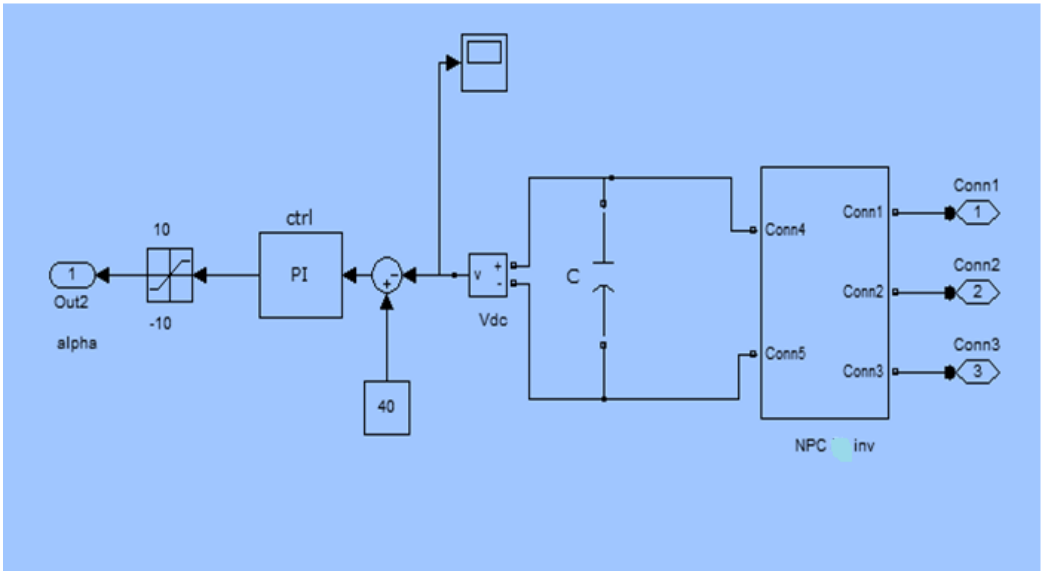

Figure 9: STATCOM

Voltage across capacitor is measured and compare with reference value and the error is given to PI controller and it gives alpha to the abc to dq & dq to abc block to generate reference current signal for HCC

Results and Interpretations

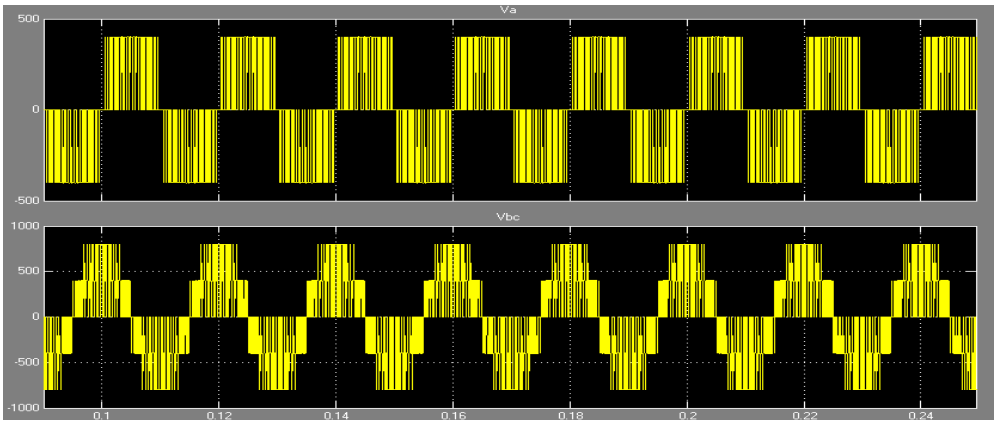

Figure 10: Phase Voltage and Line Voltage of 3 level NPC inverter

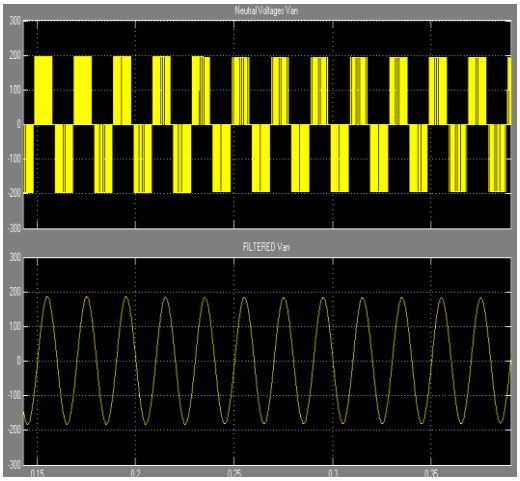

Figure 11: (a) Phase Voltage & filtered Phase Voltage

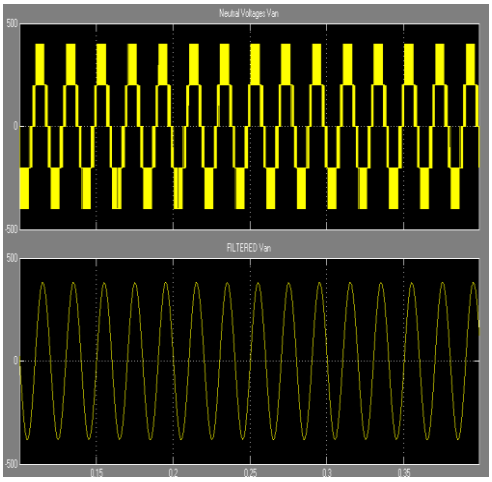

Figure 11: (b) Line Voltage and filtered Line Voltage

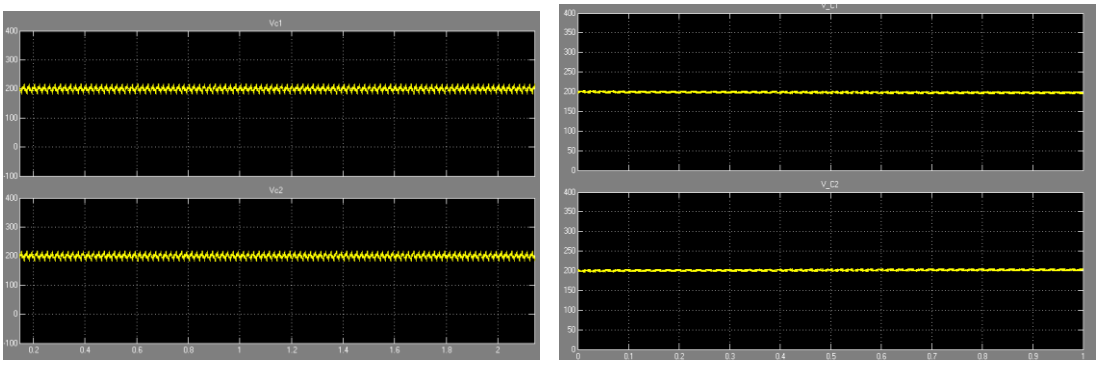

Figure 12: Voltage across Capacitor C1 & C2 (a)open loop (b) Closed loop

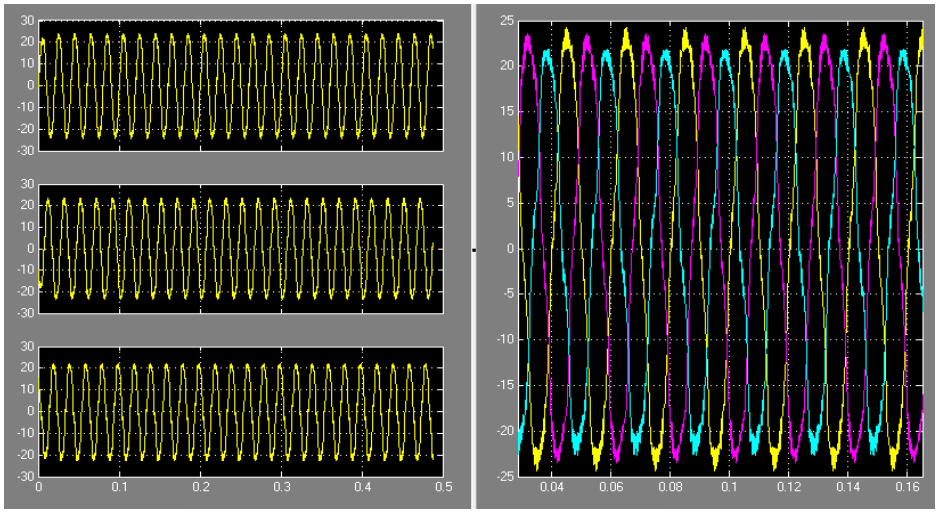

Figure 13: (a) Line Current and 3 phase load current of System in open loop

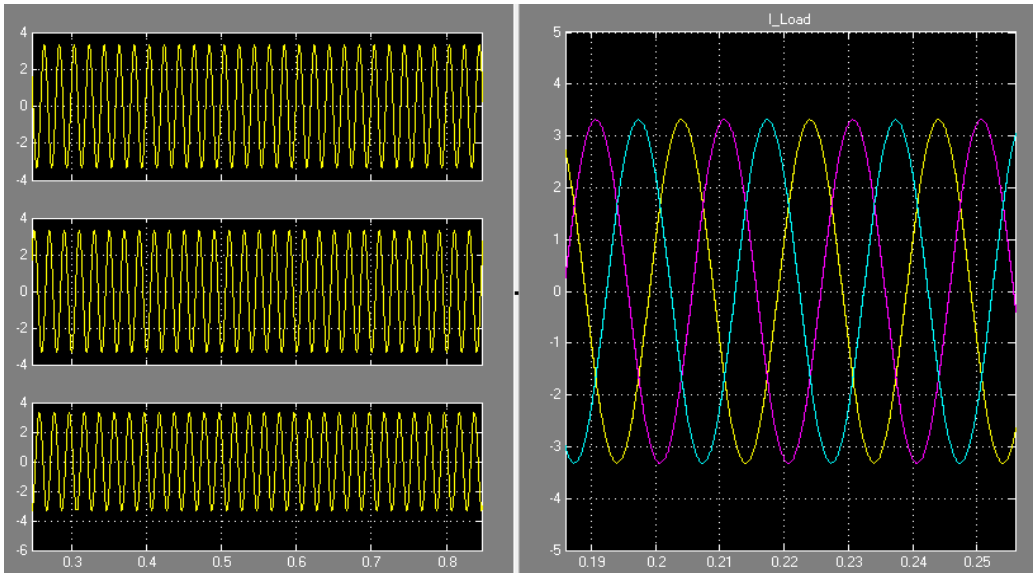

Figure 13: (b) Line Current and 3 phase load current of System in open loop

By comparing open loop and closed loop waveforms , distortion is decrased in closed loop waveform . Closed loop controller i.e.Hysteresis Current Controller and Multi Carrier PWM Technique decrease distortion in output waveform and also maintain constant DC link.

Conclusion

Deregulation of power system has made several changes in the way power system operates. As the customers have the options to choose among the various utilities, power utilities are striving to maintain their quality and reliability. Many FACTS

devices are used to improve the quality and reliability of the system. STATCOM is one of the FACTS device used predominantly to improve voltage profile of the system by injecting reactive power. In this project a Neutral Point Clamped (NPC) multilevel inverter is used and its performance in open loop and closed loop is analysed using MATLAB/SIMULINK software. A non-linear hysteresis controller is used to maintain constant voltage across DC capacitor and to regulate voltage at Point of Common Coupling (PCC). Multi Carrier Pulse Width Modulation (MCPWM) is used to generate pulses for NPC inverter. Appreciable results are obtained using the above method.

References

[1] Josep Pou, Saeedifard, "A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter", IEEE Trans. Power electron, vol. 27, no. 2, Feb 2012

[2] Jing Zhao, Xiangning He, "A Novel PWM Control Method for Hybrid-Clamped Multilevel inverters", IEEE Tran. Ind. Electron, Vol. 57, no. 7, Jly 2010.

[3] Javier Chivite-Zabalza, Pedro Izurza-Moreno, Danel Madariaga, Gorka Calvo, "Voltage Balancing control in 3-Level Neutral-Point Clamped Inverters Using Triangular Carrier PWM Modulation for FACTS Applications", IEEE Trans. Power Electron, vol. 28, no. 10, Oct 2013.

[4] Amit Jain, Ned Mohan, "Voltage Regulation With STATCOMs: Modeling, Control and Results", IEEE Trans. Power delivery, vol. 21, no. 2, April 2006.

[5] N. N. V. Surendra Babu, B. G. Fernandes, "Cascaded Two-Level Inverter-Based Multilevel STATCOM for High-Power Applications", IEEE Trans. Power delivery, vol. 29, no. 3, June 2014.

[6] Xiaoming Yuan, Ivo Barbi, "Fundamentals of a New Diode Clamping Multilevel inverter", IEEE Trans. Power Electron, vol. 15, no. 4, Jly 2000.

[7] Pradyumn Chaturvedi, Shailendra Jain, Pramod Agarwal, "Carrier-Based Neutral Point Potential Regulator With Reduced Switching Losses for Three-Level Diode-Clamped Inverter", IEEE Trans. Ind. Electron, vol. 61, no. 2, Feb 2014.

[8] Amit Kumar Gupta, Ashwin M. Khambadkone, "A Simple Space Vector PWM Scheme to Operate a Three-Level NPC Inverter at High Modulation Index Including Over modulation Region, With Neutral Point Balancing" IEEE Trans Ind. applications, vol. 43, no. 3, May 2007.

[9] Yao Xu, Fangxing Li, "Adaptive PI Control of STATCOM for Voltage Regulation" IEEE Trans. Power delivery, vol. 29, no. 3, June 2014.

[10] Thomas Brückner, Donald Grahame Holmes, "Optimal Pulse-Width Modulation for Three-Level Inverters" IEEE Trans. Power. Electron, vol. 20, no. 1, Jan 2005