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A Low Power Neural Amplifier Designing In 180nm CMOS Technology

K Pratyusha and Sanjeev Kumar
pratyu0320@gmail.com, sanjeevrawal99@gmail.com

Abstract

As analog integrated circuits are having high precision and accuracy, there is a great demand of analog VLSI in biomedical field. In this paper, two stage OTA architecture for neural amplifier is proposed, which is suitable for processing bio-potential signals with high gain, low noise and low power. In proposed neural amplifier transistors are made to operate in either weak or moderate inversion region for low power applications. Proposed neural amplifier is designed using 180 nm CMOS process with a supply voltage of 1.8 V. Simulated results shows that neural amplifier is operating with a mid band gain of 44.8 dB, input referred noise of 1.82 μV/sqrt(Hz), power consumption of 7 μW and pass the bio-potential signals in the frequency range of 6 Hz to 1.7 KHz.

Keywords: Neural amplifier, bio-potential signals, weak or moderate inversion.

Introduction

Processing of bio-potential signals is an important aspect in biopotential acquisition systems. Bio-potential signals that are acquired from the surface of body are very low in amplitude that is in the range of micro volts or millivolts and are in the low frequency range starting from millihertz to killohertz. EEG, EMG, ECG signals comes under the biopotential signals category, EEG signals captured from the surface of skull are in the range of 50μV to 500μV and EMG as well as ECG are in milivolts range. Amplification of these signals are very necessary for the proper operation and these signals are generated due to the electrochemical activities inside the body. Signals can be captured invasively or non-invasively from the body cells using electrodes and these electrodes establish a connection between brain cells and neural amplifier. Electrodes are designed using MEMS technology specifically for application in biomedical field and these are of different types depending upon the type of bio-potential signals acquired, either wet electrodes or dry electrodes. Generally dry electrodes are preferred as these are more convenient for the patient. Signals captured through the electrodes are suffered from DC offset voltage

interference, which is generated due to the electrode-tissue interface. DC offsets are in the range of milli volts and acquired input signals are in the micro volts range, so when these signals are passed through the neural amplifier for processing, DC offset signals dominates the input signals and at the output undesired result is achieved.

For accurate processing of biopotential signals dc offset voltage interference should be rejected. Biopotential signals are having different frequency range, so neural amplifier should be designed to amplify particular range of frequency depending on the applications. INA(instrumentation amplifier)[10] is mostly used in biomedical field for the measurement purpose as it is having high differential gain, low common mode gain, high CMRR(common mode rejection ratio), high input impedance, low output impedance properties. Due to the drawback of having high power consumption and large chip area, new neural amplifier designs were came into picture which eliminates these problems to some extent.

Important factor while designing neural amplifier is to reduce the low cutoff frequency, as most of the bio-potential signals are in the low frequency range. It can be achieved by using large valued resistor in the feedback circuit but large value of resistance increase the chip area. This problem is resolved by using PMOS transistors instead of resistor in the feedback circuit. Using PMOS transistors operating in weak inversion region[1], resistance in the range of tera ohm is achieved and neural amplifier operates with high time constant. Neural amplifier can be designed using different architecture of OTA, single stage op-amp, two stage op-amp, cascoded configurations, folded cascoded configurations etc. Each architecture is having certain advantages and disadvantages. Cascoded and folded cascode configuration is having advantage of high gain and disadvantage of output voltage clipping. In the cascode and folded cascade configurations, due to use of multiple stages, number of poles in the amplifier circuit increases and becomes difficult to set the dominant pole frequency.

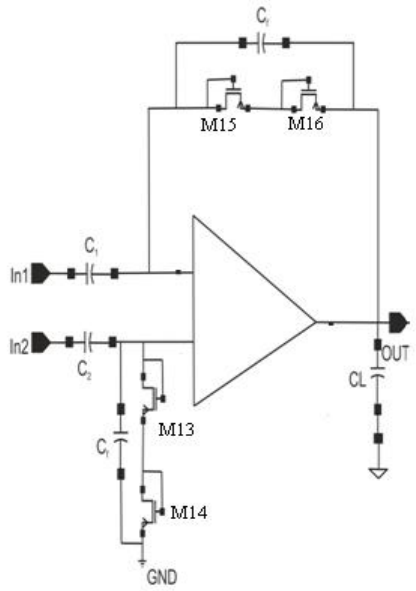

Figure 1: Neural amplifier

Using single stage op-amp in neural amplifier circuit leads to lower gain which is not sufficient for amplifying the bio-potential signals. Due to these problems a two stage OTA is used in this paper to get the desirable gain with better frequency compensation. One more critical problem in designing neural amplifier is to reduce the input referred noise and power consumption of the circuit. As the input signal is coupled with dc offsets generated due to the electrode tissue interface and common mode signals due to 60 Hz interference signals and suffers from electromagnetic and electrostatic interferences, input referred noise of OTA is designed to be small value so that it will not affect the desired input signal. In multiple electrode configuration large number of neural amplifiers are required to amplify the signals. Due to that reason neural amplifiers should have low power consumption, such that it can be used in wearable and implantable applications.

Neural amplifiers can be designed as single ended or fully differential depending upon the applications. Fully differential amplifier is having the advantage of high common mode rejection ratio in comparison with single ended but fully differential amplifier[2] requires an additional common mode feedback circuit at the output which results in increase in complexity of the circuit.

High valued resistors in the feedback circuit are required to get the low frequency of operation and feedback circuitry consisting of resistors and capacitors can be replaced by a simple integrator using active low frequency suppression technique[3]. Integrators and RC networks used in the feedback of amplifiers are used for selection of particular frequency range. Bio-amplifier proposed in [4] uses an additional band pass filter following the gain stage for achieving proper pass band.

As bio-potential signals are having different frequency ranges depending upon the type of bio-potentials acquired from the surface of body, bio-amplifier proposed in [5] consisting of adjustable band pass filter which amplifies the different frequency range signals depending upon the application. During the designing of neural amplifier power consumption and input referred noise of the circuit plays critical role and both are inversely proportional to each other. Neural amplifier with good noise efficiency factors are designed[6] to overcome this problem. Instead of using MOS pseudo bipolar resistor, NMOS transistor operated in deep depletion region provides better incremental resistance[7]. CMRR of neural amplifiers plays an important role in rejecting the common mode signals, capacitive neutralization technique[8] is used for enhancing CMRR value.

Proposed Design

For low power and low noise applications dimensions of transistors plays an important role. Input differential pairs of the OTA contribute large amount of noise in the circuit. Aspect ratios of input differential pair are made larger to minimize the input referred noise of OTA.

In Fig.1 the mid band gain of amplifier depends upon the input capacitors C_1, C_2 and feedback capacitor C_f. Relation between input capacitance, feedback capacitance and mid band gain is given by the equation(1). Frequency compensation of the OTA can be achieved by using proper values load capacitor C_L. Feedback capacitor along

with the MOS bipolar pseudo resistors used to set the low cutoff frequency. Fig.2 shows the proposed architecture of OTA.

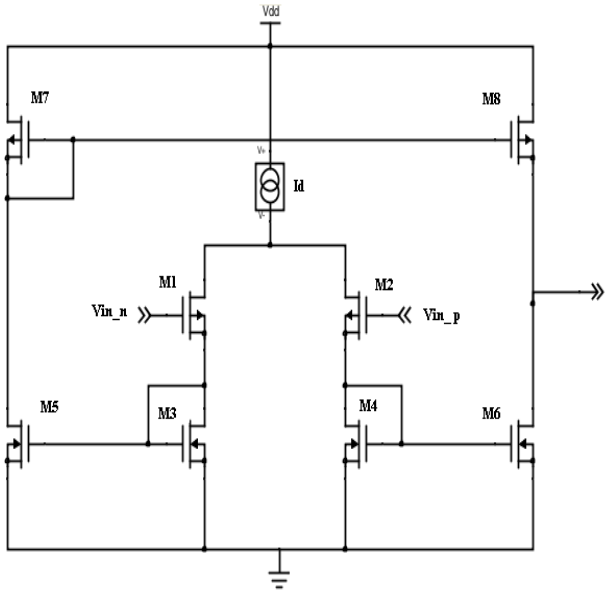

Figure 2: Proposed OTA schematic

$$A_V = \frac{C_1}{C_f} \tag{1}$$

A_V = midband gain.

From noise analysis following equation represents the input thermal noise.

$$I_n^2 = 4kT\gamma g_m$$

$$V_n^2 = I_n^2 r_o^2$$

$$V_{ni,thermal} = \frac{4kT\gamma}{g_{m1}}\left[1 + \frac{2g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right] \tag{2}$$

$V_{ni,thermal}$ = Input thermal noise of neural amplifier

T= Operating temperature

k= Boltzmann constant

γ= Coefficient which value is 2/3 for long channel devices and larger value for submicron devices.

In a MOSFET between the oxide layer and the silicon substrate a special phenomena arises where some dangling bonds are formed on the silicon substrate, which results in extra energy states. So when charge carriers cross these bonds some of the charge carries are trapped and released later. This results in the flicker noise in the overall circuit. Generalized formula for the flicker noise is given by

$$V_n^2 = \frac{k}{C_{ox}W.L} \cdot \frac{1}{f} \tag{3}$$

From the equation(3) it is clear that flicker noise is independent of the temperature and the biasing current. Flicker noise is also called as the 1/f noise and it generally occurs at the lower frequencies. It is inversely proportional to the (WL), so when we are designing a circuit for low noise applications aspect ratios of transistors generally made larger. Flicker noise content in PMOS devices is less in comparison with the NMOS devices. For bio-amplifier designing PMOS differential input pairs are used with high aspect ratios to decrease the flicker noise.

Input noise= input thermal noise + flicker noise (4)

From the equation (2) it shows, trans-conductance of input differential pair plays critical role in reducing the input thermal noise. Input thermal noise is inversely proportional to the g_{m1} and directly proportional to g_{m3}, g_{m7}. Higher trans-conductance value is achieved by increasing the aspect ratios of input differential pair.

$(W/L)_1$= aspect ratios of M_1 and M_2

$(W/L)_3$= aspect ratios of M_3, M_4, M_5, M_6

$(W/L)_7$=aspect ratios of M_7, M_8

Equation(2) shows that for reducing the input thermal noise trans-conductance of input differential should be very large in comparison with remaining transistors in the circuit. As dimensions of input differential pair are increased power consumption of the circuit increases, so a tradeoff arises between the input noise and power consumption of circuit. NEF(noise efficiency factor) determines the tradeoff between the input referred noise and power consumption of the circuit. Equation(5) represents the NEF.

$$NEF = V_{ni,thermal}\sqrt{\frac{2I_{total}}{\pi.U_T.4kT.BW}} \tag{5}$$

$$U_T = \frac{kT}{q} \tag{6}$$

U_T =thermal voltage

k = coupling coefficient(0.7)

Ideally a circuit should have a NEF of value one, but practically it is not possible and NEF values nearer to ideal value are accepted for the circuits. Table I shows the aspect ratios of transistors.

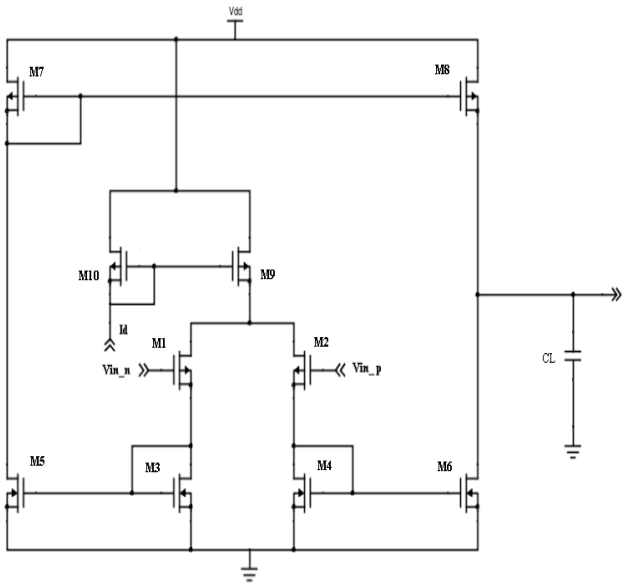

Figure 3: OTA architecture used in neural amplifier using simple current mirror configuration

$$f_c = \frac{1}{2\pi RC} \tag{7}$$

Equation(7) represents the dependency of cutoff frequency upon the RC time constant. When negative Vgs is applied to these devices they act as the diode connected PMOS transistors. Performance of pseudo resistors can be enhanced by using fixed dc voltage diode connected PMOS transistor and current source amplifier for setting the required dc voltages. Simple MOS-bipolar pseudo resistors are used to avoid the complexity, while using these devices high resistance in the range of tera ohms is attained.

Table 1: Aspect ratios of transistors used in neural amplifier

Devices	Dimensions(μm)
M_1- M_2	200/1
M_3, M_4, M_5, M_6	6/20
M_1, M_8	3.2/6.4
M_{13}, M_{14}, M_{15}, M_{16}	1/0.18

Neural Amplifier Design With Different Current Mirror Configurations

Biasing of OTA in neural amplifier plays a very crucial role in power consumption of the circuit. Dependency of

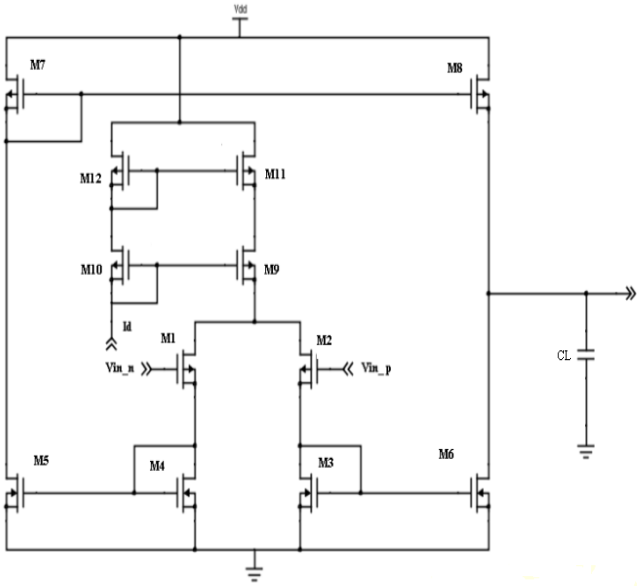

Figure 4: OTA architecture used in neural amplifier using cascode current mirror configuration power consumption on different biasing circuitry is discussed in this section.

A. Neural amplifier using simple current mirror

Simple current mirror provides low output impedance. Designed circuit results in a mid band gain of 44.8 dB which amplifies signals in the frequency range of 30.6 Hz to 7 KHz. The circuit consumes 42 uW of power with an input referred noise of 1.37 uV/sqrt(Hz). The schematic of the bio-amplifier using simple current mirror is shown in the Fig.3.

B. Neural amplifier using cascode current mirror

Transistors aspect ratios of cascode current mirror used in neural amplifier are as follows $(W/L)_{10}$, $(W/L)_9$, $(W/L)_{11}$,$(W/L)_{12}$=10/6. Schematic of OTA using cascode current mirror is shown in Fig.4.

C. Neural amplifier using Wilson current mirror

Fig.5 shows the OTA design with Wilson current mirror for biasing. Neural amplifier using Wilson current mirror for biasing provides a mid band gain of 44.8 dB, input referred noise of 1.82 uV/sqrt(Hz), low pass frequency of 6 Hz and high pass frequency of 1.7 KHz and ultra low power consumption of 7 uW. Transistors aspect ratios of Wilson current mirror used in neural amplifier are as follows $(W/L)_{10}$, $(W/L)_{12}$=10/10 and $(W/L)_9$, $(W/L)_{11}$=20/2.

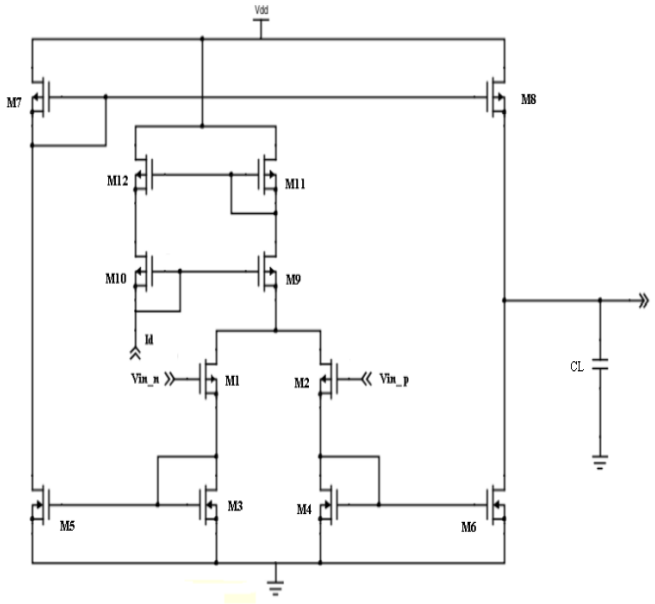

Figure 5: OTA architecture used in neural amplifier using Wilson current mirror configuration

Experimental Results

Neural amplifier using SCM configuration provides mid band gain of 44.8 dB and input referred noise of 1.37 uV/sqrt(Hz) as shown in Fig.6 and Fig.7 respectively.Fig.7 shows the gain plot of neural amplifier using cascode current mirror. A mid band gain of 44.98 dB is achieved, amplifying signals in the frequency range of 31.7 Hz to 3.8 KHz. This circuit is operating by consuming 22 uW of power, with an input referred noise of 1.36 uV/sqrt(Hz) as shown in Fig8. Circuit is having a bandwidth of 3.47 KHz.Fig.6 shows the simulated results of bio-amplifier using Wilson current mirror, providing a mid band gain of 44.8 dB, amplifying signals in the frequency range of 6 Hz to 1.72 KHz. The amplifier with feedback is consuming a power of 7 uW. Proposed one is having input referred noise of 1.8 uV/Sqrt(Hz) as shown in Fig.9 and bandwidth of 2.9 KHz.

From the above discussion a comparison is made among all these configurations. Neural amplifier using SCM configuration consuming more power and having higher low cutoff frequency in comparison with the WCM configuration. Though in the WCM configuration bandwidth is decreased in comparison with SCM configuration, WCM configuration is having a better low cutoff frequency of 6 Hz. When SCM is replaced with CCM in bio-amplifier, gain becomes high and having a larger bandwidth as compared to the WCM

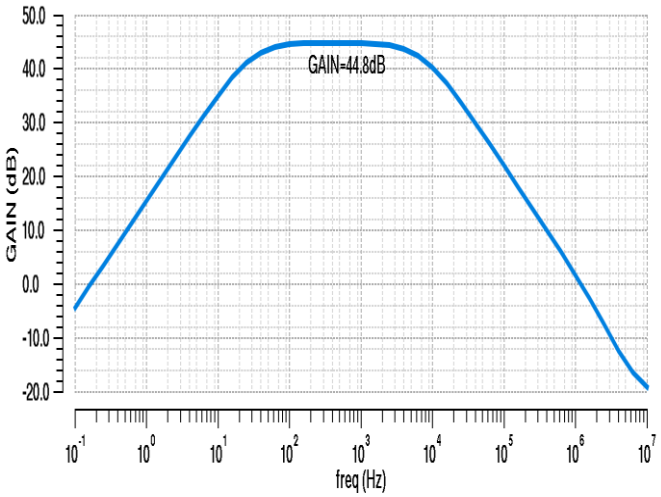

Figure 6: Gain plot of neural amplifier using SCM configuration

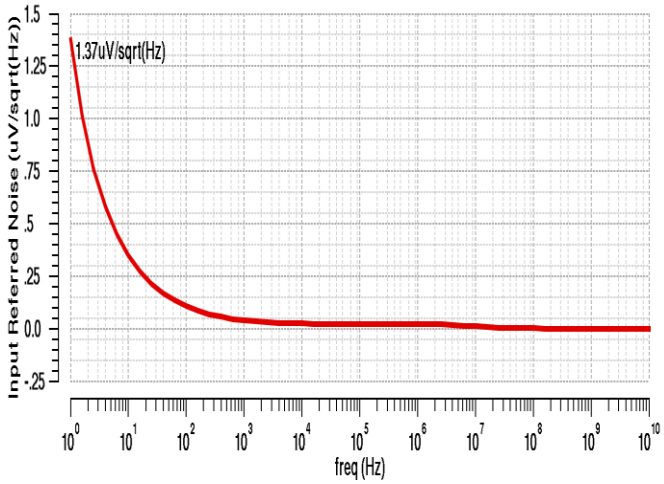

Figure 7: Input referred noise plot of neural amplifier using WCM configuration

configuration, but it is having a shortcoming of very high power consumption and higher low cutoff frequency. Instead of CCM when WCM is used approximately same gain is achieved, but there is a large difference in power consumption which is very less in comparison with cascode and simple current mirror circuit and WCM configuration is having better lower cutoff frequency in comparison with SCM and CCM configurations. When these three current mirror configurations are used for biasing neural amplifier no significant difference arises in input referred noise value of the circuits.

In proposed circuit WCM configuration is preferred as this configuration providing better results in comparison with SCM and CCM. Table II show the comparison of proposed circuit with previous studies.

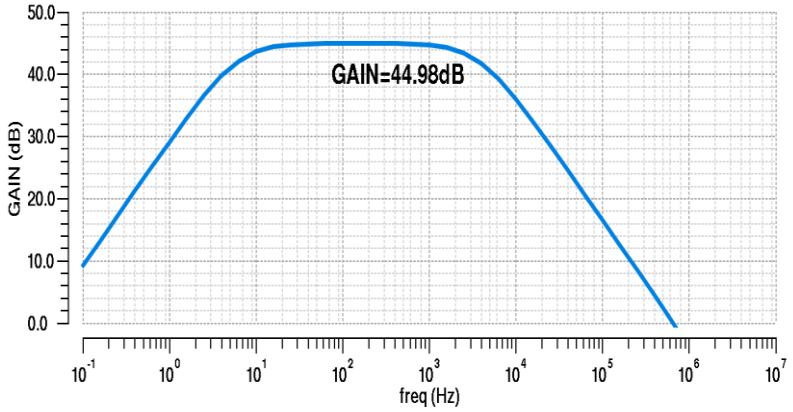

Figure 8: Gain plot of neural amplifier using CCM configuration

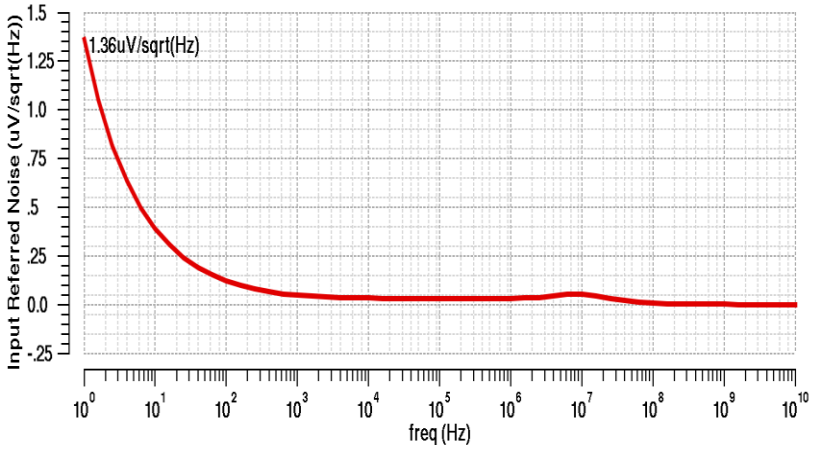

Figure 9: Input referred noise plot of neural amplifier using WCM configuration

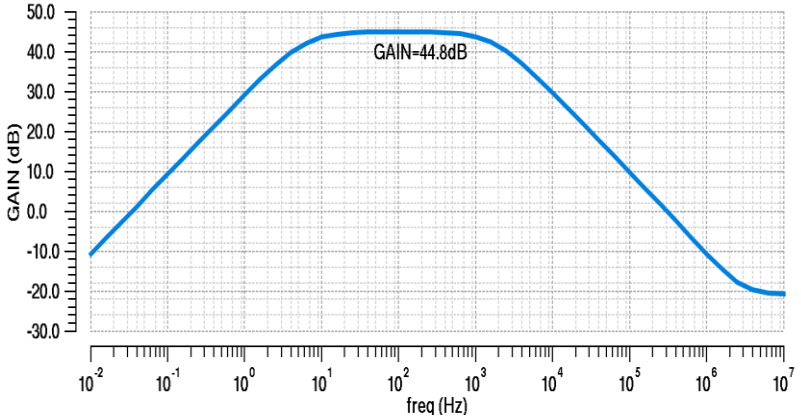

Figure 10: Gain plot of neural amplifier using WCM configuration

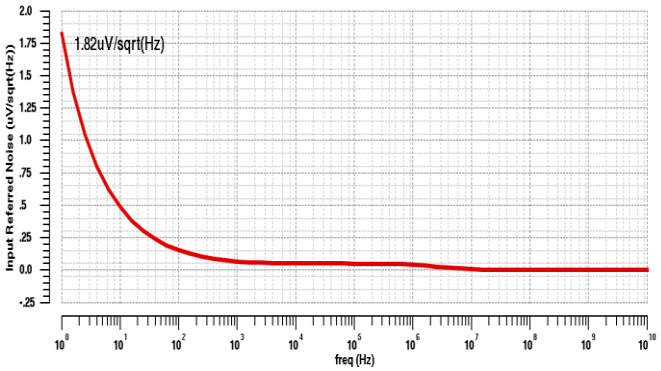

Figure 11: Input referred noise plot of neural amplifier using WCM configuration

Conclusion

A neural amplifier with high gain, low input referred noise and low power consumption is proposed in this paper to overcome the challenges in the neural amplifier designing for bio-potential acquisition systems. Bio-amplifier is biased with different current mirror configurations and a comparison is shown that how a current mirror plays an important role in designing of bio-amplifier. As bio-potential signals are in range of micro volts and miili volts, many remarkable circuits were developed till date for the amplification purpose. Low power circuits are generally preferred for the safety of patients. Most of the proposed circuits were consuming high power, so to overcome that bio-amplifier is designed in 180 nm CMOS process with a supply voltage of 1.8 V, in which transistors are operating in weak or strong inversion region consuming power of 7 uW and amplifying signals in the frequency range of 6 Hz to 1.72 KHz with a mid band gain of 44.8 dB. Results of the paper shows that proposed architecture with Wilson current mirror gives better performance in comparison with simple current mirror and cascode current mirror circuits.

Table 2: Comparison with previous neural amplifiers designs

References	Gain(dB)	B.W(KHz)	Frequency range	Power (uW)	Noise (uV/sqrt(Hz)
2003[1]	39.5	7.19	0.02Hz-7KHz	80	2.2
2007[4]	40.8	5.27	45Hz-5.32KHz	7.56	1.66
2010[5]	70	10	0-10KHz	31	88
2012[9]	44.5	0.3	……	13	4.4
Proposed work	44.8	1.7	6Hz-1.72KHz	7	1.82

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