International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 10 (2015) pp. 25317-25328

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A PFC Control Strategy For Single Phase Bridgeless Diode Rectifier Based on SEPIC Converter Topology

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Abstract

In this paper, a single phase bridgeless ac -dc converter with power factor correction control technique has been implemented, which is based on the SEPIC [Single - Ended Primary Inductance Converter] converter topology. In this proposed topology, there is no front end diode bridge and also during each switching cycle only one diode present in the flow of current path. The proposed converter topology gives less conduction loss and better thermal efficiency compared to other power factor correction circuits. The main advantages of the proposed control topology are simple control circuitry, low voltage stress on the switch and low EMI noise. The performance of this proposed control technique is validated through experimental and simulation results.

Key words: Power Factor Correction [PFC], single ended primary inductance converter [SEPIC], Bridgeless ac-dc converter, EMI, conduction losses.

Introduction

Now a days, the number of electronic components are increased, so that the demand is increased for improving the power quality of an ac system. Power factor correction (PFC) converters became an active topic of research in power electronics and efforts have been made on the development of different Power Factor Correction circuits[8]. To achieve a perceivable improvement in power quality, PFC circuits are becoming compulsory on single phase power supplies[1].

There are broadly two types of PFC converters, one is active and passive[3]. The most favorable type of power factor correction is active PFC, this formulates the load act like a clean resistor and leading to close to unity load power factor, produce less harmonics in the input current. Now a days , the majority of the active power factor correction circuits in the market place consist of front end diode bridge. It will be followed by DC - DC converter with high frequency ,for example fly back, cuk,

boost, buck boost and SEPIC etc. This process is appropriate for low , medium power level. When the power level increases, the voltage drop of the diode bridge rectifier is very high. This will causes the high conduction losses. Due to this, the whole system efficiency will degraded, the heat is produced in the diode bridge rectifier may destroy the diodes[2]. As a result, necessary to use a high current handling ability diode bridge rectifiers[9]. Due to this, the volume and price of the power supply increases, This is not acceptable for an efficient design[7]. In this active power factor correction circuits, there is also one more cause for the high conduction losses that is during every switching cycle, there are always 3 semiconductor devices in the flow of current path.

In order to increase the efficiency of the power supply, large number of bridgeless power factor correction circuit topologies have been proposed. So far the bridgeless topologies implemented with boost-type circuit configuration. Because of its low price and high efficiency, power factor, and simplicity. In[10],in every switching cycle, simply 2 power semiconductor devices are in the flow of current path, instead of 3 semiconductor devices. So, the overall conduction losses are reduced compare to normal boost type power factor correction boost type rectifier. But it is having the drawbacks which are similar to that of normal boost converter[4]. Those are, 1.The output voltage is all the time greater than that of source voltage. 2. The isolation is difficult to implement between input and output.3. High startup inrush current in overload state[6]. In addition, there are several benefits when the boost converter operating in DCM mode for example power factor correction function, easy control ,reversed recovery losses of the diode will be reduced. But, this operation needs a high class inductor because the inductor control the high ripple voltages and currents. Therefore, an input filter have to be used to suppress the pulsating current[5]. As a result, the total heaviness and price of the converter increases.

To overcome these problems, in this paper, we have been proposed a bridgeless power factor correction circuit converter. This proposed converter is based on the[single ended primary inductances converter]SEPIC topology. Not like a boost type converters, the cuk, SEPIC converters recommend a number of advantages in power factor correction circuits applications, those are limitation of current during overload condition and simple implementation of isolation, low EMI noise and less input current distortion.

Description of The Proposed PFC Converter Topology

The proposed bridgeless single - ended primary inductance converter is as shown in Fig1(a).

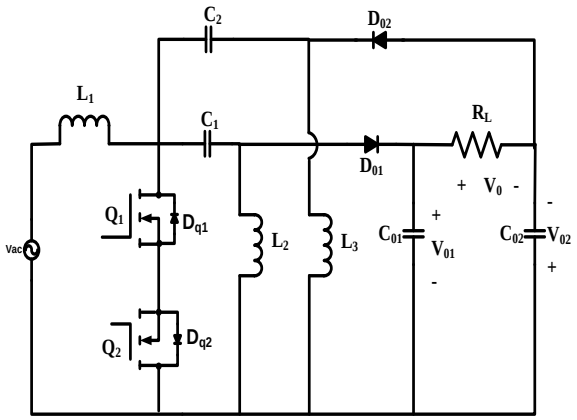

Figure1(a): Proposed Bridgeless SEPIC Rectifier

This proposed bridgeless SEPIC circuit is created by linking the two SEPIC's, one is with positive half line cycle source , another one is with negative half line cycle source.

This proposed bridgeless converter uses two fast diodes and a bidirectional switch. The semiconductor switches, namely, switchQ1, switch Q2 can be driven by the same control signal. Effective circuit in a positive half line source is shown in the fig1(b). The circuit for inverted or negative half line source is shown in the fig1(c). Here is either one or two semiconductor devices in the flowing current path, during each switching cycle. So, the conduction losses and the thermal stresses on the semiconductor devices are reduced and by compared with the bridgeless boost rectifier, the circuit efficiency is improved. The proposed rectifier uses three inductors, which are frequently illustrated as a disadvantage. But, by coupling the inductors (what we used in the circuit) on a single magnetic core leads to reduction of quantity and price and additionally we achieve the low ripple current at the input side.

The proposed converter operation will be explained below. Before we go to the explanation, assume all the inductors what we used in the circuit are functioning in the DCM mode. As well as, when we operated this SEPIC converter in this mode, this mode offers many benefits compare to CCM. For example, we can get the near unity power factor. In DCM, both the switches Q_1 ,Q_2 are turned on at zero current, while the output diodes D_{01} and D_{02} are turned off at zero current. So the switching losses and the diode reverse recovery losses of the rectifier are considerably reduced. The circuit operation in DCM, during one switching period Ts, in a positive half line cycle {fig.1(b)} will be discussed below. It can be separated into three stages.

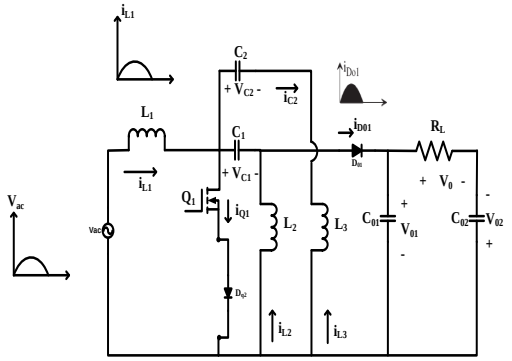

Figure 1(b): Circuit diagram for positive input source

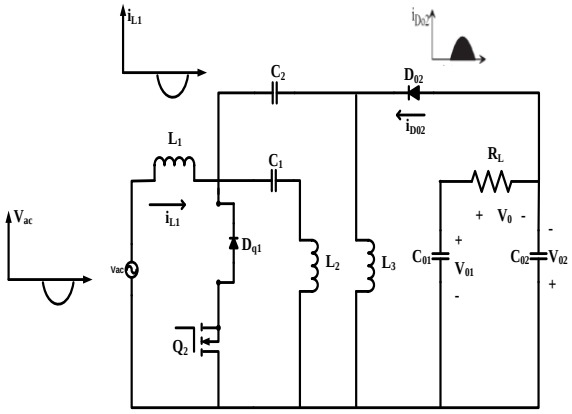

Figure 1(c): Circuit diagram for negative input source

Mode 1 {Fig.2(a):
In this mode ,the switch Q_1 is turned ON. When the first switch Q_1 is ON, the second switch Q_2 is conducting via anti parallel diode D_{q2}.Thus, the second switch Q_2 turning ON or turning OFF which will not effect on the operation of the circuit. Therefore, the two switches Q_1 and Q_2 are driven by single control signal. Due to this the circuit price and complexity will be reduced. In this Mode, all the inductor currents i_{L1}, i_{L2}, i_{L3} will increase linearly.

Mode 2 {Fig.2(b)}:
In this Mode, the output diode D_{01} is turned ON. The switch Q_1 is turned OFF. At the same time there is a path for the all the three inductors currents $i_{L1}i_{L2}i_{L3}$, which is shown in the fig.2(b).In this mode of operation all the three inductor currents will linearly decreases.

Mode 3 {Fig.2(c)}:
In this Mode, the entire switches and diodes are in open that means they are in the OFF state. Which is shown in the fig.2(c). Total three inductors, namely, L_1 , L_2 , L_3

are acts like current sources and the voltage is zero across all the three inductors. The capacitor C_1 is charged by the inductor current i_{L2}.The capacitor C_2 is charged by inductor current $i_{L3.}$

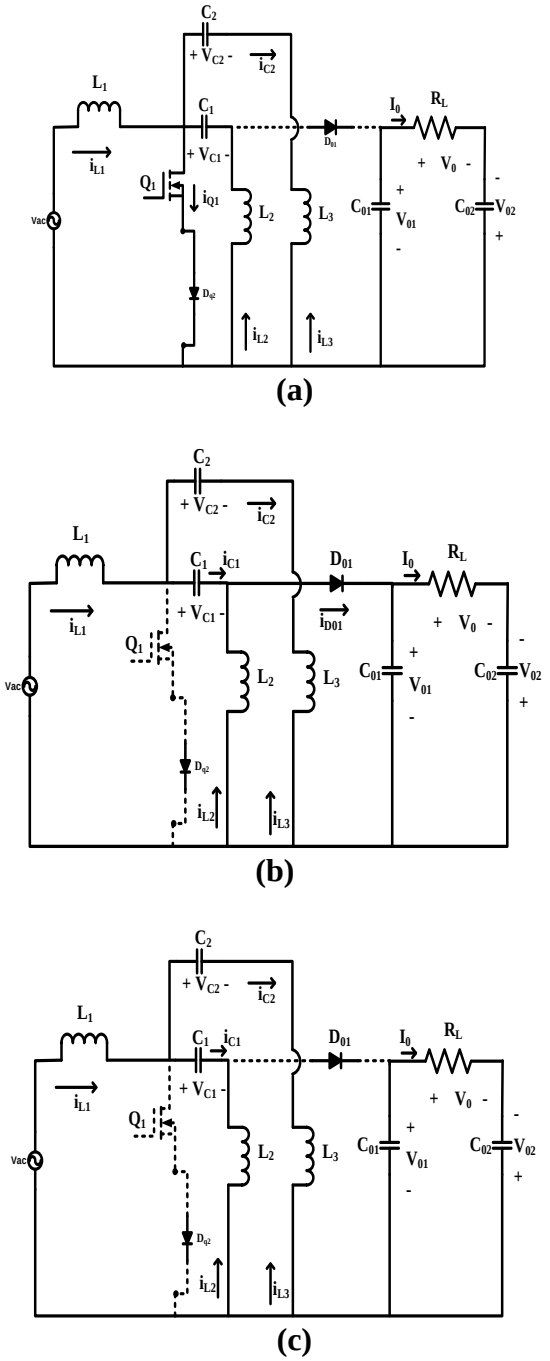

Figure 2: Modes for proposed converter during switching cycle *Ts*. (a) Circuit diagram for switch ON mode. (b) Circuit diagram for switch OFF mode. (c) Circuit diagram for DCM.

Simulation Results

The following parameters are used for the implementation of the bridgeless SEPIC converter.

1) Input voltage V_{ac} 120Vrms at (50Hz);
2) Output Voltage(V_0) 400V_{dc}
3) Output power P_{out} 200W
4) Switching frequency f_s 50 kHz;
5) Output capacitance C_{01} =C_{02} 400uF
6) Input inductance L_1 3.6mH
7) Output inductors L_2 , L_3 377uH The proposed converter was simulated in MATLAB Software.

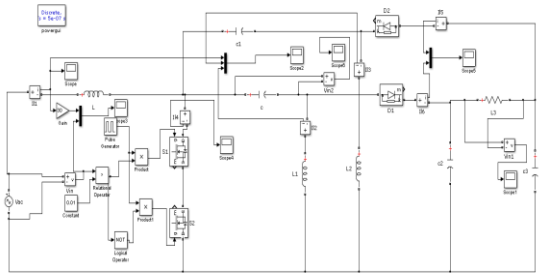

Figure (3): Matlab / simulink model of proposed bridgeless converter.

The input current and voltage waveforms are shown in below fig. Fig.4(a).

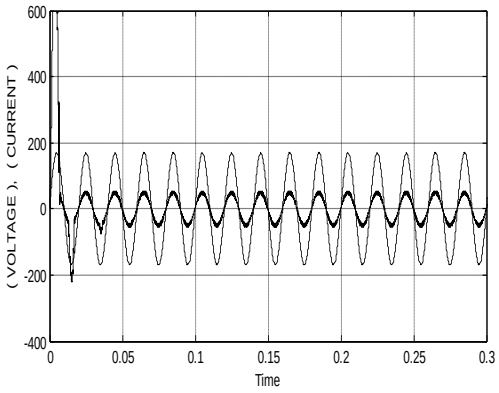

Figure 4(a): Input current and Input voltage

The output voltage V_0 ,which is shown in Fig.4(b). The average output dc voltage of the proposed converter is nearly 400V, with ripple 9V.

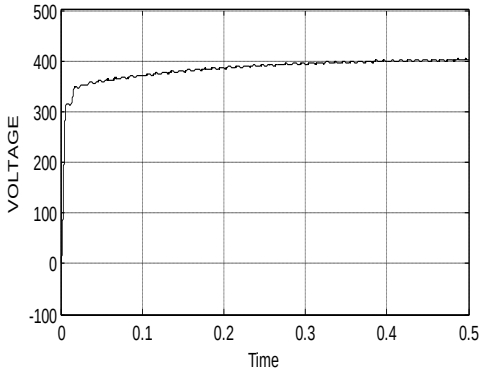

Figure 4(b): Output voltage

The intermediate capacitor voltage V_{C1}, is shown in the Fig.4(c).The voltage across the capacitor V_{C1} is nearly 180V.

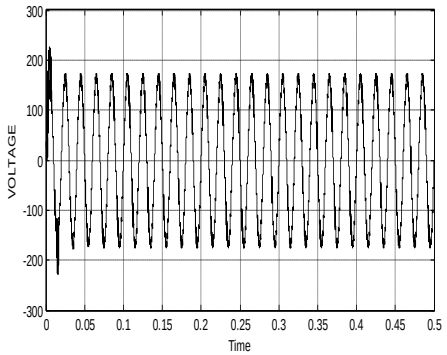

Figure 4(c): Capacitor voltage

The output diodes currents over a complete AC line cycle is shown in the Fig4(d). The diodes currents are nearly 9A.

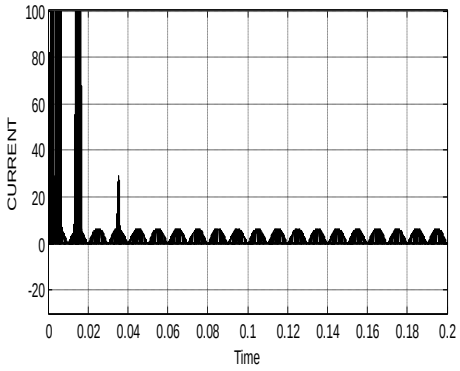

Figure 4(d): Diode currents

The switch current i_{Q1} is shown in Fig.4(e). The switch current is nearly 8A.

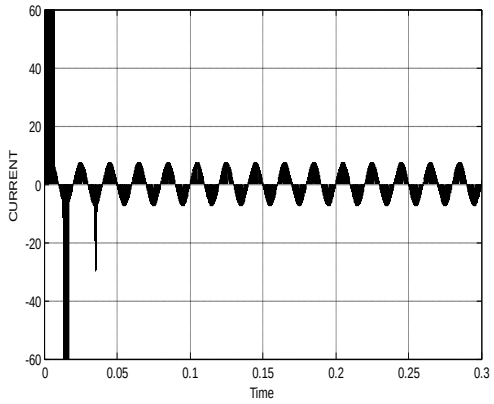

Figure 4(e): Switch Current

The simulation results verify the operating principles of this proposed SEPIC bridgeless converter.

Experimental Results

Converter specifications:

Input ac voltage Vac 6V
Output voltage V_O $25V_{dc}$
Input Inductor L_1 800uH
Output Inductors $L_2 = L_3$ 100uH
Link capacitors $C_1 = C_2$ 1uF
Filter Capacitors $C_{01}=C_{02}$ 470uF
Switching frequency 50kHz
Switches Q_1 and Q_2 3N80Z

The experimental results of the proposed converter are shown in fig 5(a) to 5(f).

The experimental output voltage of the proposed converter is shown in the figure 5(a). The output voltage is nearly 25V.

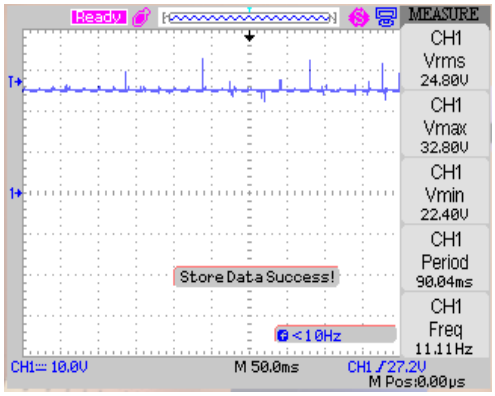

Figure 5(a): Output Voltage

The voltage across the capacitor C_{01} is shown in the fig5(b). The capacitor (C_{01}) voltage is 20V.

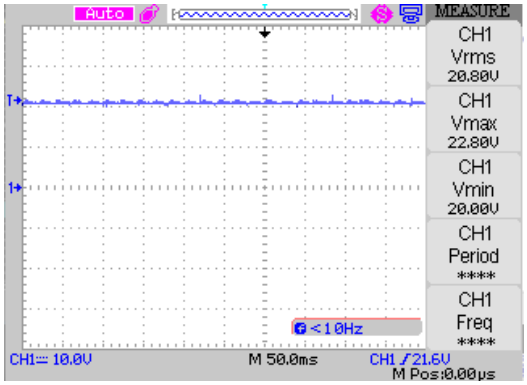

Figure 5(b): Output capacitor1 voltage

The voltage across the second output capacitor C_{02} is nearly 5V . The below figure 5.(c) represents the voltage across the second output capacitor C_{02}.

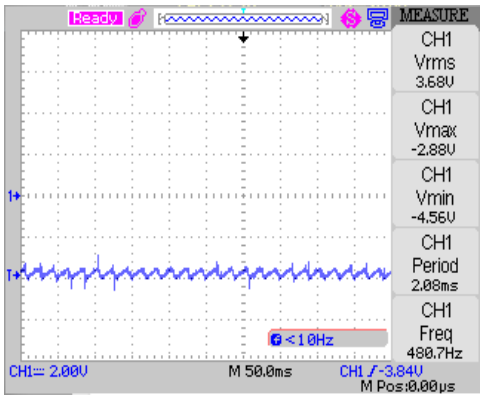

Figure 5(c): Output capacitor2 voltage

The switch voltage waveform is shown in the below figure 5.(d). The voltage across the switch is nearly 10V.

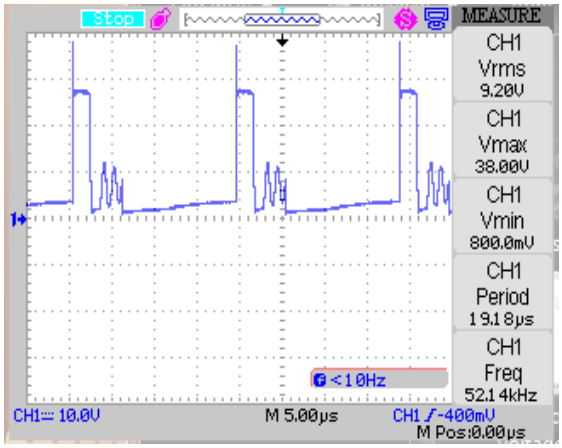

Figure 5(d): Switch Voltage

The voltage across the diode D_{01} is shown in the below figure 5(e). The diode (D_{01}) voltage is 22V.

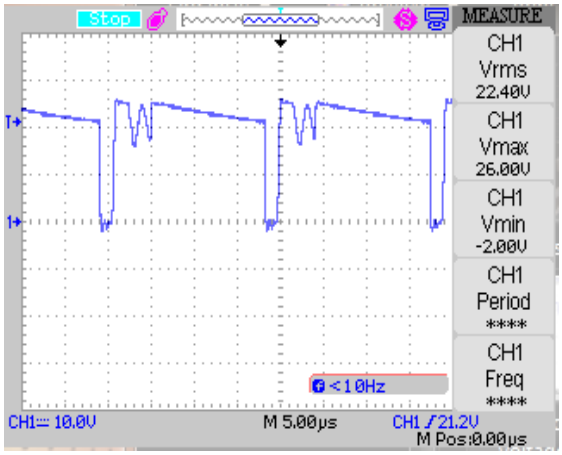

Figure 5(e): Diode1 Voltage

The voltage across the diode D_{02} is shown in the figure 5(f). The diode (D_{02}) voltage is nearly 8V.

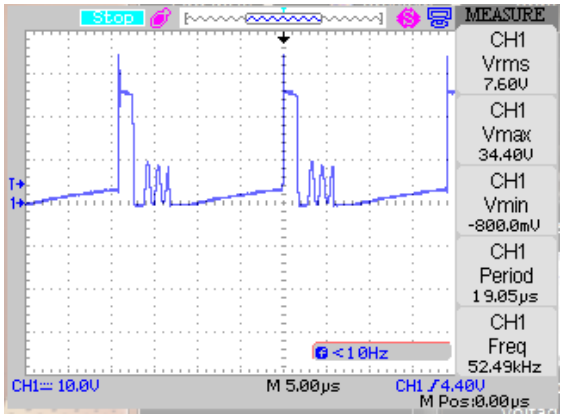

Figure 5(f): diode2 voltage

Conclusion

In this paper, a new bridgeless SEPIC rectifier with low input current ripple, reduced conduction losses has been implemented. This bridgeless SEPIC rectifier is developed using MATLAB/SIMULINK. The major features of this proposed converter comprise simplicity and low voltage stress on the switch and high efficiency. The performance of this converter is verified experimentally. This is easily extended to other power conversion systems. So, these are attractive characteristics for high voltage and also high power applications.

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