International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 11 (2015) pp. 27531-27540

http://www.ripublication.com

Validating The Choice of A, B, C Parameters of The PID Compensator For Controlling The Key Paramaters of High Frequency Dc-Dc Buck Converter

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Abstract

Excessive spread of portable electronic devices necessitates the usage of dc-dc converter for effectively managing the limited power source[1] Controller circuit is mandatory for any power stage. PID compensator[2] is the effective feedback control mechanism. Proper tuning of a, b, c parameters of the compensator ensures a loop system, that is stable and close and also the dynamic response of the digital controller is improved. This tuning is necessary to saturate the output parameters of the converter within minimum settling time. The closed loop configuration of this dc-dc converter and PID controller has been implemented using MATLAB /Simulink environment

Keywords: dc-dc converter, digital controller, PID compensator, dynamic response, stable closed loop system

Introduction

Dc-Dc Buck Converter

Portable electronic devices use dc-dc buck converter for effectively managing the limited battery source. It produces the output dc voltage which is lower than that of the input dc voltage i.e. it is a step down converter.

Operating Modes Of Buck Converter

- Continuous Conduction Mode-CCM
- Discontinuous Conduction Mode-DCM

Continuous Conduction Mode

This mode of operation supports heavy loaded condition and the current of the inductor never becomes zero during the off condition.

Discontinuous Conduction Mode

The mode of operation supports low loaded condition and the current of the inductor drops down to zero during the off condition.

Closed Loop Configuration of Buck Converter And Digital Controller

The main objective of this closed loop configuration is to produce a regulated output voltage despite variations in load and input voltage parameters. This closed loop configuration is depicted in the figure 1.

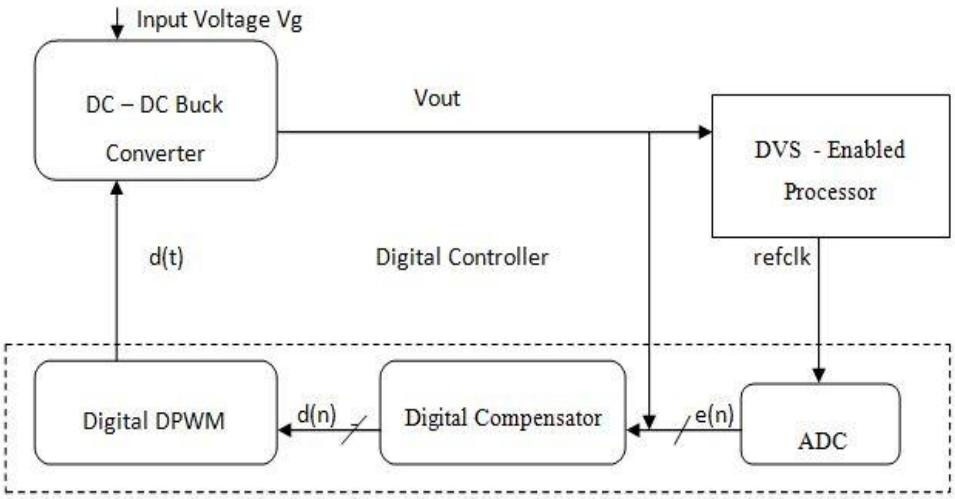

Figure 1: Closed Loop Configuration of Buck Converter And Controller

The converter output voltage is sampled by an ADC (Analog to Digital converter) circuit. This ADC circuit compares the sampled values of the output voltage with the sampled values of the reference voltage and produces the digital error signal e (n). This e (n) is fed to the digital compensator that computes the discrete command d (n). Digital pulse width modulator (DPWM) produces the duty signal d (t) from discrete command d (n). This duty signals d (t) is used to control the buck converter switches SW1 and SW2 to regulate the output voltage of the converter.

Importance of The PID Compensator

PID compensator computes the discrete control command d (n) for controlling the switches of the buck converter. Switching converters often exhibit non linear

switching characteristics that affect the stability of the system. The systems stability is ensured by designing this compensator. In order to ensure improved buck converters dynamic response and to saturate the converter's output voltage within minimum settling time, proper tuning of the parameters (a, b, c) of the PID compensator is mandatory. These a, b, c values are directly obtained from the discrete model of the converter.

Focus of The Proposed Work

The proposed work mainly focuses on validating the choice of a, b, c parameters of the digital compensator. The discrete model of the buck converter are used to design these values properly. The main objective of this proposed work is to produce saturated output voltage within minimum settling time and thus assuring the stability of the system. This also improves the dynamic response of the system.

Related Work

Different digital controller design approaches are available. The two general methods for designing the digital PID compensator are

- Digital redesign method
- Direct digital method

Digital Redesign Method

In this method, continuous domain is used to design the compensator and the calculated transfer function is then converted to discrete domain. Another simpler method is Backward Euler method that does not give clear information about the frequency and impulse response. The method that eliminates the aliasing effect by transforming the s-plane's left hand side into the z-plane's domain is the Bilinear Transformation method. The step response of the system is preserve in Step Invariant transformation but does not preserve the impulse and frequency response. The preserved pole-zero location which introduces aliasing when greater frequencies of Nyquist frequency than zeros are seen in pole/zero match transform

Direct Digital Method

In this method the continuous system domain is transformed to Z-domain initially and then directly the compensator is designed in this domain.

Here several methods are also available. Backward Euler method is the simplest method and it is easy to implement.

Conventional PID Structure

The conventional PID structure is depicted in the figure 2.

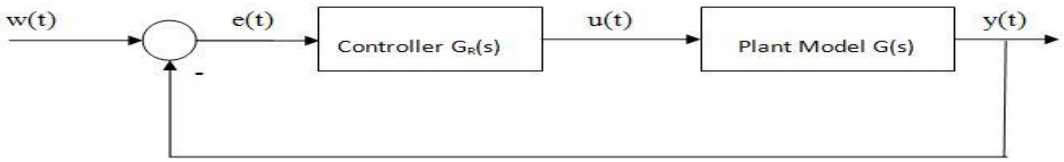

Figure 2: Conventional PID structure

e- Tracking error
w- Reference variable
u- Plant model variable
y- Controlled output variable

The mathematical representation of the PID compensator is given by the equation (1).

$$u(t) = Pe(t) + I\int e(t)\,dt + D\frac{de(t)}{dt} \quad (1)$$

D,I, P – derivative, integral and proportional gains of the system

The error signal is computed by using the formula e (t) = w (t) – y (t)

The s- domain transfer function is given by the equation (2)

$$G(s) = P + \left(\frac{I}{s}\right) + (D.s) \quad (2)$$

Settling, rise, overshoot, steady state error the four major characteristics of the closed loop response of the system

Proposed Model of The PID Compensator

PID compensator computes the discrete command d (n) to control the switches of the buck converter. The design that is introduced here I Pole-zero cancellation. The poles of the buck converter introduces phase drop in the system which is not desirable. This also affects the stability of the system. To cancel these poles, PID compensator zeros are introduced. According to this method, the pole is cancelled if the zero is located close to the pole. By this method, the two poles of the buck converter are cancelled by using the two zeros of the PID compensator. This improves the stability of the system with overshoot that is minimum. All mentioned objectives are met by adjusting the gain parameters of the PID controller.

The PID controller has the s-domain transfer function is given by the equation (3)

$$G_{pid}(s) = K_p + \frac{K_i}{s} + K_d s \quad (3)$$

s-domain transfer function is converted into the z-domain transfer function by using the Backward Euler's method by putting s = $((1-z^{-1})/Ts)$, where Ts is the switching period of the converter.

The z-domain transfer function is given by the equation (4), (5), (6), (7) and (8)

$$G_{pid}(z) = \frac{d(z)}{e(z)} \quad (4)$$

$$G_{pid}(z) = \frac{(a + bz^{-1} + cz^{-2})}{(1 - z^{-1})} \quad (5)$$

$$a = \left(K_i T_s + K_p + \frac{K_d}{T_s}\right) \quad (6)$$

$$b = \frac{(-K_p - 2K_d)}{T_s} \quad (7)$$

$$c = \frac{K_d}{T_s} \quad (8)$$

The final equation of the PID compensator is given by the equation (9)

$$d\,(n) = d\,(n-1) + a * e(n) + b * e\,(n-1) + c * e(n-2) \quad (9)$$

where d (n) is the discrete command and e(n) is the error value

The s-domain transfer function is given by the equation (10)

$$G_v d\,(s) = \frac{V_g\,(1 + sCR_{esr})}{LC\,s^2 + \frac{L}{R}s + 1} \quad (10)$$

Where Vg, Resr, R, C, L, represents the input voltage, resistance of the capacitance, load resistance, output capacitance and inductance respectively.

By using Backward Euler's method, the z-domain transfer function is given by (11)

$$G_v d(z) = V_g \frac{\left(1 + \frac{CR_{esr}}{T_s}\right) - \frac{CR_{esr}}{T_s} z^{-1}}{\left(\frac{LC}{T_s^2} + \frac{L}{RT_s} + 1\right) - \left(\frac{2LC}{T_s^2} + \frac{L}{RT_s}\right) z^{-1} + \frac{LC}{T_s^2} z^{-2}} \quad (11)$$

Design Consideration

For the optimized design the following parameters are designed as shown in table 1.

Table 1: Design Consideration For The Proposed Approach

DESCRIPTION	PARAMETER	NOMINAL VALUE
Input voltage	Vg	5
Inductance	L	2.2uH
Capacitance	C	11uF
Equivalent series resistance	Resr	10mohm
Load resistance	R	10ohm
Switching Frequency	F	1MHz

The transfer function of the buck converter and the PID compensator are mapped and other mandatory value are calculated by considering all the above parameters. The obtained values are c=24.2, b= -48.62,a=25.42. These values can be set so that

the stability of the system is ensured. From this the dynamic response of the system can also be improved. These values are stored in look-up table format. The external memory storage is reduced by smaller values of a, b, c. All the product values are calculated for error value range {-7, 7} and pre-computed to reduce the computational complexity.

Experimental Setup

The closed loop configuration of this PID controller and the buck converter is designed and implemented in MATLAB/Simulink as shown in figure 3.

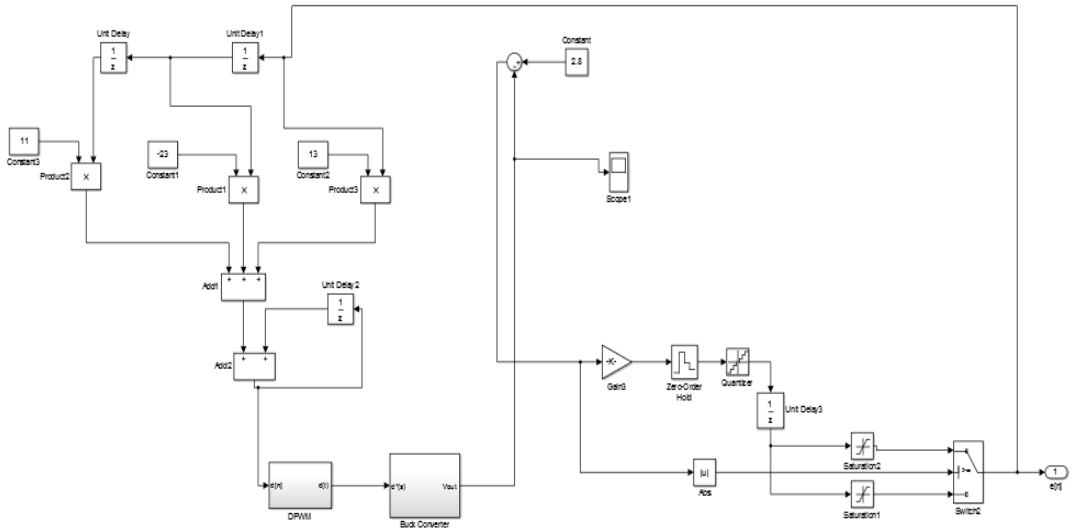

Figure 3: Simulink model of the closed loop configuration of the buck converter and PID controller

Results and Discussion

The closed loop configuration of buck converter and digital controller without proper tuning of a, b, c parameters**:**

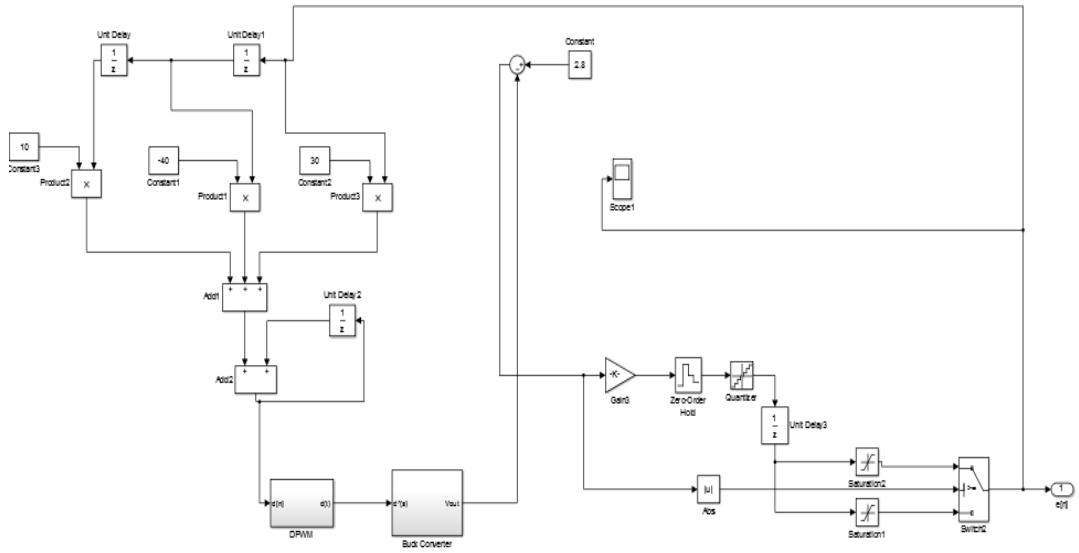

Figure 4: Simulink model of the closed loop configuration without proper tuning of PID parameters

The above MATLAB model figure (4) shows the closed loop model of buck converter and digital controller without proper a, b, c values. The corresponding regulated output voltage of buck converter without saturation is depicted in figure (5), figure(6) represents duty signal d(t) and error signal e(n)

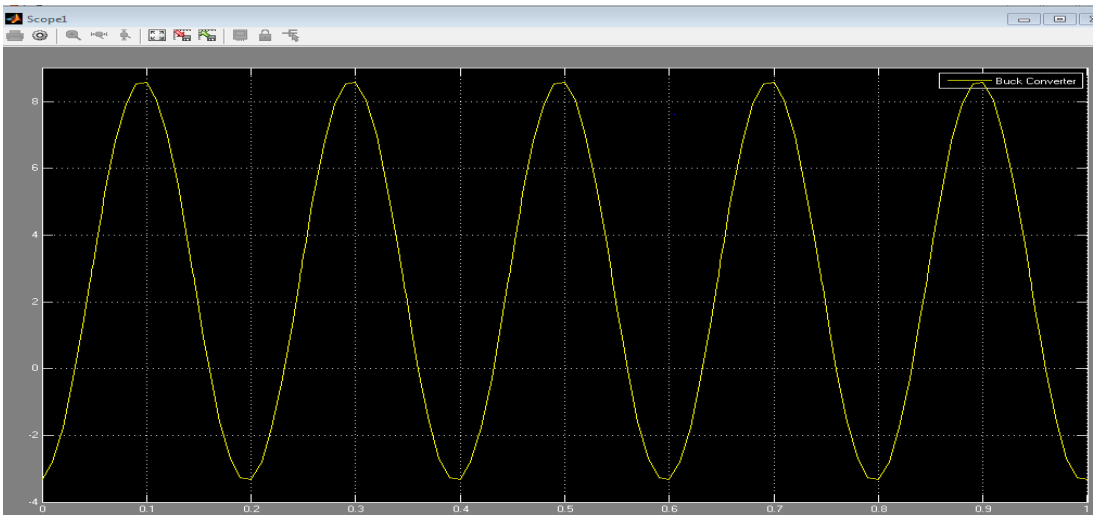

Figure 5: Regulated Output Voltage of Buck Converter Without Saturation

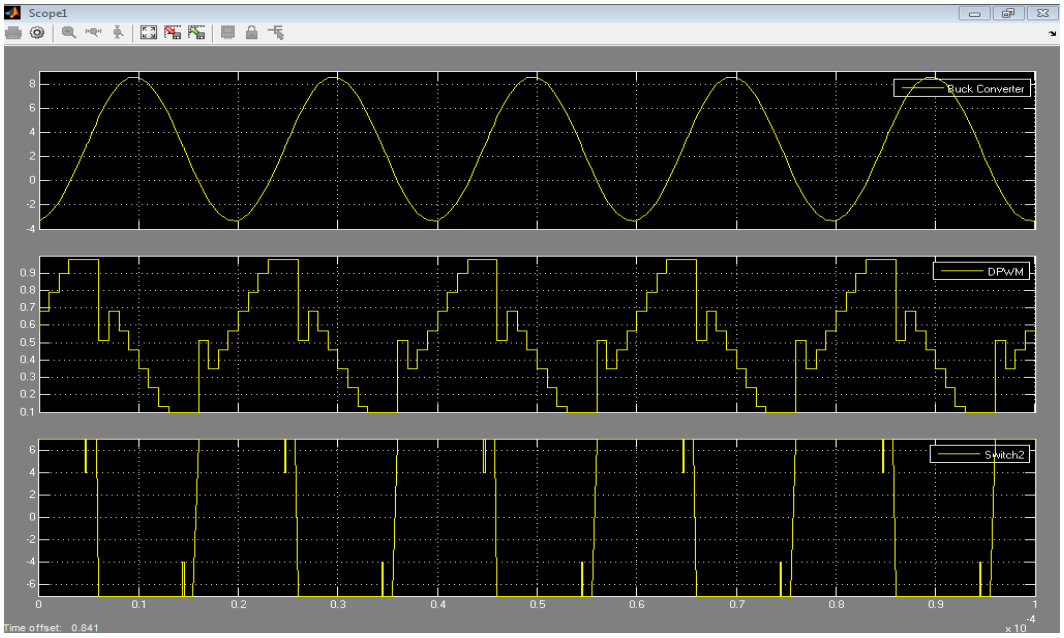

Figure 6: Duty signal d(t) and error signal e(n) of closed loop buck converter

The closed loop configuration of Buck converter and digital controller with proper tuning of a, b, c parameters:

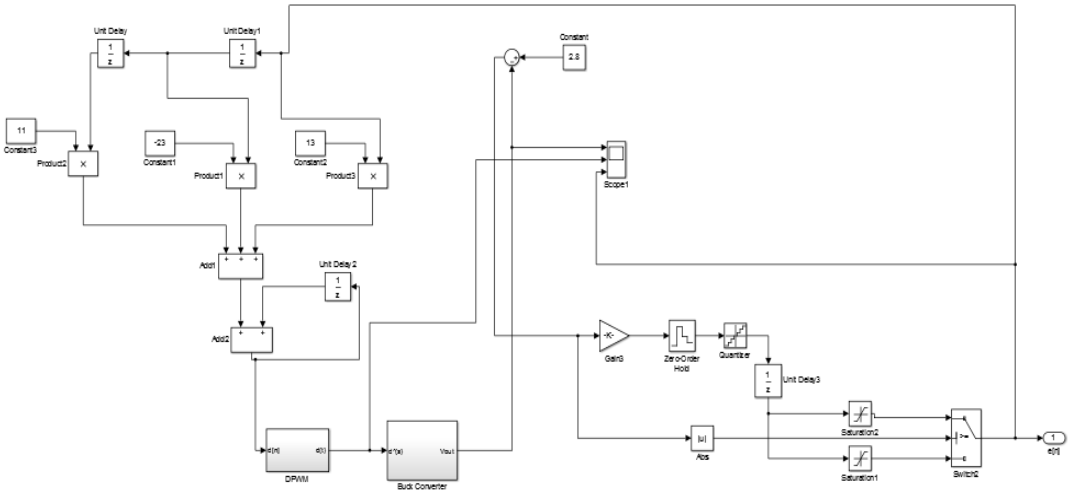

Figure 7: Simulink Model of Buck Converter With Proper A, B, C Values

The above MATLAB model figure(7) shows the model of buck converter with close loop structure and digital controller that has proper values of a, b, c. The corresponding regulated output voltage of buck converter with saturation is depicted in figure (8) , figure(9) represents duty signal d(t) and error signal e(n)

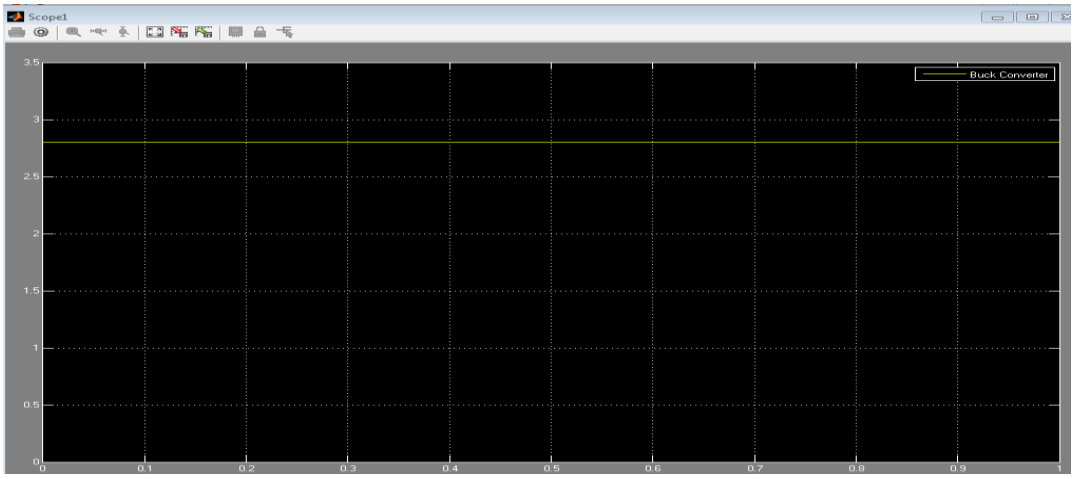

Figure 8: Saturated regulated output voltage of buck converter

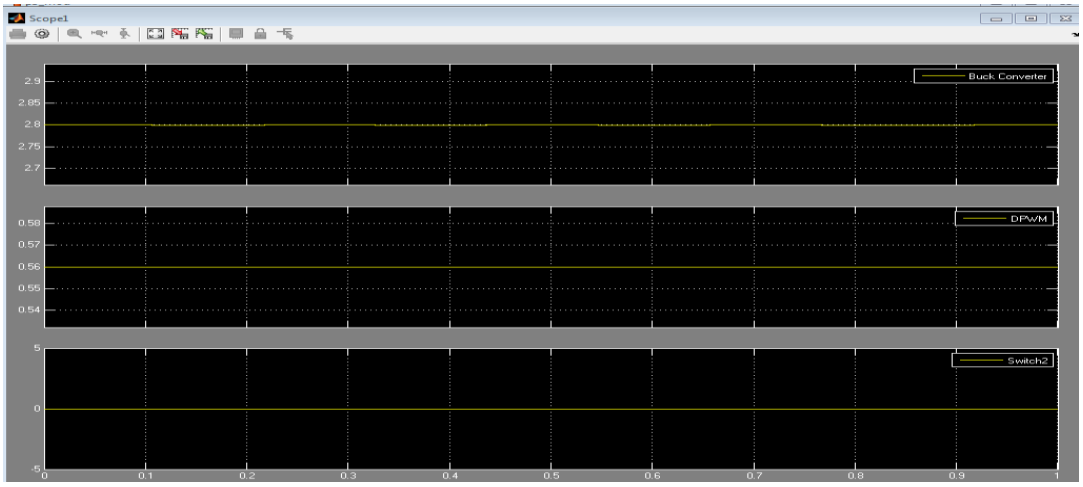

Figure 9: Duty signal d(t) and error signal e(n) of closed loop buck converter

From the simulation result of the proposed model, we can clearly notice that the buck converter output voltage value is saturated. This is done with minimum settling time without any voltage overshoot. This ensures that the system is stable and it improves the dynamic response of the system. All these results are possible only when a, b, c parameters are chosen as per the above guidelines. For all other values of a, b, c parameters the system will not be stable and the saturation of the buck converter output parameter is not obtained. Hence proper tuning of the parameters a,b,c are mandatory so that we can obtain a stable closed loop system.

Conclusion

This proposed design architecture provides the stable closed loop system which has voltage overshoot that is minimum. The dynamic response of the controller is also

improved. The buck converter is saturated over the output voltage is achieved by the proper tuning of a, b, c parameters. Also this is achieved within minimum setting time. Thus the stability of the proposed system is verified by using the MATLAB results.

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