International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 10, Number 11 (2015) pp. 27559-27568

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Design of A Stable Closed Loop Model of Buck Converter and Digital Controller With Tuning of PID Parameters

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Abstract

Proliferation of the electronic devices that are portable leads to various power manageable techniques. Dynamic voltage scaling is the effective power management technique for properly managing the limited available battery source. Steady state operation and dynamic range of voltage regulation are the key challenges while implementing the DVS technique. This DVS technique utilizes the dc-dc buck converter for power management because of its higher efficiency. PID compensator plays a vital role in deciding the stability of the system. So proper tuning of these parameters are mandatory for obtaining a stable closed loop system. The closed loop configuration of this buck converter and the controller is first implemented in C programming language using integer representation and then it is converted into a behavioural model in verilog HDL. The functional and timing simulation of this design is done by using Altera Quartus II simulation tool.

Index Terms: dynamic voltage scaling, dc-dc buck converter, PID compensator, stable closed loop system, dynamic voltage regulation

Introduction

Dynamic Voltage Scaling Technique

Rapid growth of electronic devices that are portable has led various power management techniques developement. Dynamic voltage scaling is the effective

technique for managing the limited available battery source of these mobile electronic devices. Dynamic power components generally dominates the Power consumption of an IC (integrated circuit) which is given by multiplication of the operating clock frequency and supply voltage taken to its square.

Scaling down of the supply voltage is a technique where the dynamic power consumption can be greatly reduced. For implementing this technique, two challenges are need to be addressed: steady state operation and dynamic voltage regulation. These challenges are addressed with the help of buck converter since it has higher efficiency.

Dc-Dc Buck Converter

Step down converter-Buck converter where the output voltage that is regulated is slightly lesser than the voltage given at the input. It is utilized by the DVS technique for effectively managing the available battery source. The typical buck converter configuration is shown in figure 1.

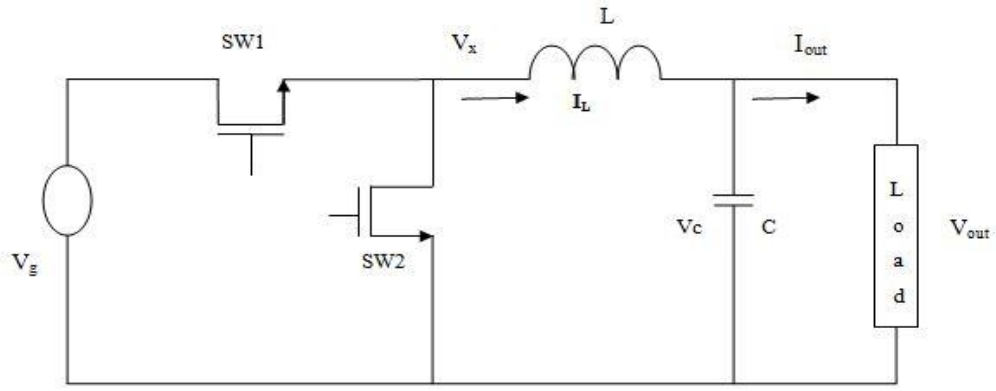

Figure 1: Typical Dc-Dc Buck Converter Model

Buck Converter- Conducting Modes

It can be classified as

- Continuous conduction mode
- Discontinuous conduction mode

Continuous Conduction Mode

This mode operation is supported by heavy loaded condition and the inductor current never becomes zero under OFF condition.

Discontinuous Conduction Mode

This mode operation is supported by light loaded condition and the inductor current drops down to zero under OFF condition.

Digital Controller

For any power stage, the controller architecture plays a very important role in controlling the operating parameters of the converter stage.

Contolling Methods

The controlling methods are classified as follows.

- Analog mode of control
- Digital mode of control

Initially analog method of control is used for the controlling purpose. But it is sensitive to high frequency noise and analog component variations. So digital control method is preferred which is insensitive to high frequency noise and component variations. This digital controller can be easily modeled by using verilog HDL and can be designed using automated tools. This digital controller consists of various blocks such as ADC, PID and DPWM blocks.

Components of The Digital Controller Architecture

The digital controller architecture comprises of the following blocks.

- Analog to digital converter
- PID compensator
- Digital pulse width modulator

Analog To Digital Converter

This resolution of this block determines the precision with which the controller output voltage needs to be regulated. Under any transient conditions, the reference voltage with close tolerance to that output voltage that is regulated is ensured. This block compares the reference voltage with the output voltage that is regulated and produces an error value e (n) digitally. This error value is then fed to the PID compensator block. Here delay line ADC is preferred. This delay line ADC uses propagation delay of the CMOS logic gate for the conversion mechanism. This provides better accuracy and flexibility.

Proportional, Integral and Derivative Compensator

For controlling the switches of the buck converter, this compensator produces the discrete control command d (n). Non-linear switching characteristics of the converter affect the stability of the system. To overcome this issue, we need to design the compensator properly. For obtaining saturation of the converter output parameters and to improve the dynamic response, a, b, c parameters of the compensator should be properly tuned. These parameters are directly obtained from the discrete model of the buck converter. This improves the stability of the system.

DPWM

The DPWM is used to generate the duty signal d (t). This duty signal d (t) controls the operating MOSFET switches of the buck converter. The resolution of this DPWM provides the precise voltage regulation and avoids limit cycle oscillations. Low

power, low latency, high resolution and linearity are some of the key factors of the pulse width modulator. The overlap of set and reset pulses of the logic provides hardware timing constraints. These constraints are overcome by the edge triggered logic.

Tuning The Parameters of The PID Compensator

Proportional, integral and derivative compensator produces discrete command d (n) for controlling the buck converter switches. The stability of the system is affected by the phase drop in the system which is introduced by the poles of the buck converter. To cancel these poles, pole-zero compensation method is introduced. The two poles of the buck converter are cancelled by the two zeros of the compensator. The stability of the system is improved by this method. To achieve all these objectives, gain parameters of the compensator are tuned properly.

The s- domain transfer function is converted into z-domain transfer function by the Euler's method (Backward method) as shown in (1).

$$G_{pid}(s) = K_p + \frac{K_i}{s} + K_d s \tag{1}$$

Where Kp, Ki, Kd are the proportional, integral and derivative gain of the compensator.

By putting s = ((1-z^{-1})/Ts), it is converted into z- domain function represented by (2) to (5).

$$G_{pid}(z) = \frac{(a + bz^{-1} + cz^{-2})}{(1 - z^{-1})} \tag{2}$$

$$a = \left(K_i T_s + K_p + \frac{K_d}{T_s}\right) \tag{3}$$

$$b = \frac{\left(-K_p - 2K_d\right)}{T_s} \tag{4}$$

$$c = \frac{K_d}{T_s} \tag{5}$$

These a, b, c parameters should be tuned properly.

From the discrete model of the buck converter's discrete model we obtain the value as depicted in (6).

$$G_v d(z) = V_g \frac{\left(1 + \frac{CR_{esr}}{T_s}\right) - \frac{CR_{esr}}{T_s} z^{-1}}{\left(\frac{LC}{T_s^2} + \frac{L}{RT_s} + 1\right) - \left(\frac{2LC}{T_s^2} + \frac{L}{RT_s}\right) z^{-1} + \frac{LC}{T_s^2} z^{-2}} \tag{6}$$

Where Vg, Resr, R, C, L, represents the input voltage, resistance that are equivalent and series of the output capacitance, load resistance, output capacitance and inductance respectively.

Discrete command d(n) is finally obtained from compensator given by (7)

$$d\,(n) = \; d\,(n-1) + \; a * e(n) + \; b * e\,(n-1) + \; c * e(n-2) \tag{7}$$

Where the error value is given by e(n) and the previous instance discrete command is given by d (n-1).

After all these manipulations, the final values of a, b, c are a= 25.42, c=24.2, b=-48.62

Hence these values are used for calculating d (n) which ensures the stability of the system. It also improves the dynamic response of the system.

Closed Loop Configuration of Buck Converter and Digital Controller

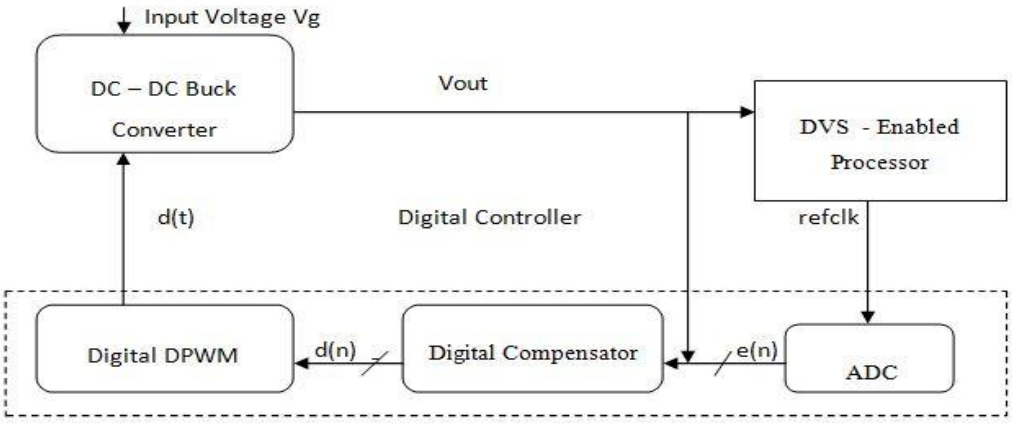

Figure 2: Closed Loop Configuration of Buck Converter And Digital Controller

The figure shows the buck converter with the digital controller in the closed loop configuration. Initially the buck converter produces a regulated output voltage Vout. This regulated voltage at the output is compared with the voltage(reference) in analog to digital converter block. The digital error value e (n) is generated. The proportional, integral and derivative compensator takes this e (n) as input and produces the discrete command d (n) as output. Then it is given to the digital pulse width modulator block for generating d(t),duty signal. The generated duty signal d (t) is used to control the MOSFET switches of the buck converter.

Proposed Approach

Motivation For The Proposed Approach

In all the existing methods, the stability of the system is not ensured in the closed loop configuration of the controller and the buck converter. The regulated output voltage is subjected to the limit cycle oscillation issues. This is because, the parameters of the

compensator are not tuned properly and the converter's parameters are not calculated according to these variations. This gives the motivation for the proposed approach to address all these issues by an effective verilog model.

C Code Implementation of The Proposed Model

The entire design is initially modeled in C programming language for obtaining better accuracy within stipulated time. This model is developed using floating point representation of the parameters and then it is converted into an integer level implementation. This gives accurate results when simulated in event driven simulator.

Design Consideration

The parameters of the closed loop configuration should be designed as depicted in table 1.

Table 1: Design Consideration

DESCRIPTION	PARAMETER	NOMINAL VALUE
Input voltage	Vg	5000
Reference voltage	Vref	2800
Inductance	LMOD	46
Capacitance	CMOD	48
Load resistance	RMOD	1
Switching Frequency	F	1MHz
Switching period	Ts	1us
ADC resolution	INVERSER	37
PID parameters	a, b, c	25.42, -48.62, 24.2

Initially for calculating the converter output parameters, the initial values are V= 2000, and IL=1.

The inductor current IL is calculated by using the equations (a)

$$IL = (Vg * d) – (V * LMOD) \quad (a)$$

Then the variation in the output voltage is calculated by using the equation (b)

$$dv = IL – (V * CMOD) \quad (b)$$

The updated voltage value V is given by equation (c)

$$V1 = V + dv \quad (c)$$

This V1 voltage variation is used for updating the further regulated output voltage as depicted in equation (d) and (e)

$$dv = IL – (V1 * CMOD) \quad (d)$$

$$V = V1 + dv \quad (e)$$

Then the corresponding reference and regulated output voltage are represented by 8 bit values as shown in (f) and (g)

$$lval1 = Z * Vref \quad (f)$$

$$lval2 = Z * V \quad (g)$$

The difference between these two value are considered as the error value c0 by the PID compensator block as shown in (h)

c0 = lval1-lval2 (h)

these error values are restricted to the {+ /- 7} and {-4 to +4} range based upon certain conditions and the discrete command d (n) is calculated by using equation (i).

d (n) = d(n-1) + (a *e (n)) + (b * e (n-1)) + (c * e(n-2)) (i)

This d is updated for multiple iterations and the corresponding buck converter output parameters are updated accordingly. This type of closed loop configuration ensures a stable closed loop system without any limit cycle oscillation issues.

Verilog HDL Implemntation of The Proposed Approach

The integer representation of C code is directly modeled into the integer representation of the verilog HDL for obtaining better results with greater accuracy. The signed part representation is taken care properly by proper arithmetic shifting operations. Initially the model is tested for open loop condition and later it is tested for the closed loop condition. The parameters are calculated in the same manner as that of C code implementation. The error value generation and discrete command generation are taken care by the PID module and all these parameters are updated continuously to ensure a stable closed loop system and also to improve the dynamic response of the system.

Experimental Results

C Code Implementation Results

The proposed closed loop configuration of the digital controller and the buck converter is implemented in C language and the results are obtained using event driven simulator.

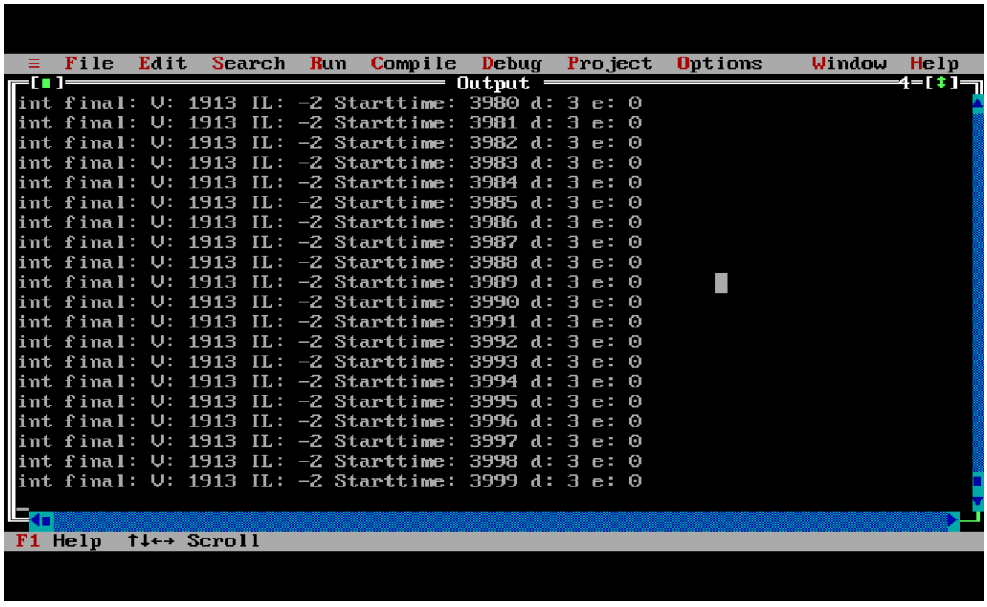

Figure 3: C Code Simulation Result of The Proposed Model

Verilog HDL Implementation Results

The proposed model is then implemented in Verilog HDL and the functional and timing simulation is done by using the Altera Quartus II simulation tool.

Functional Simulation Result

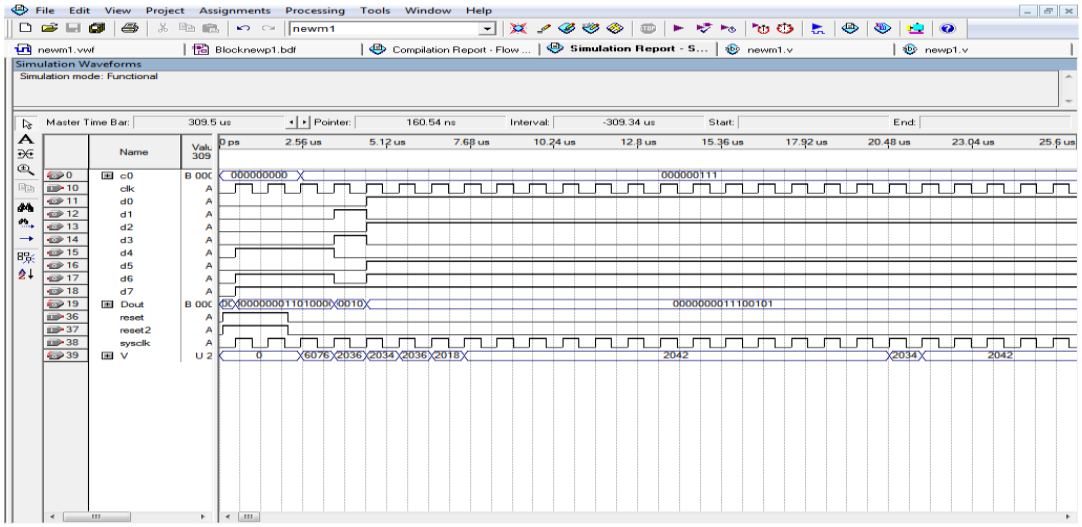

Figure 4: Functional Simulation Result of The Proposed Model

We can see that the regulated output voltage V varies for discrete command d (n). The error value c0 is also generated by comparing lval1 and lval2 respectively. The discrete command d is generated based upon the generated error values.

Timing Simulation Results

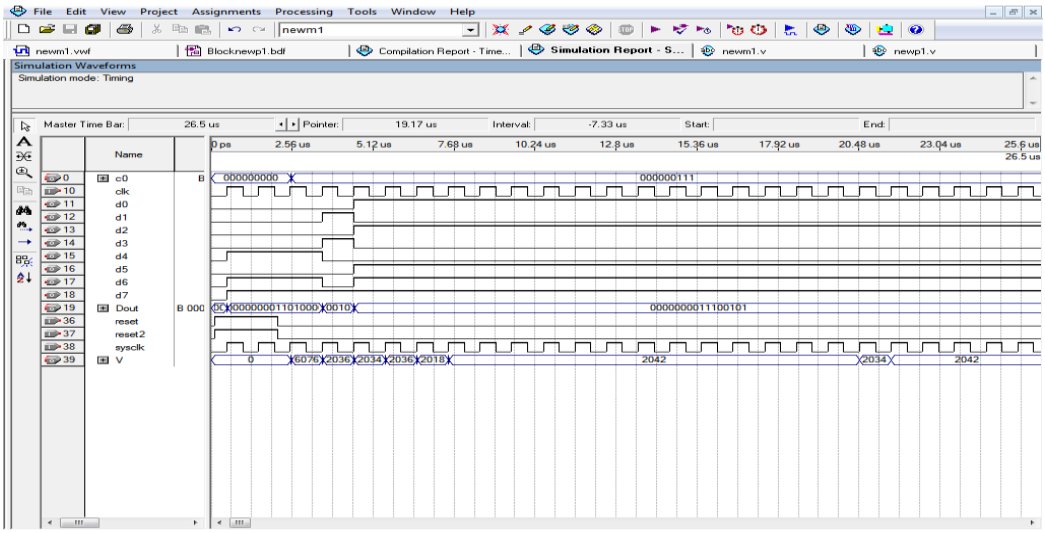

Figure 5: Timing Simulation Results of The Proposed Model.

We can see that the simulation results are obtained properly and the design meets all the timing requirements properly. All these results ensure a stable closed loop syatem without any limit cycle oscillation issues. Dynamic response of the system is also improved.

Conclusion

In this proposal, the closed loop configuration of the buck converter with the digital controller is implemented. By proper tuning of the parameters of the PID compensator, the stability of the system is achieved. Dynamic response of the system is also improved by this proposed approach. The correctness of the implementation is verified by using the simulation results obtained by using Quartus II simulation tool. This design is suitable for any entry point FPGA platform.

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