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FPGA Implementation of An Area Efficient Digit-Serial FIR Filter's Using CSE and GB Algorithm

Dr. FazalNoor Basha[1], K.Vamsi Krishna[2]
[1].Associate Professor, K L University, Vaddeswaram, Guntur, A.P
[2] M.Tech Student, K L University, Vaddeswaram, Guntur, A.P
E-mail: [1] fazalnoorbasha@kluniversity.in , [2]vamsikrish26na@gmail.com

Abstract

Many efficient algorithms have been proposed to reduce the area occupied by an FIR filters using multiple constant multiplications (MCM) implemented by shifting-adding techniques. In this paper a new approach has been implemented which reduce the hardware of an FIR filters by using common sub expression and Graph Based algorithm. Experimental results indicate that the new algorithm gives better results than the previously proposed algorithms in terms of area at gate-level and yields alternative low-complexity designs relatively to the bit-parallel design.

Keywords: Verilog, Multiple Constant Multiplication(MCM), finite impulse response, Low complexity, CSE algorithm, CSD.

Introduction

In digital signal processing (DSP) systems finite impulse response (FIR) filters have very much importance since their characteristics in linear-phase and feed-forward implementations make them very useful for building stable high performance filter architectures. The direct and transposed form FIR filter logic diagrams are illustrated in Fig.1(a) and 1(b). As shown in figure both architectures have similar complexity in hardware, and the performance and power efficiency.

The architecture of a multiplier of the digital FIR filter[3] in its transposed form is shown in [Fig. 1(b)], where the multiplication of filter inputs with the filter coefficients is realized, due to the significant impact on the complexity and performance of the design because a large number of constant multiplications are required. This is generally know as the multiple constant multiplications (MCM) operation[4] and is also a central operation and performance bottleneck in many other DSP systems such as fast Fourier transforms, discrete cosine transforms (DCT's) and ECC codes.

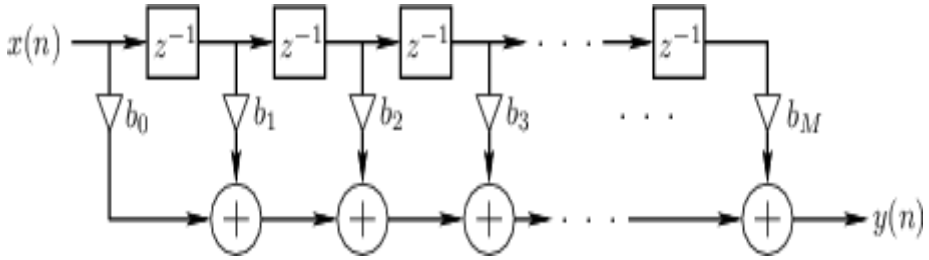


Figure 1: Design of FIR Filter. (A) Direct Form With Generic Multipliers

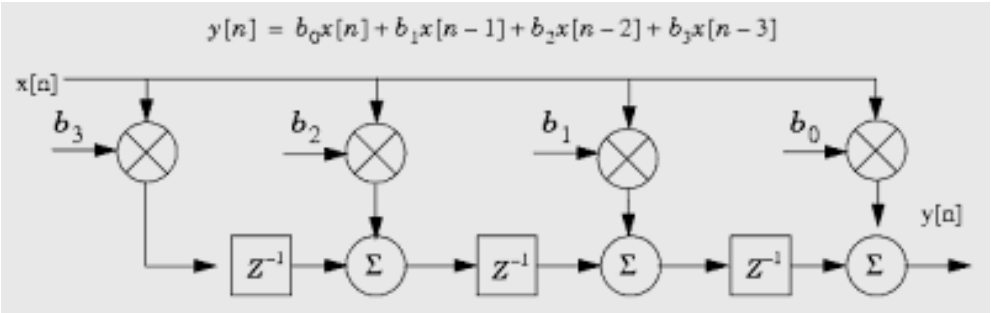


Figure 1: Design of FIR filter. (a) Transposed form with generic multipliers

Multiple constant multiplications is involved to generate constant multiplication in Digital Signal Processing, ECC codes, MIMO system applications.

In most of the applications complete use of multipliers are not needed. As the coefficients are constant then constant multiplication can be used. So depending upon the constant coefficients MCM architecture can be constructed, the designed architecture can be called as many times it required. There are two methods to implement Constant multiplication either by digit serial design or digit parallel design. Digit-parallel design of constant multiplier needs external wire for shifting. Hence it occupies more area while implementation takes place in FPGA or any other ASIC. So digit serial design overcomes area constrain with acceptable delay timing.

Multiplication done with constants is known as constant multiplication. This process is used mostly in filter functions. There are two different types of constant multiplications such as Single Constant Multiplication (SCM) and Multiple Constant Multiplication. The input sample is multiplied with single specific coefficient to produce output is called SCM. Canonical Signed Digit (CSD)[7] or Minimal Signed Digit[8] number system is used to implement SCM multipliers.

Input samples are multiplied with multiple coefficients to produce multiple outputs is known as MCM. Multiplication is a process of shift and adds operation[1]. Constant multiplier design includes the number of adders, subtractors and shifters according to the coefficient pair.

FIR filter output can be obtained by multiplication of input sample and impulse response. Direct form and transposed form implementations are two forms of FIR filter implementations. Instead of direct form, transposed form is most effective. The Multiplication process takes place in multiplier block. Thus transposed form

multiplier blocks in FIR filter will replace by MCM architecture also known as shift and add architecture.

FIR filter gives guaranteed stable, feed forward and linear phase. In FIR filter impulse response is equal to the number of coefficients. When compared to Infinite Impulse Response (IIR) filters it is not the case. Thus this FIR filter implementation is sometimes called as multiplier less digit based recoding method.

Objective Main objective is to eliminate multiplier block and introducing MCM architecture in digit serial FIR filter for the reduction of multiplication in the form of shift and add operations.

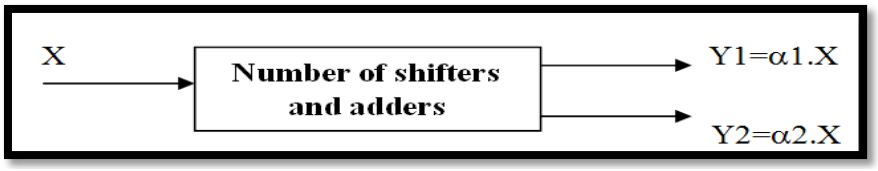


Figure 2: MCM operation

In Figure.2 X denotes input sample; α1 and α2 are coefficients; and Y1 and Y2 are the filter outputs.

Architecture with the same input which is multiplied by a set of constant coefficients is said to be MCM. Outputs Y1, Y2 are produced by multiplying Serial[2] input data with two pair of coefficients.

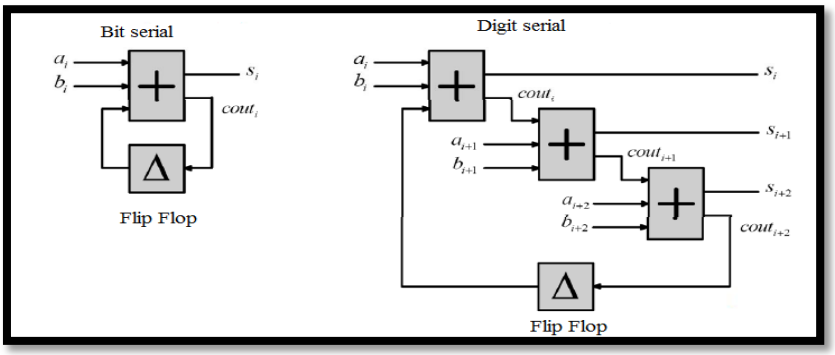


Figure 3: Digit-Serial operation

Bit-serial operation and Digit-serial operation are the two cases for serial addition, which is shown in Figure 3, while Digit-Serial operation needs less number of delay elements such as flip-flop for addition or subtraction when compared to Bit-serial operation.

Proposed Work

Common sub expression algorithm is used in design of MCM architecture with partial product sharing algorithm (Digit based recoding). In proposed method, the Graph

Based (GB) algorithm is used for this purpose. In proposed design 16 tap FIR filter have been designed. The sixteen constants are taken as coefficient pair. According to principle of MCM constant multiplication[9] is performed by number of shifting and adding operation.

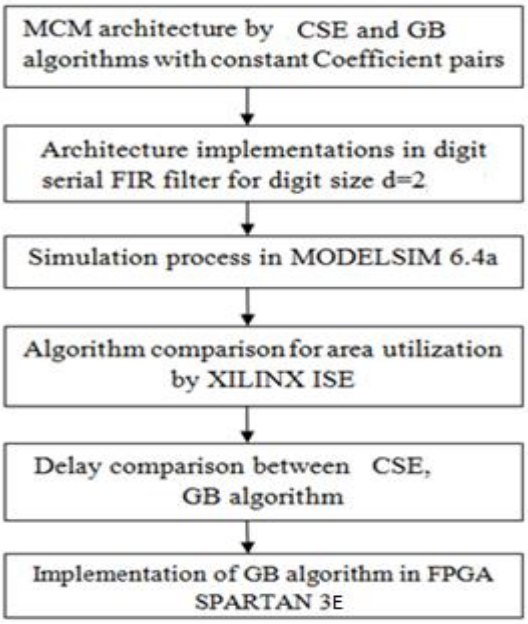


Figure 4: Flow Chart For Proposed System Design

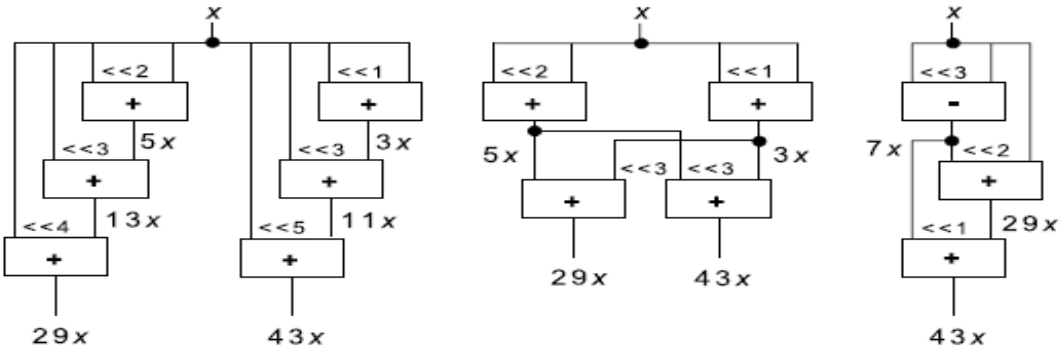


Figure 5: Shift-add's implementation of 29x and 43x (a) Without partial product sharing and with partial product sharing (b) Exact CSE algorithm (c) Exact GB algorithm

Simulation Results

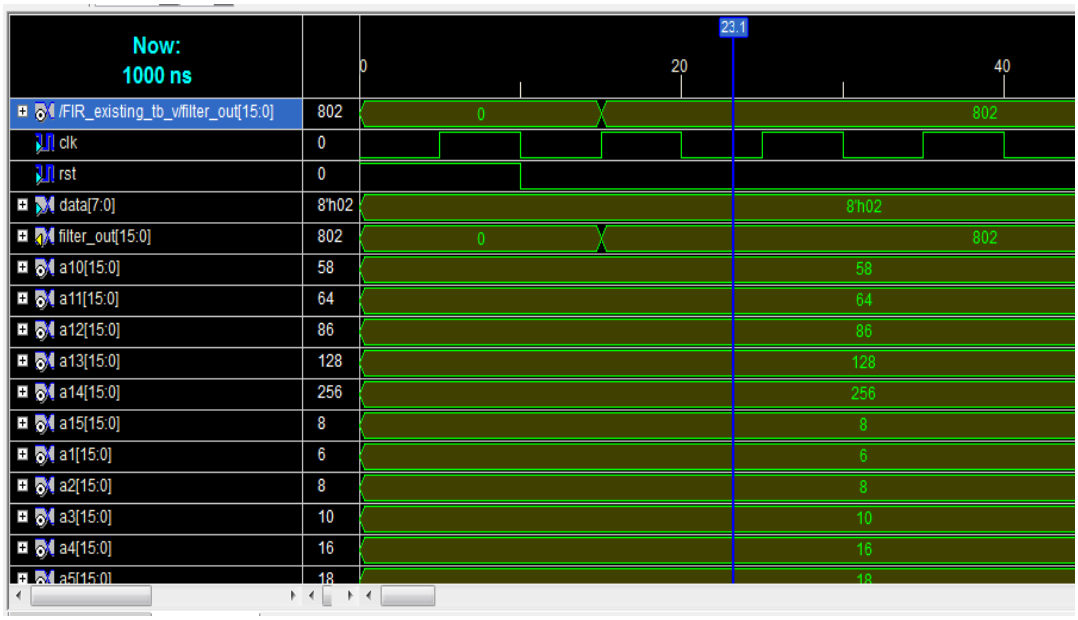


Figure 6: Output For An FIR Filter With Existing Algorithm

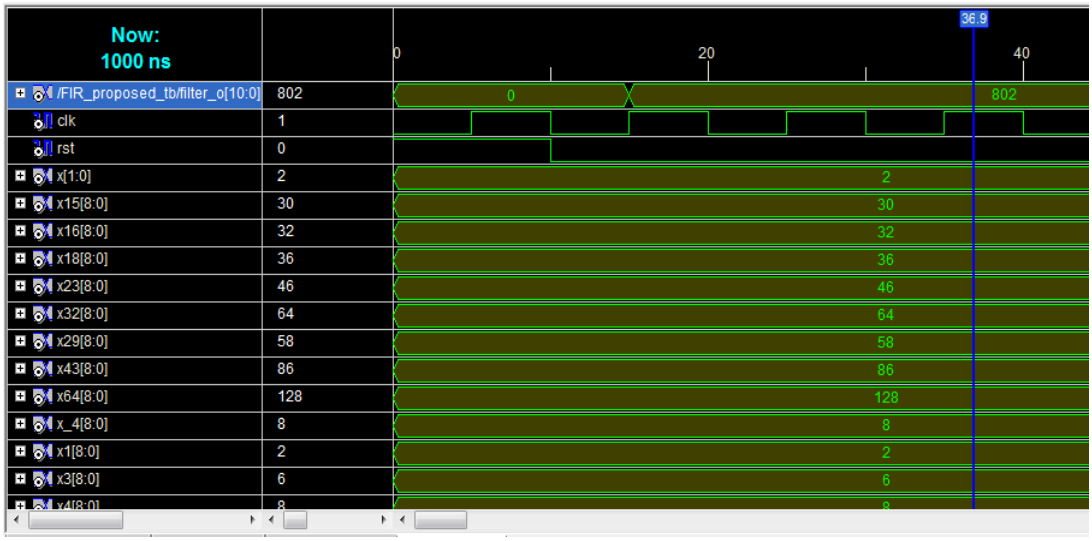


Figure 7: Output For An FIR Filter With Proposed Algorithm

Simulation results have been observed by using Modelsim simulator and synthesis results observed by XILINX ISE tool.

FIR_EXISTING_X Partition Summary
No partition information was found.

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	110	2448	4%
Number of Slice Flip Flops	105	4896	2%
Number of 4 input LUTs	161	4896	3%
Number of bonded IOBs	26	108	24%
Number of MULT18X18SIOs	7	12	58%
Number of GCLKs	1	24	4%

Figure 8: Device Utilization Report of An Existing System

FIR_PROPOSED_X Partition Summary
No partition information was found.

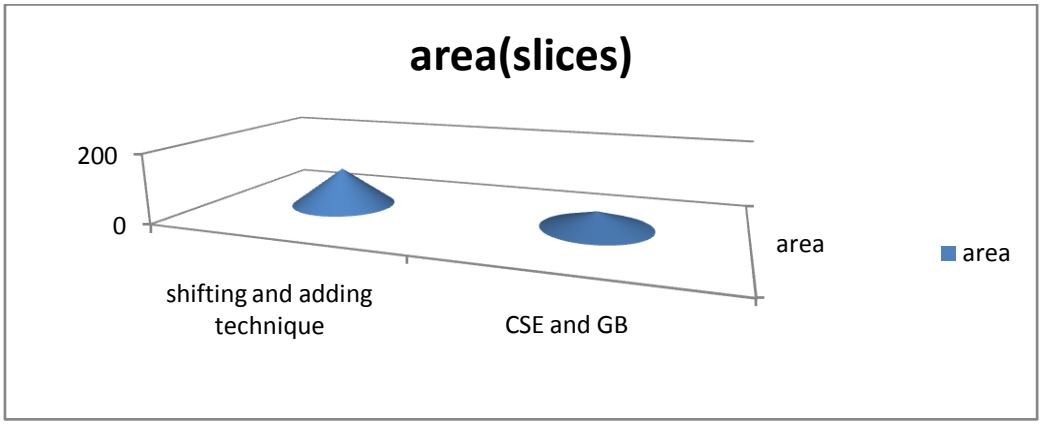
Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	47	2448	1%
Number of Slice Flip Flops	17	4896	0%
Number of 4 input LUTs	79	4896	1%
Number of bonded IOBs	14	108	12%
Number of GCLKs	1	24	4%

Figure 9: Device Utilization Report of An Proposed System

Comparion Results

Algorithm	Area(slices)
Normal multiplication	110
CSE and GB algorithm	47

Graphical representation of area reduction



Conclusion

The design of digit serial FIR filter was implemented with low complexity MCM architecture[10]. The simulation results have been observed by Modelsim simulator. Also synthesized by XILINX XST tool and implemented on SPARTAN 3E FPGA. Device utilization values of both algorithms are compared. Hence this MCM approach drastically reduces the system complexity and area. The future enhancement of this paper is to design MCM architecture with more coefficient pairs for FIR filter implementation.

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