Investigation of Independent-Gate Operation in Junctionless Devices

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Abstract

This paper investigates the possibility of Independently Driven Double Gate (IDDG) operation in junctionless devices using TCAD simulations. All the simulations are carried out at 3D level. The independent gate operation in the junctionless devices is investigated for two different gate work functions, 5.5 eV and 5.7 eV and the feasible gate voltage range is extracted. The parameters, I_{ON}, I_{OFF}, V_t and f_t are studied in the feasible gate voltage range.

Key words: IDDG, Junctionless FET, TCAD, f_t

Introduction

Short channel effects (SCE) faced in scaling of the conventional planar bulk MOSFET force us to go for quasi-planar multi-gate technology such as FinFET. Like MOSFETs these devices also rely on the source junction barrier for OFF state. The Junctionless transistor (JLT) is a new potential candidate for further device scaling and was introduced by J. P. Colinge et.al [1, 2]. Since there is no need for ultra-steep doping profile at the source and drain junctions the fabrication complexity as well as cost is reduced. SCE performance of junctionless devices is reported to be superior compared to junction-based devices [1-3]. Unlike "regular" junction-based multi gate FETs, in these devices, both the source and the drain have the same type of doping as the channel, i.e., without any pn junction. This device exploits the work function engineering of the gate electrode. The performance of dual metal gate work function in junctionless transistors has been explored [4]. Like bulk FinFET (junction-based conventional FinFET) bulk junctionless FinFET has also been investigated [5]. Nanowire junctionless transistors [6, 7], gate-all-around FET [8] etc. have also been proposed in the literature. Originally the JLT was introduced as a trigate structure [1, 2]. The effect of back bias on the electrical behavior of tri-gate JLTs has been investigated and results show that JLT devices are more sensitive to back biasing due

to the bulk conduction [9]. The conventional junction-based double gate FinFET structure could be simultaneously driven or independently driven. In the former it is known as simultaneously driven double gate (SDDG) and in the latter case it is known as independently driven double gate (IDDG). The usage of IDDG device has been demonstrated in [10] where the authors used the two gates of IDDG FinFET independently to realize mixer operation. RF characteristics of the conventional junction-based IDDG device have been studied in detail in [11].

To the best of our knowledge the IDDG mode in junctionless device has not been studied so far. In our work, we have used TCAD simulations to investigate the performance of independently driven double gate junctionless transistor (IDDG-JLT). Simulation results depict that using one of the gates as control gate the parameters, I_{ON}, I_{OFF}, V_t and f_t can be varied. The rest of the paper is organized as follows: Section 2 talks about the simulation methodology. Section 3 discusses the simulation results and finally section 4 provides the conclusion of the study.

TCAD Simulator and Device Calibration

Sentaurus TCAD simulator from Synopsys is used, which has many facilities and modules used in our simulation are: Sentaurus Structure Editor (SDE) is used to create device structure, Sentaurus Device Simulator (SDEVICE) is used to perform DC and AC simulations, Inspect and SVisual are used to view the results [12].
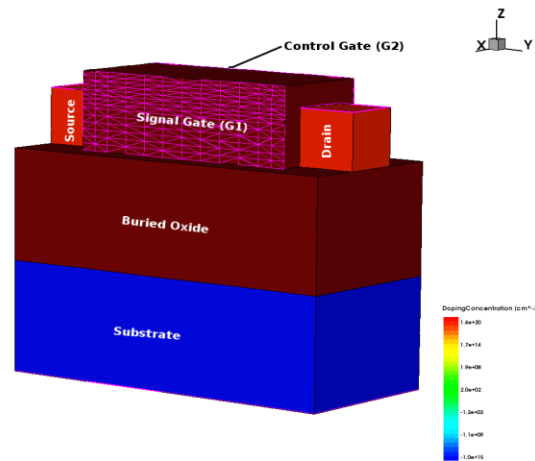

Figure 1: 3-D Structure of IDDG-Junctionless FET

Figure 1 shows the simulated 3-D structure of the Junctionless FET. The simulator is calibrated against the published results on Junctionless FETs [13], where the gate electrode work function was 5.5 eV. Device simulator (SDEVICE) includes the appropriate models for quantization of inversion layer charge, doping dependency of mobility, effect of high and normal electric fields on mobility, and velocity saturation.

Table 1: Device Dimensions and Dopings

Process Parameters	Values
Gate length (L_g)	20 nm
Fin width (W)	5 nm
Source width (SW)	5 nm
Source length (SL)	5 nm
Gate oxide thickness (T_{ox1}, T_{ox2})	2 nm
Channel doping (N_{ch})	8e19 cm^{-3}
Source/drain doping (N_{sd})	8e19 cm^{-3}
Gate electrode work function (WF)	5.5/5.7 eV

Table 1 gives the various device dimensions and doping values. As already stated, in Fig. 1 both the gates can be biased simultaneously (SDDG) or independently (IDDG). The calibrated device was modified into IDDG device, so the gates (G1 and G2) can be biased independently. The 2-D cross-sectional view of IDDG device is given in Fig. 2. An I_D–V_G characteristic of NMOS device in SDDG mode and in IDDG mode is shown in Figs. 3 and 4 respectively.
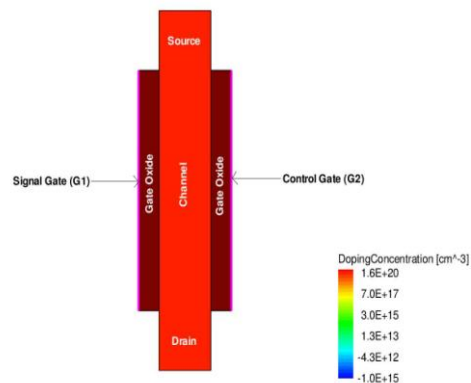
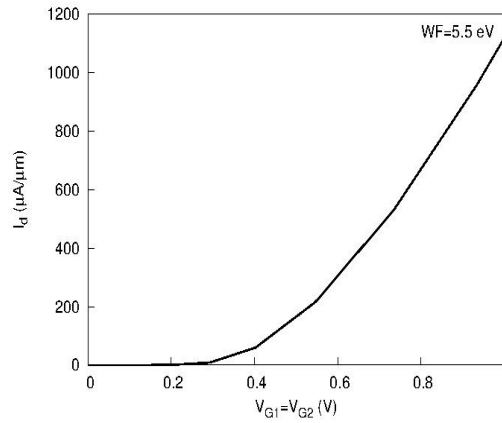**Figure 2:** 2D cross sectional view of IDDG-Junctionless FET

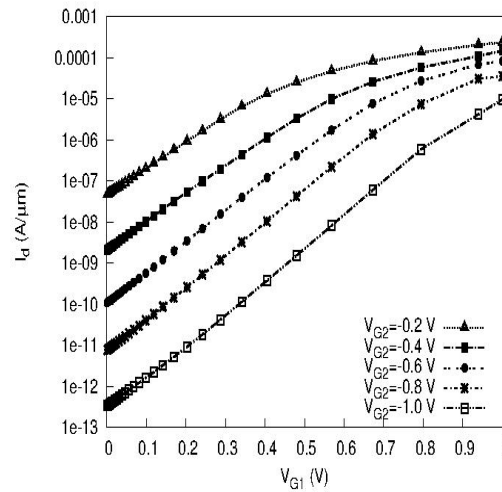**Figure 3:** I_D-V_G Characteristics of the SDDG-Junctionless FET

Figure 4: I_D-V_G Characteristics of the IDDG-Junctionless FET (WF=5.5 eV)

Supply Voltage (V_{DD}) used in this study is 1 V. I_{ON}, I_{OFF} and V_t are extracted from the saturation I_D-V_G characteristics. From the standard AC simulation f_t is extracted when $|Y21/Y11|$ equals to one. As it strongly depends on gate bias, at various gate biases f_t is calculated and maximum of them is taken as f_t. All above extractions are done for various control gate bias while signal gate bias is fixed. The control gate voltage is varied from -0.6 V to 0.2 V for the gate electrode workfunction (WF) of 5.7 eV and -1 V to -0.2 V for WF=5.5 eV. Outside these voltage ranges either I_{ON} is too low or I_{OFF} is too high.

Results and Discussion
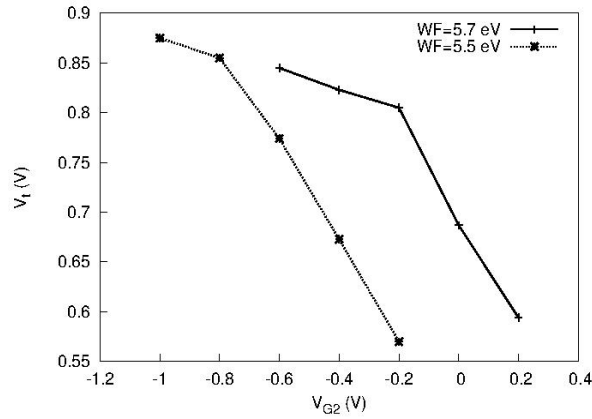Figure 5 depicts the variation of V_t with respect to control gate bias.

Figure 5: Threshold voltage (V_t) versus control gate bias (V_{G2})

V_t extraction is done through peak g_m method. It can be observed from Fig. 5 that V_t decreases monotonically with respect to V_{G2}.
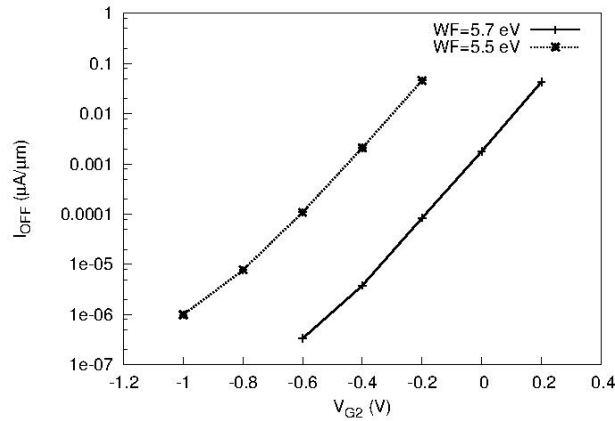

Figure 6: OFF-State drain current (I_{OFF}) versus control gate bias (V_{G2})

In the conventional i.e Inversion mode IDDG, the expression for change in V_t with respect to other gate voltage is given by the following expression [14],

$$\frac{\Delta Vt_{G1}}{\Delta V_{G2}} \approx -\frac{3T_{ox1}}{3T_{ox2} + Fin_{Width}} \qquad (1)$$

The above model predicts a linear decrease of V_t with respect to V_{G2} with a slope of -0.54, for the t_{ox1}, t_{ox2} and Fin_{width} values given in Table 1. The model fits well with extracted V_t for the V_{G2} range of -0.8 V to -0.2 V and -0.2 V to 0.2 V for the gate work function of 5.5 eV and 5.7 eV respectively.
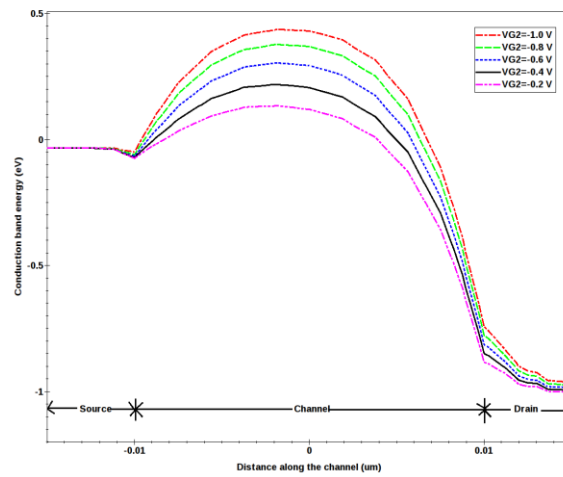
Figure 7: Conduction Band diagram of IDDG-Junctionless FET along the channel with respect to control gate bias at $V_{G1} = 0V$ and $V_{DD} = 1V$ (WF=5.5 eV)
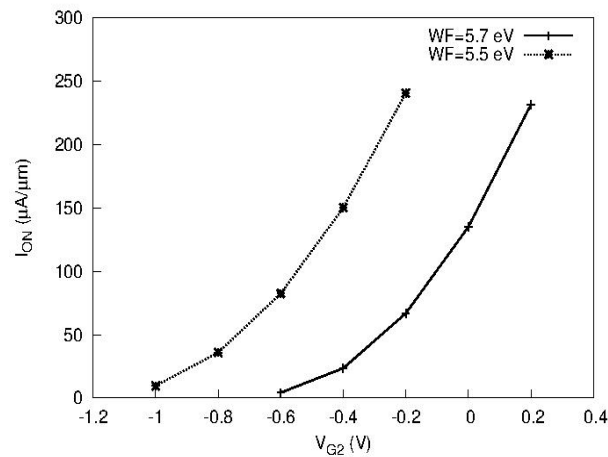

Figure 8: ON-State drain current (I_{ON}) versus control gate bias (V_{G2})

Figure 6 shows the I_{OFF} as a function of V_{G2}. Since, I_{OFF} shows the exponential dependence with V_t, I_{OFF} is plotted in log scale in Fig. 6. Figure 7 shows the conduction band energy profile along the channel for various control gate bias voltages, with $V_{G1}=0$ V and $V_{DD}=1$ V. Since the barrier height reduces with the increase in control gate bias, I_{OFF} increases. Figure 8 depicts the variation of I_{ON} with respect to control gate bias. Similar to I_{OFF} trend I_{ON} increases with V_{G2}. Various combinations of V_{G1} and V_{G2} for achieving the same ON currents of 10 µA and 100 µA are plotted in Fig. 9.
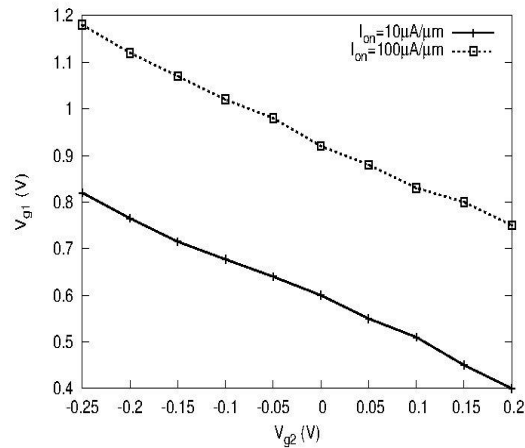
Figure 9: Various combinations of V_{G1} and V_{G2} that results in same I_{ON} of 10 µA and 100 µA (WF=5.7 eV)
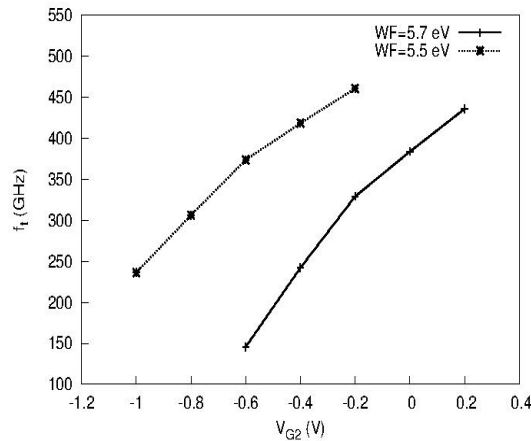

Figure 10: Unity gain cut-off frequency (f_t) versus control gate bias (V_{G2})

Figure 10 gives the unity gain frequency (f_t) versus control gate bias (V_{G2}). It is observed that f_t increases with respect to V_{G2}. This behaviour is the expected one as the parasitic series resistance decreases with the V_{G2}, which improves g_m and thereby f_t. It was observed in the simulations that the change in C_{GG} was not significant.

Conclusion

In this work, Independent gate operation was investigated in Junctionless FinFET using 3D-TCAD simulations, for two different gate electrode work functions. Feasible gate voltage range was extracted and the parameters such as ON current, OFF current, threshold voltage and f_t, were studied. It was observed that all the above parameters can be tuned using the second gate/control gate bias. It was found that the maximum

control gate voltage is -0.2 V and 0.2 V for the gate work function of 5.5 eV and 5.7 eV respectively.

Acknowledgement

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