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An Efficient 16-Bit Carry Select Adder With Optimized Power and Delay

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Abstract

Design of electronic devices is very important to reduce power, delay and area of components because these factors are impact the quality and performance of devices. Adder is most fundamental and important device in microprocessors and DSP chips Carry Select Adder (CSA) is the finest adder of choice while considering the need for high speed arithmetic designs. Previous architectures i.e., Conventional CSA and Binary to Excess-1 Converter (BEC) based Square Root Carry Selected Adder (SQRT-CSA) clearly explained. The redundancies in logic operations and dependencies of data factors are effects the power, area and delay in any adder design. The analysis of BEC-based SQRT-CSA (BEC SQRT-CSA) clearly shows the possibility to reduce the power and area by proper modifications at gate-level architecture because this design has been effected by above factors. This work reduces the redundancy in logic operations by introducing a new adder instead of the conventional BEC. The proposed design generates the sum and carry signals for both carry input signals (C_{in} =0 and C_{in} =1) for n-number of bits using n-number of new adder. The proposed new adder implemented with less number of logic gates compared with Half Adder (HA). the proposed CSA has less power consumption of 1.5%,44.21%,54.77%, and low area of 6.2%,21.2%,31.4% for 4,8,16-bit respectively compared to BEC SQRT-CSA.

Keywords: CSA; BEC; BEC-SQRT CSA; Half adder; Full adder.

Introduction

Electronics is one of the major technology domain to achieve many successes in the universe. As per today's technology, billions of electronic components has been consuming a lot of power and that power nearly equals to the power delivered by one nuclear power plant [1]. In digital electronic systems, the scope of less area and fastness requirement keeps increasing since Large Scale Integration (LSI) technology was introduced. For any digital device

The performance merely depends on power, area and delay characteristics. So VLSI technology has been concentrating more on these three factors while designing any high performance digital subsystems [1], [2].

Addition is the most fundamental and key operation in subtraction and multiplication. Addition is repeatedly required in arithmetic units such as multipliers, Finite Impulse Response and Infinite Impulse Response filters. Adder is the most important block in DSP designs and Arithmetic Logic Units (ALU) [3].So the necessity of addition operation is very high as compared with subtraction and multiplication. In adders, HA, FA and Ripple Carry Adder (RCA) are simple and basic adders, and they are used to implement various types of adders such as Carry Select Adder (CSA), Carry Skip Adder (CSKP), etc. [2].

In 1958, as the first attempt to enhance the propagation speed of carry, Carry Look Ahead (CLA) scheme was introduced by Weinberger and Smith [4]. The speed of operation depends on the bit width of operands. After that CSKP was introduced and it succeeded in speed but both schemes are necessary to maintain less area, low power and appropriate speed so as to get a high performance system. This was achieved by CSA, which was introduced by Bedrij in 1962 [5]. In adders, CSA is faster and less complex while considering the addition of two numbers with large number of bits.

Literature Survey

A basic CSA implemented with two RCA adders generates sums and carries for dual carry-inputs. In this adder, carry bit has to propagate through every FA in RCA [3]. Comparing with RCA, the propagation delay to generate final sum and carry is low for CSA, still it is not good at quality performance because of two RCA designs. This drawback was improved by the CSA design [6]. In this design one RCA is replaced with add-one logic circuit, which has been implemented by multiplexer (MUX). This CSA design is very good at short range of bits [7]. The first SQRT-CSA has been designed using two parallel RCA architecture with balanced delay even if it increases circuit complexity. After that a simple SQRT-CSA was designed to get wide range of addition operations by Y.He et al [8]. This design has less delay even when operated on wide range of bits. SQRT-CSA is non-linear, which has been implemented by cascading adders and the concentration is more on delay of the design. This design still requires to achieve less area and low power consumption so as to accomplish high performance. To achieve high performance a modified SQRT-CSA was suggested by Ram Kumar and Kittur, that is BEC-SQRT CSA [9]. This design succeeded in low power and area compared with conventional SQRT-CSA but delay increased by 5%. From the analysis of previous works, the power and area are

depending upon the redundancy in logical operations and delay depends upon dependency of the data in the design. In the BEC-SQRT CSA still redundancy problem exit. This has been overcome by proposed architecture to enhance the system performance.

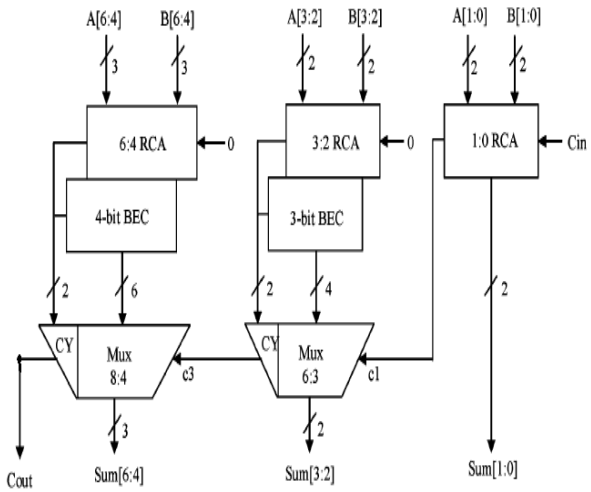

Figure 1: 7-bit BEC-SQRT CSA

A. BEC-SQRT CSA

In the RCA-SQRT CSA, two RCA blocks were utilized to generate the sum and carry for Cin=0 and Cin=1. This was modified in BEC-SQRT CSA by replacing the RCA block with BEC for Cin=1.

Fig.1 represents the block diagram of the 7-bit BEC based SQRT CSA. In this design the RCA block generates the sum and carry with input carry as logic 0. The generated sum and carry in turn drives BEC circuitry and generates another set of sum and carry, which is equal to the sum and carry generated by RCA with input carry as logic 1. The BEC circuit is shown in Fig. 2 and it is designed using related BEC Boolean expressions having 4-bit inputs (X0, X1, X2, and X3) and is implemented using AND, XOR and NOT gates.

$$Y0 = not(X0)$$

$$Y1 = (X0)\ xor\ (X1)$$

$$Y2 = (X2)\ xor\ (X1 and X0)$$

$$Y3 = (X3)\ xor\ (X2 and X1 and X0)$$

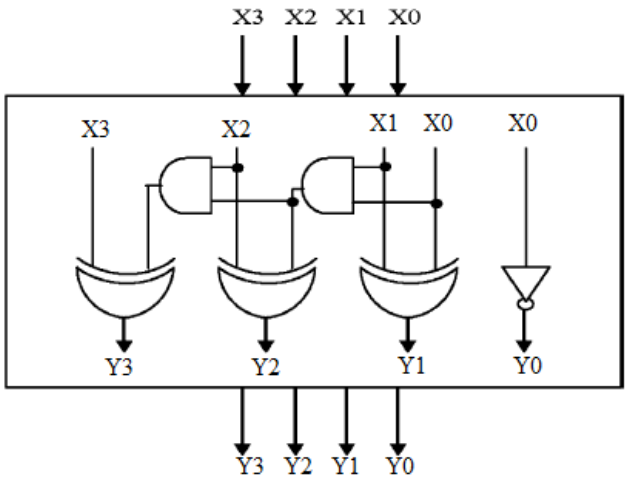

Figure 2: 4-bit BEC Circuit

The main design in this architecture is BEC circuit, which performs the operation of RCA with Cin=1. This design curtails power and area utilization when compared to RCA-SQRT CSA. So far the circuit has generated two sets (for Cin=0 and Cin=1) of sum and carry. The multiplexer is used to select one set of sum and carry based on the carry output from the previous stage. This operation is explained with the help of internal circuit diagrams shown in Fig.3 (a) and Fig.3 (b).

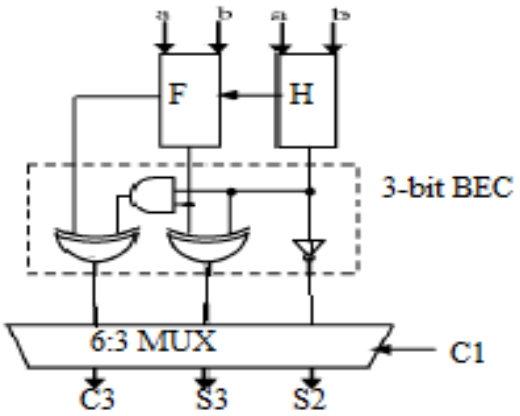

Figure 3 (a): 2-bit sum generator in SQRT-CSA

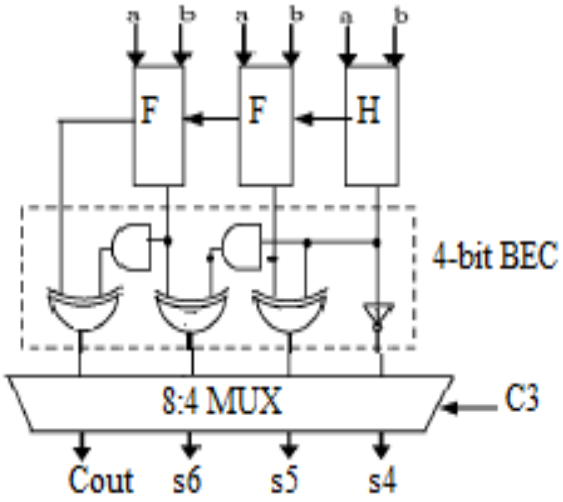

Figure 3 (b): 4-bit sum generator in SQRT-CSA

Proposed Design and Impementation

To achieve low power and low area, the BEC based SQRT CSA is modified by replacing the RCA and BEC blocks with a simple new adder block and this generates the sum and carry signals for Cin=0 and Cin=1.

The proposed design Boolean expressions (from (3) to (6)) are derived from the basic full adder (FA) logic expressions ((1) and (2)) [10]. The corresponding equations are given as follows.

$$S = AxorBxorCin \tag{1}$$

$$C = ABor(AxorB\,\overline{Cin}) \tag{2}$$

Where S, C are output sum and carry signals and Cin is input carry signal in FA.

When Cin =1,

$$S = S^1 = not(AxorB) \tag{3}$$

$$C = C^1 = AorB \tag{4}$$

When Cin =0,

$$S = S^0 = AxorB = not(S^1) \tag{5}$$

$$C = C^0 = AandB \tag{6}$$

The proposed new Adder circuit has been implemented using equations (from (3) to (6)) as shown in Fig.4. A MUX is used to select one set of sum and carry depending on the carry output from the previous stage as shown in Fig.5.

In the proposed design, sum and carry of generated by addition of least significant bits (LSB) is generated using HA and the newly proposed adder generates the sum

(S^1, S^0) and carry (C^1, C^0) for the remaining bits positions as shown in Fig.4. The final sum and carry of each bit is selected by multiplexer block by using the previous bit carry output signal as the select line as shown in Fig.6.

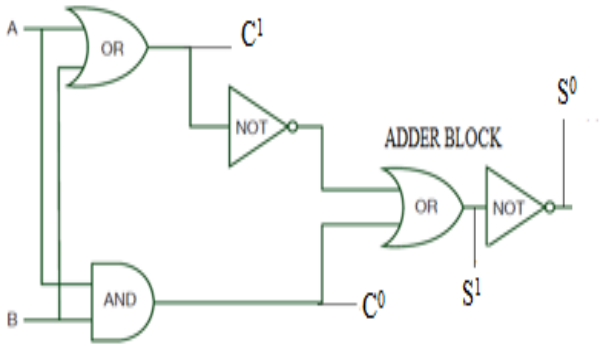

Figure 4: Proposed Adder

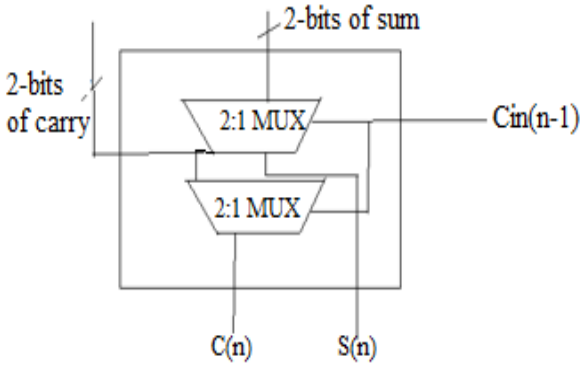

Figure 5: Multiplexer Block

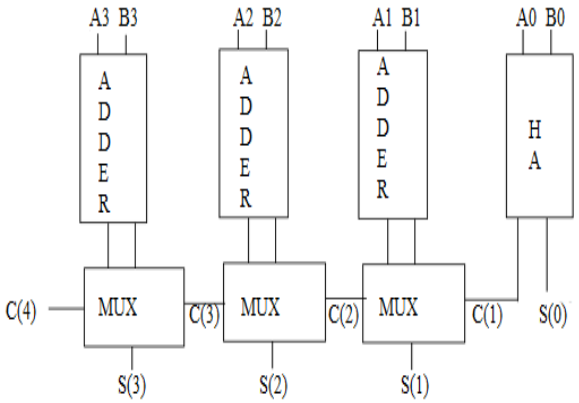

Figure 6: 4-bit proposed CSA

Results and Discussion

The proposed CSA and BEC-SQRT CSA are simulated using Synopsys 90nm library Design Compiler (DC) with same specifications of basic logic gates. The simulation results of power, area and delay are noted in Table-1, Table-2 and Table-3 respectively.

Table 1: Power Comparison

Width (n)	**Total Power (µw)**	
	Proposed CSA	***BEC-CSA***
4-bit	52.8034	53.6089
8-bit	83.0332	148.8525
16-bit	167.95	371.3960

Table 2: Area Comparison

Width (n)	**Total Area (μm^2)**	
	Proposed CSA	***BEC-CSA***
4-bit	187.6	200
8-bit	400.1	507.8
16-bit	808.6	1178.8

Table 3: Data Arrival Time

Width (n)	**DAT (ns)**	
	Proposed CSA	***BEC-CSA***
4-bit	0.57	0.76
8-bit	1.36	1.20
16-bit	2.63	1.52

The proposed CSA improved the power consumption efficiency compared to BEC-SQRT CSA. The 4-bit, 8-bit and 16-bit CSA designed using proposed architecture consumed power 1.5%, 44.21% and 54.77% respectively, less than the BEC SQRT-CSA. Compared to BEC-SQRT CSA, area of proposed design is found to get reduced by 6.2%, 21.2% and 31.4% for 4-bit, 8-bit and 16-bit respectively. Hence the overall performance has been improved by the proposed CSA, but with small cost of delay. But the effect of increased delay on performance is negligible while considering the reduction in power and area achieved by implementing the proposed CSA.

Conclusion

The proposed adder design has achieved significant improvement in area and power with small increased cost in terms of delay. It can be applied to digital signal processing and MAC units. These analysis are helpful to find out the impact of redundancy in logic operation on CSA. The new adder block has been implemented with less number of gates compared to HA and it generates sum and carry signals for carry inputs logic 0 and logic 1. Our future work will focus on data dependency to reduce the delay.

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