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Content Addressable Memory of Reordering Overlapped Mechanism With Efficient Power In Asynchronous Transfer Mode

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Abstract

Content addressable memory (CAM) is a memory unit that performs single clock cycle content matching instead of an address. CAMs are vastly used in network routers and cache controllers, as basics look-up table function is performed over all the stored memory information with high power dissipation. There is a trade-off between power consumption, area used and speed. A robust, low power and soaring speed sensing amplifier are requisite after memory design. In this paper, a parity bit is used to reduce the peak and average power consumption and enhance the robustness of the design against process variation. Thus, proposed method is a reordering overlapped mechanism used to reduce power consumption. In this mechanism, the word circuit is split into two sections that are searched sequentially. The main CAM challenges are to reduce power consumption associated with large amount of parallel process, exclusive of sacrificing speed or memory density.

Keywords: CAM, Parity CAM, Match lines, ATM Controller, reordering overlapped search mechanism.

Introduction

Content addressable memory (CAM) is the hardware search process that will boost up compared to other algorithmic approaches for searching function. CAMs composed of conventional semiconductor memory static RAM with added number of circuitry to verify that enables a search operation to complete with a one clock cycle.

A CAM is a type of memory which is implemented using the single clock of the lookup-table function in a cycle that contrast circuitry. CAM is a different type of memory, but they are special and popular for packet forwarding and packet classification in communication network path routers. They are usage is very frequent in a number of applications that requires a high speed lookup. The main purpose of

CAM-design challenges are to reduce power consumption and to reduce delay associated with the large number of parallel circuitry running, speed is not changed with memory content. At the processing terms, three methods are used for reducing the power consumption.

ATM is a packet-oriented transfer mode. The logical connections are multiplexed over a single terminal towards a physical interface. Cells flow information on each path of connection that is to be organized into finite-size of packets. Frames relay controls the link-by-link error control and flow control. The two classes of ATM net devices are switch and end point and are combined to form terminal points. The cells are input to the switching function from an ATM endpoint and switch. The Switch reads the input data and also updates the information in the cell header. And switch the cell toward its destination for interfacing. ATM switch is to ease the cell to be received across a link on a known VCI/VPI identity value. The lookup tables are used in the local translation identity values to determine the outgoing port of the connection and the new VPI/VCI value of the connection determine link. The cells are switched to the outgoing link by the transmission of data with the appropriate connection identifiers.

Existing Methods

Three architectures are proposed for reducing power, namely bank selection, pre-computation and dense coding. The results are measured are in terms of power savings of the proposed sensing scheme in paper [1]. Additionally, the CAM includes a pipelined search-line architecture which CAM power is reduced of the SL portion of [2].A pipeline approach is a general solution for high throughput [4]. The power saving of the pipelined match lines as a result of activating only a small portion of the LSLs [3]. This paper presents allocation less power to match decisions match line sensing scheme involving a large number of disparity of bits. Since large number of CAM words are disparity, this scheme results in a significant power of CAM is reduction [5]. In the match-line architecture, the match line in each TCAM partitioned the words into number of segments and are selectively pre-charged to reduce the match line power consumption [6].The array in memory and priority encoder are powered by a supply with high and low voltage. A self power-off ML sensing amplifier is employed to the top to reduce the voltage swing on the ML buses [7]. The proposed design consists of a new matching technique that uses coding to increase the appropriate distance between the words, in the conjunction MLSA with a modified match line sensing scheme paper [8]. Pipelined architecture is built as inherent accumulation, utilizing the data locally in Internet interchange. The number of memory accesses which supply the majority of power consumption, is reduced. No external cache is required. Second, as a substitute of using a global clock, different pipeline stages are driven by unique clocks [10]. The limited clocking scheme is designed carefully that reduces the traffic rate variation and improved performance. Unnecessary memory accesses are restricted by fine-grained memory scheme that preserving the packet order [9]. Packet forwarding and packet classification in network routers [11]. To improve the throughput NAND type word circuitry, some

techniques at circuitry level has been proposed [12]. In this paper, a reordered overlapped search mechanism for a high-throughput, low energy CAM. The report also includes an earlier version of this mechanism in paper [13] and this work is the extension. It includes two new approaches: a reordered word-overlapped process (RWOS) at the scheduling level and phase – overlapped processing (POP) at the circuit level [14]. At the circuit level, the pop scheme is proposed in order to fully take full advantage of the RWOS scheme for further throughput [15]. The CAM word circuit is designed based on dynamic logic that contains evaluate and pre charged phases that reduces the area. In proposing POP scheme, each word circuit is designed using asynchronous circuits [16].

Proposed Method

A. Parity Cam

CAM is frequently used in a lookup tables, networking, databases and associative computing type of applications. That requires high-speed search due parallel comparison technique performance is improved by using to diminish seek the time. Although the parallel comparison to abridged search time, in which power consumption is significantly increases. Analysing the Block-XOR approach in this paper which also improves efficiency of low power pre computation-based CAM. The major work contribution of this paper is based on realistic approach without the need for a special CAM cell design of our proposed reordering mechanism system can achieve greater power reduction.

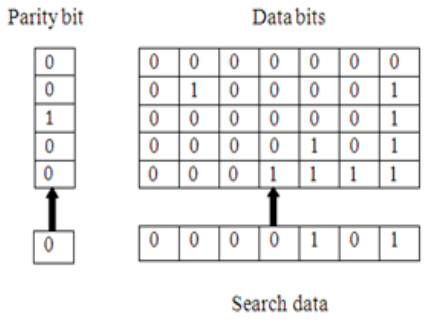

Figure 3.1: Parity bit approach

B. Reordering Overlapped Search Mechanism

An overlapped search mechanism that eases restriction to improve the throughput of a CAM. It contains two approaches: a word – overlapped search (WOS) and phase – overlapped processing (POP). The overlapped search mechanism can be realized in hardware using synchronous circuits and asynchronous circuit. This can be applied to both binary CAM and Ternary CAM, but here applied to binary CAM. In this proposed method, input words are searched from the Least Significant Bit (LSB). The

1st-stage segment stores the last *K* bits of words and the 2nd -stage segment stores the first (*n-k)* bits of words.

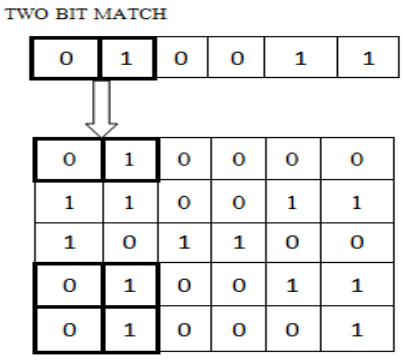

Figure 3.2: Reorder Overlapped Mechanism

Fig.3.3 Shows the block diagram of the input controller when m is set to value. It includes registers, a mode controller and comparator and, which operates in one of two modes: fast and slow. As search words are processed before searching them in a CAM, this method can be categorized as a pre–computation method. A search word is partitioned into the last k bits and the first (n - k) bits of the word. Consecutive last *k* bits of the current and *m* search words are compared to check whether they are the same or not. As long as these splited words are different the input controller sends search words to the CAM block at high speed.

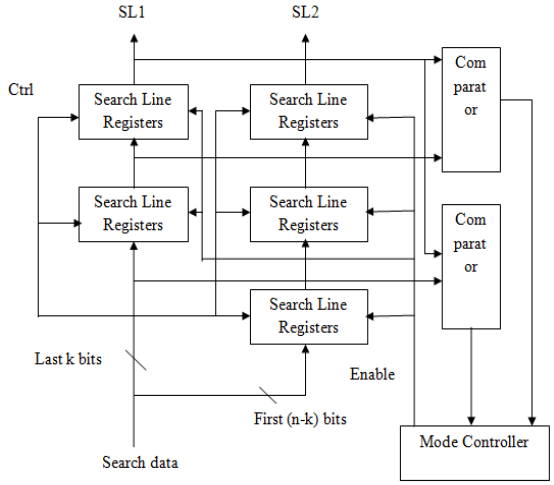

Figure 3.3: Block Diagram For Overlap Search Mechanism

C. ATM Controller

An asynchronous transfer mode (ATM) controller includes a number of buffer memory, a transfer circuit which transfers packet data between the buffer and an

internal memory of an associative terminal unit with a data block and the mode controller length predetermined therefore, a cell transmit circuit section that subdivided and they are named as "slices" . Data block sent from the terminal memory into data cells to the buffer memory which are again sent forth to the ATM network, receive control circuit get input cell operable to reconstruct the data cells received over a transfer path from ATM network forming in the buffer memory a predetermined length data block, and a transfer control circuit operable to permit the transfer circuit to transfer the predetermined length data block between the buffer memory and the terminal memory, thereby enabling accommodation of a variety of kinds of setup configurations any possible changes in ATM protocol processing as assigned to a microprocessor. Since ATM networks components as a transformation table and are connection-oriented, virtual circuit need to be set up across them prior to any data relocation. There are two kinds of ATM virtual circuits: virtual path (identified by a virtual path identifier or VPI) and channel path (identified by a channel path identifier or VCI).VCI/VPI values are localized; each segment of the total connection has unique VCI/VPI combinations. Whenever an ATM cell travels through a switch, its VPI/VCI value has to be changed into the value used for the next segment of the connection. This process is called VPI/VCI translation. Since speed is an important factor in ATM network, the speed at which this translation occurs forming a critical part of the network's overall performance.

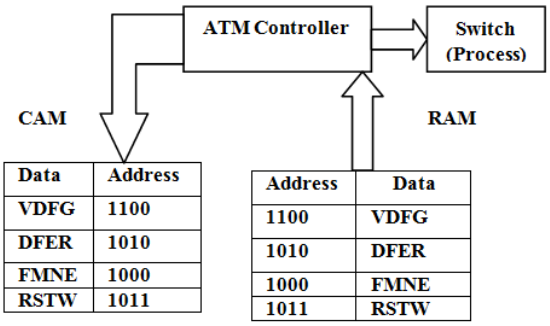

Figure 3.4: Block diagram of ATM Controller

Memory Structure

ATM functions to be operated with the parameters are required for each channel. There are address compression tables for the receiver to decide which channel any given cell relays to, connection tables for both receiver and transmitter for defining all the protocol and data routing information for each channel, pace control tables for directing the scheduling of cell to transmit, interrupt queues for both receive and transmit, and buffer descriptor and buffers for the data. Some of this parameter in RAM some in external memory.FCC buffering is an intermediate buffer to improve data throughput and where some processing is handled by the CP and the registration area is where the basic functionality of the FCC is defined.

VPI/VCI Evaluation

VPI is the virtual path identifier and can be considered like the outer case of a multi core cable. It identifies the major route of the data. VCI is a virtual path circuit identifier and can be considered like an inner core of the cable.

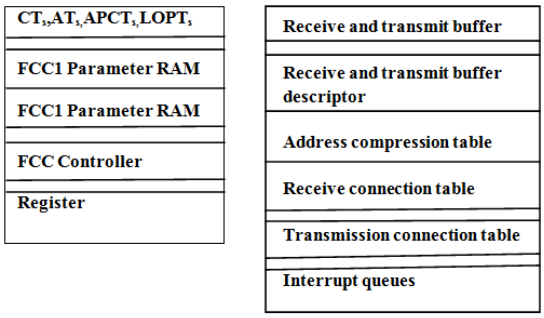

Figure 3.4.1: Memory Formation

These values are routed to the cell data at the required destination. However, the tricky concept here is that when the cell is transmitted, these values are not defining the final destination but simply the first stage routing. To find the best routing for the cell and in the cell process each node or ATM switch must set up a table for VPI/VCI values, and priority and quality of service for the transfer.

CAM can act as an address translator in an ATM switch and performs the VPI/VCI transformation very quickly. During the conversion process, the CAM takes incoming VPI/VCI values in ATM cell headers and generates addresses that access data in an external RAM (since standard CAM architecture cannot support the required capacity, a CAM/RAM combination enables the realization of multi-mega bit translation tables with fully-parallel search capability).VPI/VCI field from the ATM cell header are compared against a list of current connections stored in the CAM array. As a result of the comparison, CAM generates an address that is used to access an external RAM where VPI/VCI mapping data and other connection information is stored. The ATM controller modifies the cell header using the VPI/VCI data from the RAM and the RAM and the cell is sent to the switch.

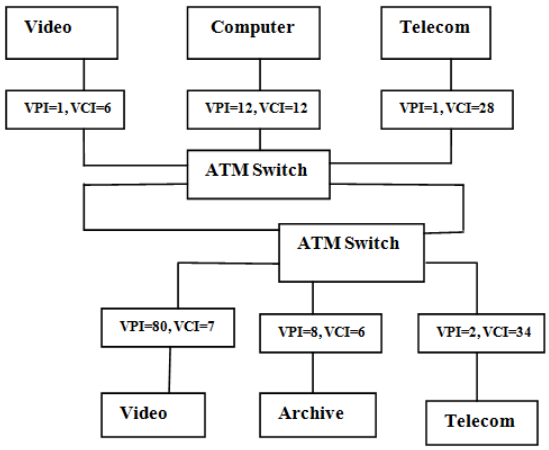

Figure 3.4.2: ATM Network VPI/VCI

D. ATM Controller With Cam

Content addressable memory is used in ATM switches, due to their connection based protocol, must translate each ATM cell address at every point along the routing path.There are two basic forms of CAM , they are binary CAMs support storage and searching of binary bits(0,1). Ternary CAMs support storing of zero, don't care and one bit.Each bit of CAM storage includes comparison logic. A data value input to the CAM is simultaneously compared with all the stored data. The input data are matched such that the result is the corresponding address of the data. A CAM operates as a data parallel processor. CAMs can be used to design Asynchronous Transfer Mode switches. The time required to compute VPI/VCI translations is critical in order to determine the performance of ATM networks. CAM can act as an address translator for look-up tables in ATM switches and perform VPI/VCI translation quickly.

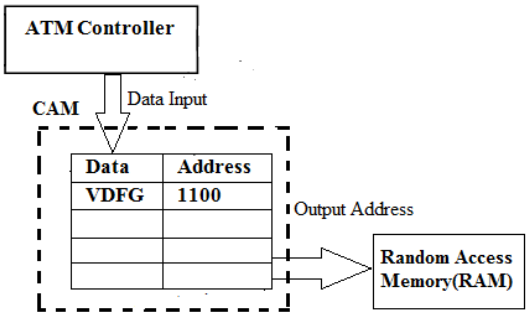

Figure 3.4.3: Content Addressable Memory with

ATM Controller Virtual path identifier and channel identifier are the data input to CAM. VPI/VCI fields from the ATM controller are compared against a list of current connections stored in the CAM array. CAM generates an address that is used to

access an embedded RAM, where VPI/VCI mapping data and other connection information are stored.

Results and Discussion

There are two parameters to be discussed are power consumption and search speed. The input data are searched in order to determine both parameters comparatively to the proposed method. Both power optimized and speed optimized designs are verified by performing the synthesis by Xilinx 9.2i version. All simulations presented this section compare ML0 against an ML1 on 144 bit CAM word.

Design Optimized For Power Consumption

For accurate comparison of the ML voltages, the initial current to all the ML must be identical, for minimum power consumption initial current must be zero and the pre charging node Fig 4.1.1, 4.1.3 and 4.1.5 shows the Xilinx simulation results. The timing summary is evaluated are shown in Fig 4.1.2, 4.1.6 and 4.1.4. Reduces the total power consumption in the system is important factor since it is desirable to maximize the run time with decreases the size, battery life and weight allocated for batteries. So the most important factor to consider while designing Silicon on Chip for portable devices is low power design.

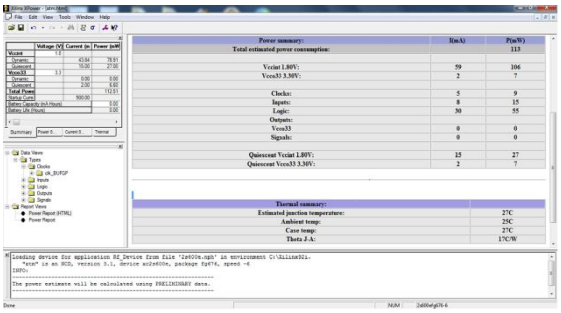

Figure 4.1.1: Power Analysis of Pre Computation

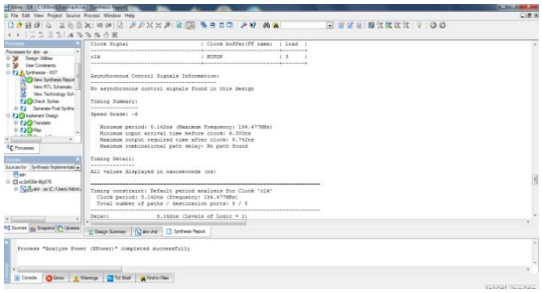

Figure 4.1.2: Timing Summary of Pre Computation

Comparison is performed by the parameters of power consumption and Timing summary with different techniques. Two types of analytical progress various types of

parameter should be analysed. In this existing method estimated power consumption 113mW at the same time temperature level 27*c. Clock pulse 69 clock. This also used parity CAM in the proposed system. Various technologies are used to find the efficient power and timing delay.

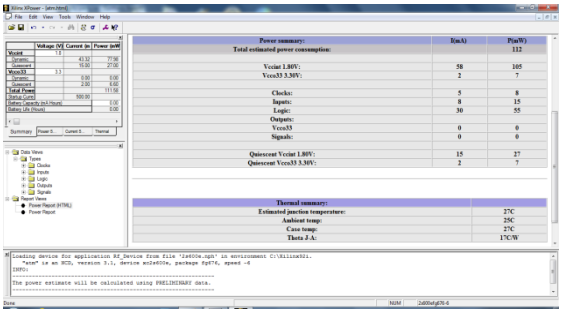

Figure 4.1.3: Power Analysis of parity bit

To compare existing and proposed system clock speed difference of maximum input arrival rate 1.373ns. But maximum output required time after clock is same. Same the power consumption is also measured for reordered search mechanism in which that entire bit streams are separated into two halves.

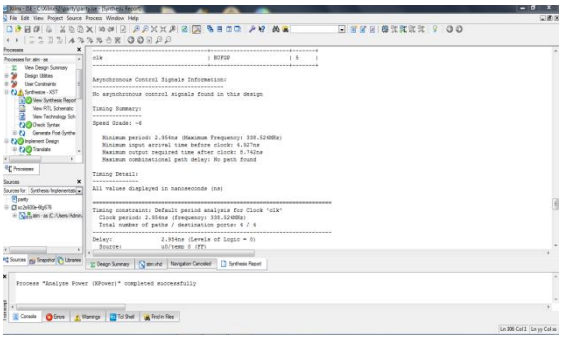

Figure 4.1.4: Timing Summary of Parity Bit

The minimum period difference between the methods is 2.466ns. The combinational paths analysed between them are same. Thus search speed plays an important role in the real time applications, which probably save the time.

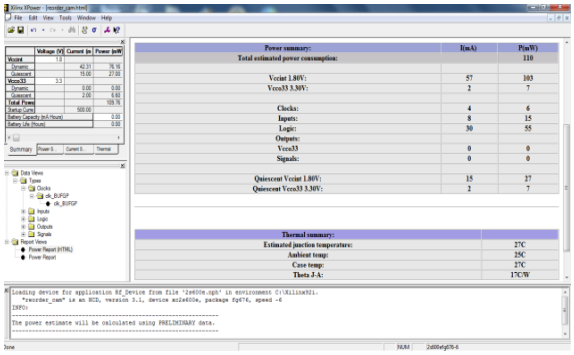

Figure 4.1.5: Power Summary of reordering method

Power varies in accordance to Vccint value in the processing methods. Thus, clock and all other terms such as signal, clock, output, logic, etc….. are similar as shown in Fig 4.1, 4.3 and 4.5. Using the Word search scheme, consecutive search words are assigned to unused different word circuits that are in an evaluate phase. Input search words can be processed with consuming the time used for pre charge time. The power consumption and timing summary of reordering mechanism is shown in Fig.4.1.5 and 4.1.6. Such that the time taken for 3.104ns which is comparatively high with other methods.

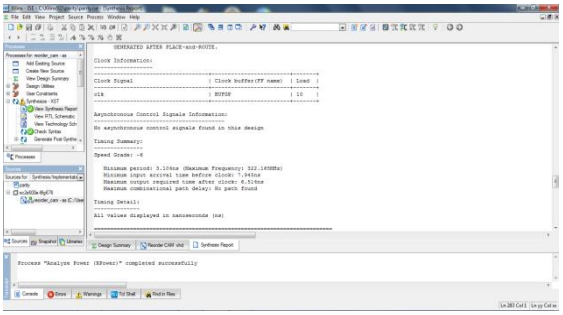

Figure 4.1.6: Timing Summary of Reordering Method

Conclusion

The proposed CAM allocated power to match decision based on the number of mismatch bit in each CAM word. There are two methods to reduce power consumption, in which parity power consumption 112mW and reorder overlapped search mechanism power consumption 110mW. When compared with existing methods which consist of 113mW, the power reduced 3mW. Thus proposed method of reorder overlapped mechanism in this paper is mainly based word overlapped search (WOS). This paper can be enhanced to phase overlapped reorder mechanism, such that the power consumption and search speed can be varied.

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