

Design and Synthesis of Radix-4 Booth Multiplier Using Gdi & Mgdi Technique

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Abstract

This paper presents a design of low power, area efficient radix 4 booth multiplier using gated diffusion input (GDI) technique and modified gated diffusion input MGDI technique. MGDI and GDI play an important role in design of low power and area efficient circuits. This has led many researchers to take GDI and MGDI technique very seriously in building important circuits related to advanced low power and area efficient CMOS design. The entire design has been performed by using backend tools it has found that there is a considerable amount of reduction in Average Power consumption (P_{avg}), delay time. In addition to this there is a significant reduction in transistor count compared to conventional CMOS technique. The simulation of the proposed design has been carried out in H- SPICE tool.

Keywords: Gate diffusion input (GDI), modified gated diffusion input (MGDI) complementary metal oxide semiconductor (CMOS), Booth multiplier, leakage current

Introductio

A. Background and Motivation

In today's electronics world processors became very important for performing multiple operations. Processors consist of adders, subtractions, multipliers etc these consume power, area and also cause delay in data transition. To reduce these parameters we introduce a new arithmetic device called gated diffusion input (GDI) technique radix- 4 booth multiplier [1] which reduces power consumption and also reduces the area.

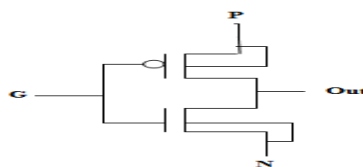
In past technology, the main concentrations of the VLSI designer were performance of the device, area required, cost and reliability of the complete system. Power dissipation was secondary issue. But in today's technology, it has been changed and power dissipation is given equal weight age to area and speed considerations. So many factors have been contributed to this trend. But the main driving factor is the remarkable success and growth of personal computing devices Such as multimedia products, portable desktops and wireless communication systems like personal communicators which need high- speed computation and complex functionality with low power consumption. In such applications, low power consumption is a critical design issue.

Power dissipation in CMOS circuits is caused by three main sources: 1) the charging and discharging of capacitive loads due to change in input logic levels. 2) the short-circuit current arises because of the direct current path between the supply rails during output transitions and 3) the leakage current which is determined by the fabrication technology, consist reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage, The short- circuit and leakage currents in CMOS circuits can be made small with proper device and circuit design techniques. The dominant source of power consumption is the charging- discharging of the node capacitances and it can be minimizing by reducing switching activity of transistors. Switching activity of the digital circuits is also a function of the logic style used to implement the circuit.

GDI & MGDI Introduction

A. Origin of GDI

First the GDI basic cell was introduced by Arkadiy Morgenshtein in 2002[4]. The basic GDI cell contains one nMOS and one pMOS transistors with four terminals: G, P, N and D. Input G is the common gate input of nMOS and pMOS transistors, input P is the outer diffusion node of pMOS transistor, input N is the outer diffusion node of MOS transistor, and output D is the common output diffusion node of both transistors. The GDI primitive cells are designed in twin-well CMOS or silicon on insulator (SOI) technologies. The following figure shows the basic GDI cell.



B. Introduction to GDI

Gate Diffusion Input (GDI) method is based on the utilization of a simple cell as shown in above Fig which can be used for low power digital circuits . This technique

is implemented in twin-well CMOS or Silicon on Insulator (SOI) technologies. In this process, the bulks of both NMOS and PMOS transistors are hardwired to their diffusions to reduce the bulk effect that is dependence of threshold voltage on source-to-bulk voltage. The dependence of transistor threshold voltage on source-to-bulk voltage is as follows

$$V_{th} = V_{th0} + \gamma \left(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|} \right) - V_{ds}$$

Where V_{SB} is source-body voltage, V_{th0} is threshold voltage at $V_{SB}=0$, γ is linearized body coefficient, Φ_F is the Fermi potential and η is Drain Induced Barrier Lowering (DIBL) coefficient. Using this procedure power consumption can be reduced along with delay time thereby delivering a reduced power delay product. Consequently area of the circuit is minimized. This analysis is based on the Shockley model in which the drain current I_D is represented as shown below

$$I_{D0} \left(\frac{W}{L} \right) e^{qV_{GS}/KT}$$

$(V_{GS} \leq V_{TH})$: *subthreshold region*

$$K \{ (V_{GS} - V_{TH}) V_{DS} - 0.5 V_{DS}^2$$

$(V_{DS} < V_{GS} - V_{TH})$: *linear region*

$$0.5K (V_{GS} - V_{TH})^2$$

$(V_{DS} \geq V_{GS} - V_{TH})$: *saturation region*

Where K denotes device trans conductance parameter, V_{TH} denotes threshold voltage, W denotes channel width and L denotes channel length.

C. Drawbacks of GDI

The basic Gate Diffusion Input (GDI) logic style suffers from some practical limitations like swing degradation, fabrication complexity in standard CMOS process and bulk connections. These limitations can be overcome by modified gate diffusion input (Mod-GDI) logic style. To overcome these drawbacks we go for MGDI technique.

D. Introduction to MGDI

This modified gate diffusion input (Mod-GDI) logic style allows reducing power consumption, delay and area of digital circuits. Fig 1 shows basic Mod-GDI cell. In contrast with the basic GDI cell, Modified-GDI [Mod-GDI] cell contains a low-voltage terminal S_P configured to be connected to a high constant voltage (i.e. supply voltage) and a high-voltage terminal S_N configured to be connected to a low constant voltage (i.e. Ground). Including terminals this ensures that the Mod-GDI cell can be implemented with all current CMOS technologies. In the Mod-GDI cell, the bulk node of PMOS transistor is connected to the high constant voltage referred to as supply voltage or V_{DD} and the bulk of NMOS transistor is connected to low constant voltage referred to as GND.

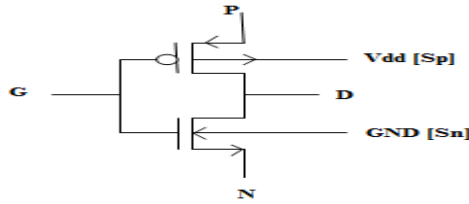


Figure 1: Modified MGDI cell

Basic GDI And MGDI Logic Gates

A. GDI & MGDI AND gate

The following figure shows the circuit diagram for GDI & MGDI AND gate

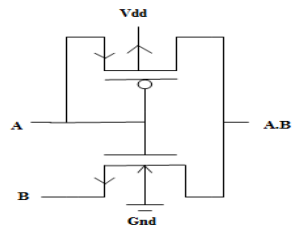


Figure 3.1: MGDI AND cell

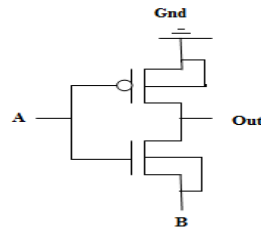


Figure 3.2: GDI AND cell

The above figure shows the design of an AND gate based on GDI & MGDI method.

B. GDI OR gate

The following figure shows the OR GDI & MGDI cell

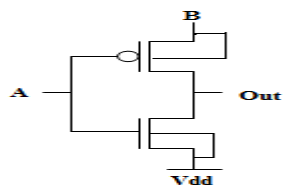


Figure 4.1: GDI OR cell

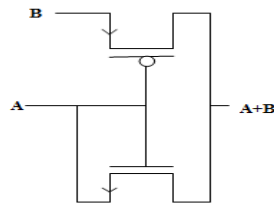


Figure 4.2: MGDI OR cell

The above figure shows the design of OR gate GDI & MGDI cell.

C. GDI & MGDI XOR gate

The following figure shows GDI & MGDI XOR gate

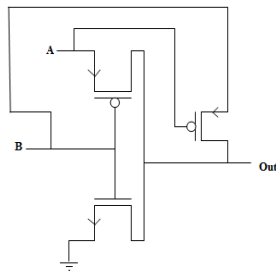


Figure 5.1: MGDI XOR cell

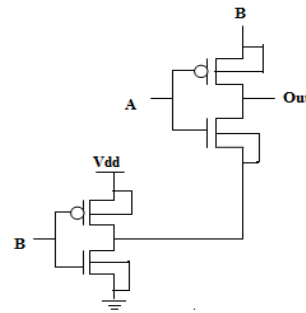


Figure 5.2: GDI XOR cell

The above figure shows the design of a XOR gate based on GDI & MGDI procedure.

Radix-4 Booth Multiplier

A. Introduction

Multiplier is one of the mostly used building blocks in the digital devices. The high performance DSP systems depend on hardware multiplication to achieve high data throughput. Digital multiplication is a series of bit shift and bit additions, where two binary numbers, the multiplier and the multiplicand are combined into the result. The entire process consists of three steps: 1) partial product generation, 2) partial product reduction and 3) final addition. There are different types of multipliers available depending upon the application in which they are used.

Basically Multiplier design consists of three operational steps: 1) encode the multiplier bit Y using Booth encoded algorithm and a partial product is produced from the multiplicand X and the encoded multiplier Y . 2) the adder array or partial product compression is used to add all partial products and then reduce them into the form of sum and carry. 3) The final addition using CSA adder or RCA adder in which the final multiplication result is generated by adding the sum and the carry. So, the important blocks in booth multipliers are decoder, partial product generator and adder to generate final result.

B.Radix-4 Encoder block diagram

The following figure shows radix-4 encoder block

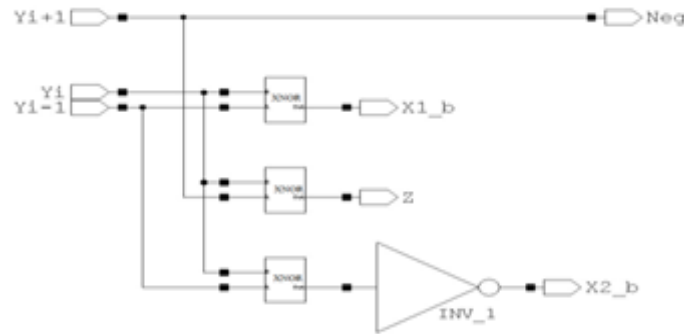


Figure 6: Radix-4 Encoder

Radix-4 multiplication obtains an improvement in the multiplication algorithm due to the less number of partial products entering the Wallace tree to be reduced [7]. This can be achieved by the application of the multiplier recoding, changing from a 2^n 's complement format to a signed-digit representation from the set $\{0, \pm 1, \pm 2\}$

Now let us assume that we are giving a triplet of multiplier one at a time in the form of Y_{i-1}, Y_i, Y_{i+1} and gets the encoded output in the form of $Neg, X1_b, X2_b, Z$. In which $X2_b$ means that the multiplicand is not to be doubled, $X1_b$ means multiplicand is to be doubled and Neg means neither to be doubled nor to be inverted.

C. Partial product generator block diagram

The following figure shows the block diagram for partial product generation

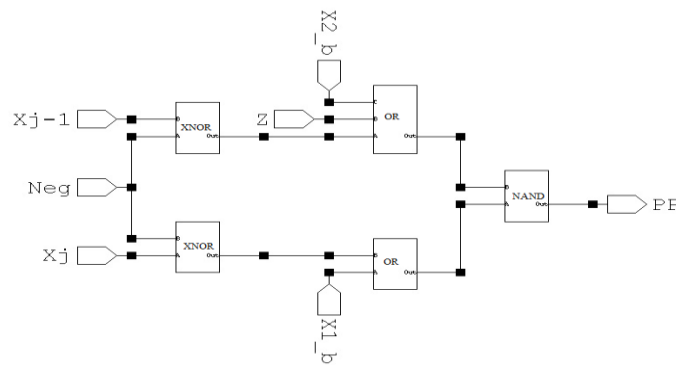


Figure 7: Partial Product Generator

In this block, multiplier bits encoded from the encoder and the multiplicand bits get multiplied and the partial products are generated. Fig. 6 shows the block diagram of 1-bit partial product generator block where the input $X1_b, X2_b, Neg, Z$ are the encoded multiplier bits from the encoder and X_j and X_{j-1} are the multiplicand bits which are to be multiplied by the multiplier bits coming from the encoder.

Simulation Results

A.H-spice simulation results for GDI & MGDI AND gates

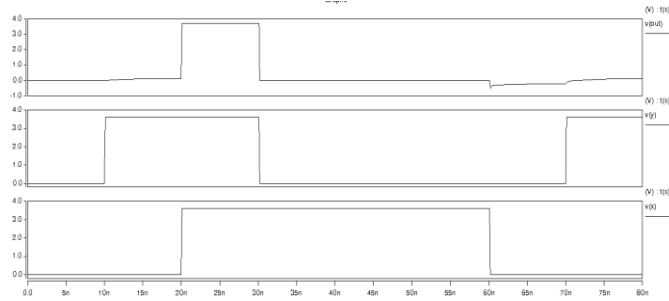


Figure 8.1: Simulation Waveform For GDI and Gate

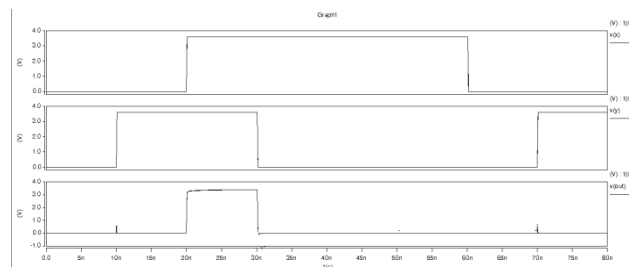


Figure 8.2: Simulation Waveform For MGDI AND Gate

B. H-spice simulation results for GDI& MGDI OR gates

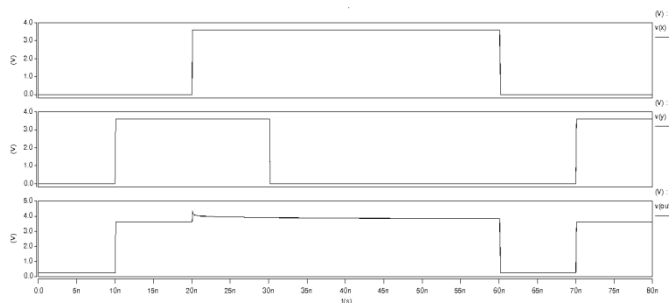


Figure 9.1: Simulation Waveform For GDI OR Gate

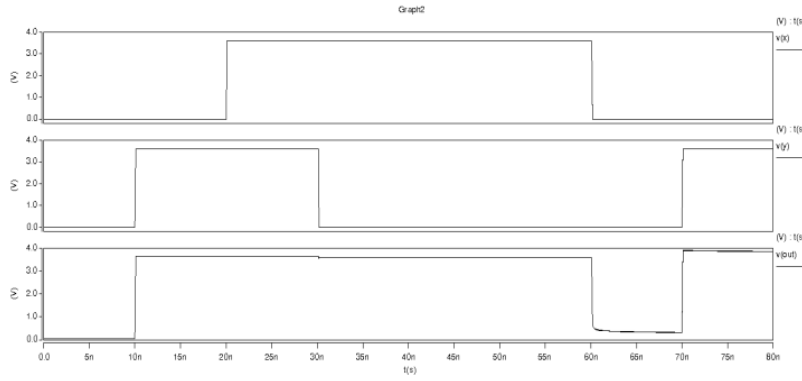


Figure 9.2: Simulation Waveform For MGDI OR Gate

C. H-spice simulation results for GDI & MGDI XOR gate

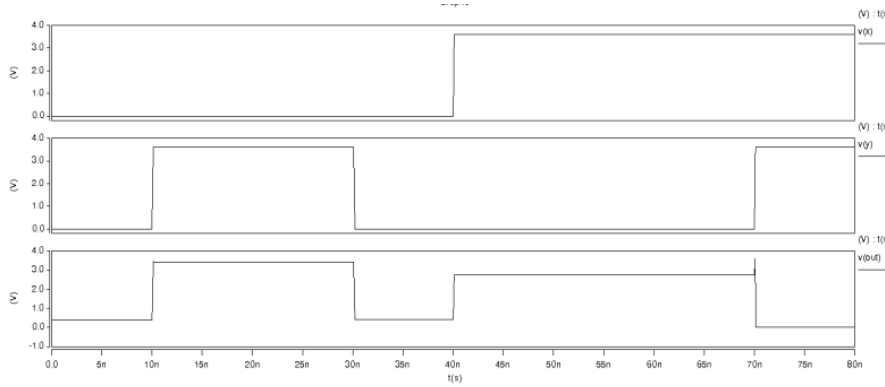


Figure 10.1: Simulation Waveform For GDI XOR Gate

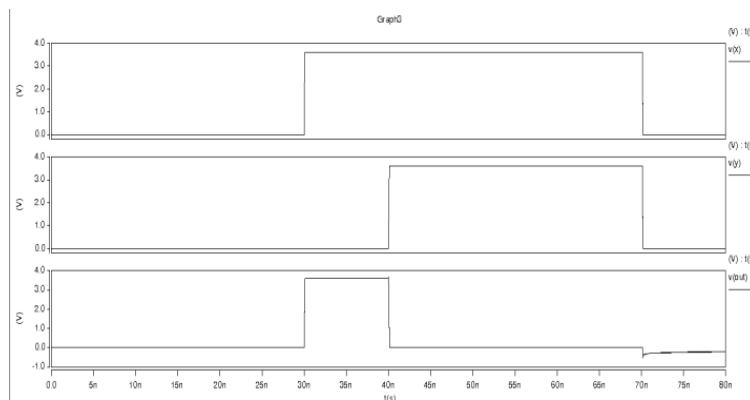


Figure 10.2: simulation waveform for MGDI XOR gate

D. H-spice simulation result for Radix-4 Booth multiplier

1) Input waveforms for MGDI booth multiplier:

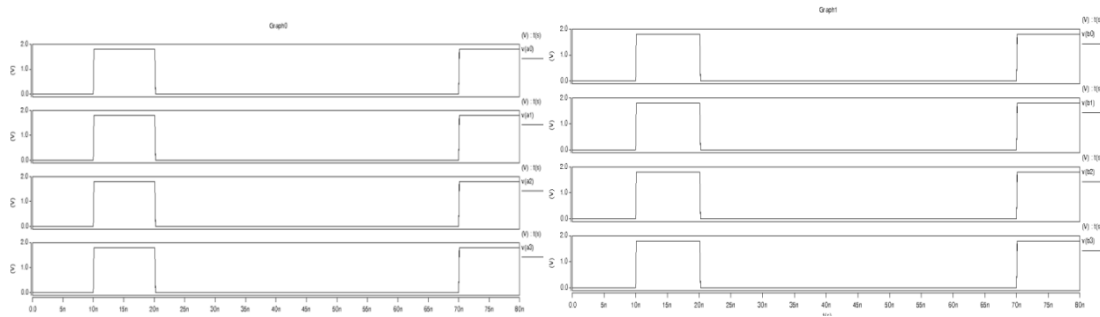


Figure 11: Input Waveforms For MGDI Booth Multiplier

2) Output waveforms for MGDI Booth multiplier:

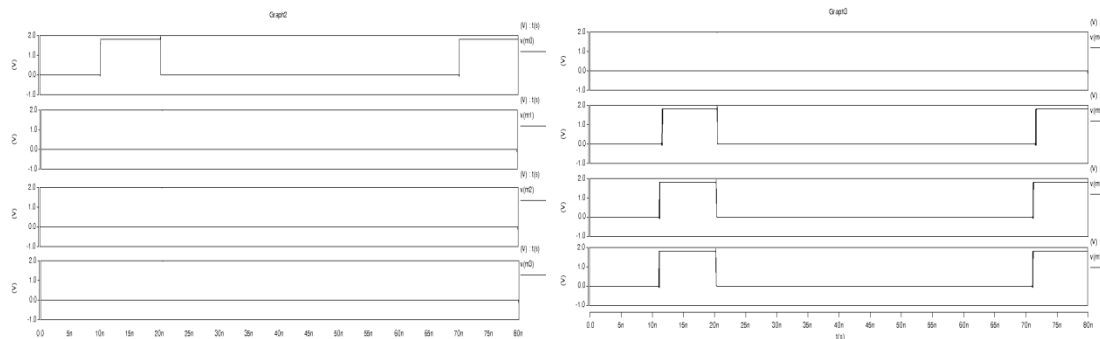


Figure 12: Output waveforms for MGDI Radix-4 booth multiplier

Gates Parameters Comparison

Table 1: Parameter Comparison

Gate type	GDI AND	MGDI AND	GDI OR	MGDI OR	GDI XOR	MGDI XOR
Delay	3.73 Pico sec	1.79 Pico Sec	30.05 nsec	30.07 nsec	5.01 nsec	1.23 nsec
Power	0.83 mw	0.67 mw	41.9 μ w	39.5 μ w	12.04 mw	7.10 mw
Transistor count	2	2	2	2	4	3

Multiplier Parameters Comparison

Table 2: Parameter Comparison

Type of Multiplier	GDI booth Multiplier	MGDI booth Multiplier
Power	18.6 mw	7.5 mw
Delay	3.75 Pico sec	3.5 Pico sec

Conclusion

This project presents a detailed study of GDI & MGDI technique and implementation of logic gates and architecture of Radix-4 Booth multiplier using GDI & MGDI technique. The simulation results reveals that there is a considerable reduction in power when compared with CMOS ,GDI & MGDI technique .The radix-4 Booth multiplier with MGDI technique gives fifty percent power reduction when compared with GDI technique and also gives high speed operation.

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