

An Improved Low Power and Modified Area Efficient Carry Select Adder – (MA-CSLA)

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Abstract

In portable systems, the density of the power has been rapidly growth and made the power dissipation as an important objective of the design. As well as in VLSI design adder is widely used components and research goal of the integrated circuit performance. Carry Select adder (CSLA) computes sum of double bits number of $n+1$ bit. In order to reduce the criteria of the existing system the architecture of the CSLA is modified the parameters of adder to provide better performances. The Modified Area Efficient CSLA observed the area reduction and low power consumption than the existing adder. In existing adder dual Ripple Carry Adder is used for the operation of adder. But in the proposed circuit Modified Area Efficient CSLA (MA-CSLA) for area and power reduction AOI is used as one of the circuit instead of existing circuit design of BEC or RCA. Moreover, subsequently the count of the total gate is reduced. The significant reduction of area and power of this work is used with efficient modification of gate-level and simple or easy manner in the circuit. Based on the CSLA bits modification in the architecture, the performances are compared and analyzed to show the better performances level than the existing. The performances are evaluated in terms of power, delay, area and their logical efforts through the CMOS process technology of the custom design in the circuit.

Keywords: SQRD-CSLA;AOI; RCA; Power Delay; Application-specific integrated circuit (ASIC);

Introduction

In VLSI industry, the components of portable electronic are rapidly growth for the circuit of low power arithmetic. The efficient design of the power and area consumption with data path high-speed systems is a research area of the design. Through the adder the speed is limited as per the time requirement for carry propagation in the digital adders. The position of each bits are generated sequentially one after another in an adder elementary and propagates a carry into the next position. Adder is used in any parts of the processor to evaluate the address of the application with table indices. Multiplier-Accumulator (MAC) unit is a significant process of the whole system and as a part of DSP processor. Hence the power and area consumption of Full Adder circuit is essential for the application of low power and for propagation delay reduction with high speed process Carry Select Adder are used. Basically it is a parallel computation and generates many partial sum and carriers and it's selected by multiplexers (mux) [9]. In integrated circuit for high speed process of digital signal processing adder is used to execute the various algorithms like FIR, IIR and FFT.

In today's digital circuitry, adder consumes the reduction of area and power in the process of data path requirement with similar speed. Adder is a widely used hardware blocks in digital signal processing (DSP) and Arithmetic and logic unit (ALU) systems. In DSP, it includes sophistication and digital filtering like digital communications and spectral analysis, Discrete Fourier transform (DFT) and Fast Fourier Transform (FFT). Based on the operation of adder the power consumption performance depends on it.

The CSLA is computational systems used to relieve the difficult of carry delay propagation by generating multiple carries then sum [1]. Carry Select Adder (CSLA) performs the function of arithmetic faster and used in data-processing processors. However, by use of RCA multiple pairs to generate sum and carry by the input $C_{in}=0$ and $C_{in}=1$ and it is selected by the multiplexers (mux); so, it is not efficient in area. Binary to Excess-1 Converter (BEC) [10] is used with the input $C_{in}=1$ to achieve reduction in area and power consumption. Instead of RCA this converter is used [3], [6]. It comes from minimum logic gates than the structure of full adder. The SQRT CSLA is processed to analysis the design performances of power, delay and area than the other adders. Ripple Carry Adder (RCA) computation time is high in the compact design. For fast process of deriving results Carry Look-Ahead Adder (CLA) is used in the Time critical applications which lead to improvement in area [1]. In RCA carry select adder provides less area with longer delay but Carry Look Ahead adder provides less delay with large area. Fig [1] shows the 4-bit RCA circuit.

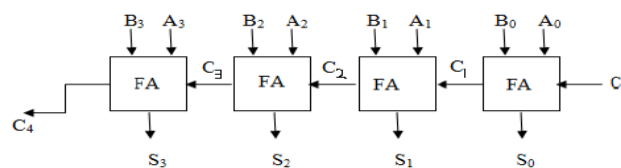


Figure 1: 4-bit RCA

This paper is organized as follows: Section II deals with the literature survey of the CSLA structure and process. Section III deals with the methodology of adder blocks RCA and BEC. In Section IV the proposed modified CSLA design and its design are discussed. Section V deals with the ASIC stimulation results analysis of the proposed circuit. Section VI concluded the work and its performances with future scope.

Related Works

In this section, the related work of the adder circuit for consumption of power and area are discussed. Ripple carry adders exhibits with slow speed of compact design but carry look ahead performed faster and consume more area[1]. Between adders it acts as a negotiation. In 2002, hybrid carry look-ahead/carry select adders is designed and performed with addition process of increasing speed. Also hybrid full adder is accessible with low power multipliers. In analysis of Carry look ahead Adder (CLA) and RCA with 32-Bit Multiplier using VHDL shows that the speed of the CLA multiplier is almost double than the RCA multiplier [10].

For the reduction of circuit consumption BEC is used in the modified CSLA instead of RCA with increasing the delay slightly. For more improvement BEC is replaced with the D latch when enabling the signals [4]. In RCA, linear proportional of N delay is performed with N-bit, so highest delay process is performed by the adders. Normally CLA provides faster results with more delay process than the other adders. It provided because of large number of logic gates and fan-in [2].

The mobile industry is growing rapidly not only because of arithmetic unit but also with the arithmetic units of less power and area. A Simple and efficient modification of gates level makes the reduction in power, area and delay. Based on the modifications of CSLA the performances compare with other adders. By the BEC modification instead of full adder chain the logic converter provides the circuit with slight changes of delay. The fast process performances of CSLA are used for arithmetic functions in data processing processors [5], [7].

The carry select adder (CSL) design is perform in the space-time tug-of-war. It exhibits the gate depth in the structure of adder and implemented dual ripple-carry adder (RCA) with the input 0 and 1 respectively. Carry Select Adder (CSLA) is an optimization process in the constraints of VLSI design. It works with efficient and simple process of significantly modification of gate-level and the Parameters reduction in CSLA [8], [11].

To overcome the issues in consumption of area, power and delay in 4-bit, 16-bit, 32-bit Regular CSLA, modified CSLA without using mux, modified CSLA using BEC and modified CSLA using D-Latch & Carry look ahead adder the proposed system is designed and simulated to give better performance. The proposed architecture has been developed and evaluated the performances of the design in terms of delay, power and area. The gates level is modified and required less gates to perform the operation in the proposed work. It provides area reduction and the total power. The results analysis shows the better performances of the circuit and faster than the others. In this way, it makes efficient and simple way of process the VLSI hardware implementations.

Methodology

In this section the blocks of adder which are used to perform the operation with less consumption of area and power are explained. The evaluation of area and delay are performed by using the theoretical approach and shows the effects of the implementation process with power and area. Fig [2] shows the AND, OR, and Inverter (AOI) implementation of an XOR gate. The methodologies of evaluating or consuming all gates are considered to have an AOI implementation and having delay and area equal to 1 unit for each. Then the longest path of the blocks are added the gates to donate the maximum delay. By counting the total gates required for the logic block the area evaluation is done.

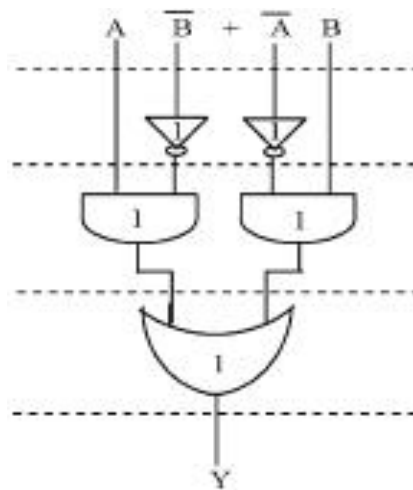


Figure 2: Delay and area evaluation of XOR gate

For speed and reduction of consumption of area and power AOI is used instead of RCA and BEC with $C_{in}=1$. In modified design this logic can be used and provides better performances by using less number of gates than the n-bit Full Adder (FA) structure. As stated above the aim of this work is to use AOI in order to provide an efficient and simple manner of performances than the existing. Fig [3] shows the function of BEC. For example consider the replacement of RCA with BEC as shown in Fig [4]. From this the proposed architecture and its function are explained in the next section.

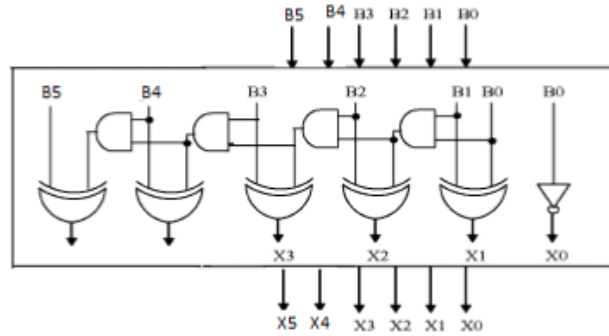


Figure 3: 6-Bit BEC - Existing Circuit

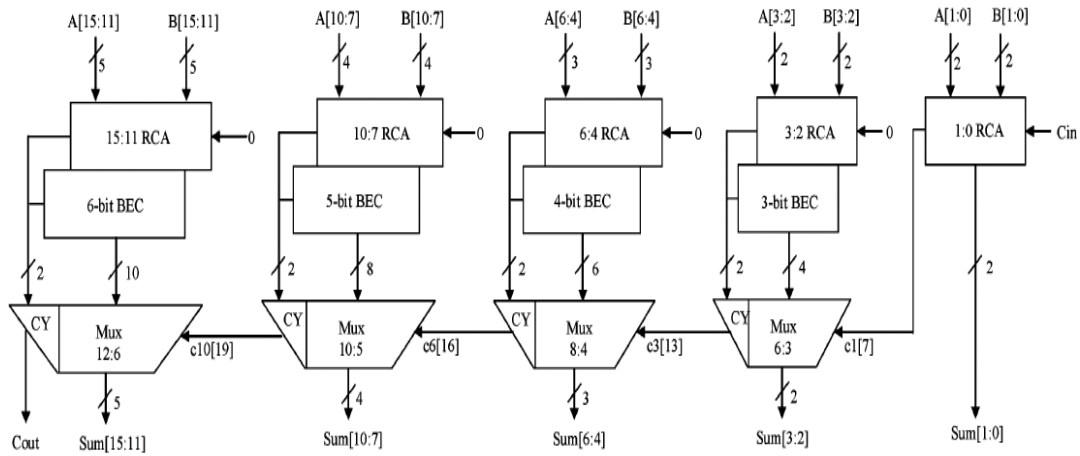


Figure 4: Modified 64-bit Sqrt CSLA of BEC -Existing Architecture

Architecture of Modified 64-Bit Sqrt CSLA

In this section the proposed architecture and design of 64-bit Sqrt CSLA are explained with its analysis. For improvement of power and area consumption in the circuit the existing circuit as shown in Fig [4] is modified by the proposed adder design. Among dual adder one of the adder is replaced by the proposed adder with the same input $C_{in}=1$. Any adder in modified 64-bits Sqrt CSLA is replaced by AOI in order to improve the performances of delay, power and area than the other adders. As per the function the proposed adder is group the blocks and evaluated the performances. The proposed group circuits are illustrated as shown in the grouped circuit.

In proposed work, AOI is performing the operation as similar as the other adder and the block diagram of modified circuit is shown in Fig [6]. The requirement of the bits for the logic function is 1 bit higher than the other. It divided the input in to various bits size of different groups which have with the RCA, equivalent Mux and AOI. Each group has a function of significant process of sum and carry. As in Fig [6]

Group 0, having lower significant bit and provides results of sum[1:0] and carry out the selection function of line as mux process in the circuit for the next stage.

Similarly, next level process as same as group but includes the logic of AOI instead of other adder with $C_{in}=1$. As per the values consideration of delay and arrival time of input selection of C_1 of 8:3 mux is processed to next level and it proceeded with previous sum of RCA and BEC. For residual groups the arrival of input selection is advanced to RCA and BEC. Thus, the output of mux are computed the results with the adder respectively. Each level of input is depends on the previous output of corresponding mux. In rest of the level the arrival time of the input selection of mux is always higher than the input from AOI. Thus, the left over process delay of MUX is depends on mux selection input and delay. The proposed Modified CSLA architecture is designed with the implementation code of multiplexers 6:3, 8:4, and 10:5 and full adder up to 24:11. The design code of AOI is designed by using the gates as in the circuit.

For the evaluation of proposed method of power, area and delay consumption is done by implementing the modified 16-bit Sqrt CSLA with modified area efficient CSLA. The main notion of proposed work (MA-CSLA) is to reduce the gate count by using XOR gate. The possibilities of gates reduction by XOR gate is clear mentioned in Fig [2]. In Modified CSLA the XOR gate count is 210. But in proposed Modified Area Efficient CSLA (MA-CSLA) count is 168. The Modified Area Efficient CSLA (MA-CSLA) is expressed the operation of XOR gate as follow.

$$Y=(a+b)(\sim ab)$$

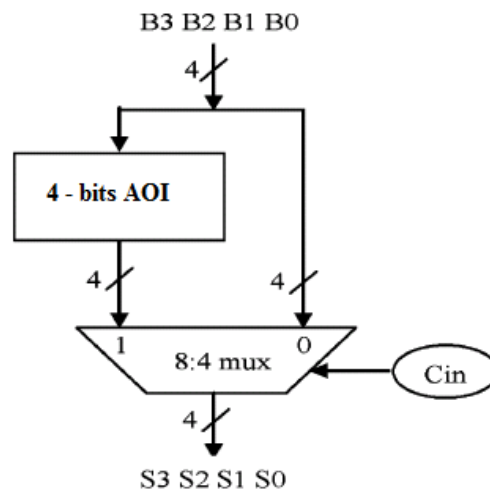


Figure 5: 4-bits AOI

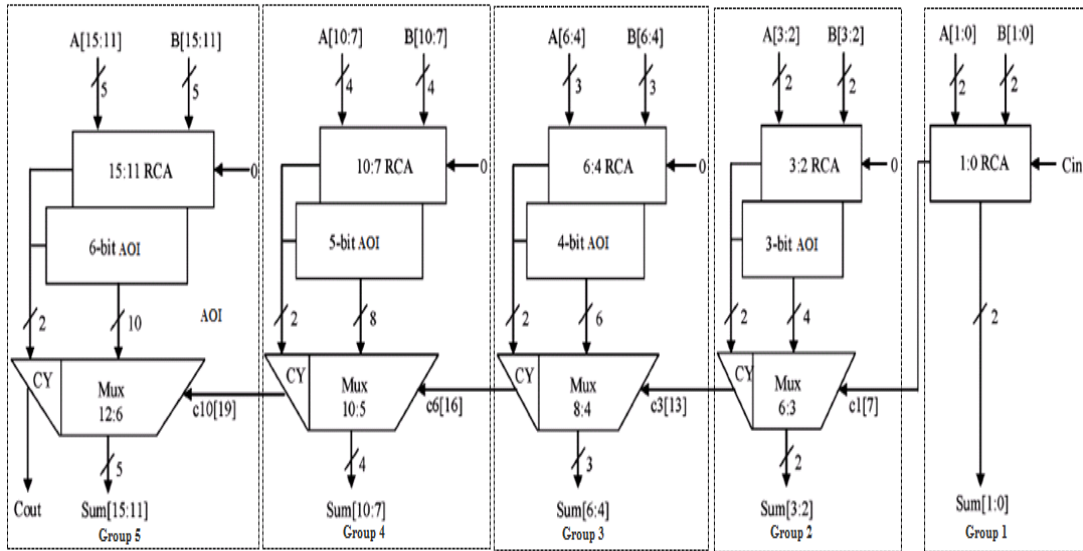


Figure 3: Modified Area Efficient Carry Select Adder (MA-CSLA) - The parallel existing adder is replaced with AOI.

The proposed structure of modified 16-bits SQRT CSLA is optimizing the consumption of parameters in the circuit. Each group level of the circuit is evaluated the power, delay and area as illustrated in Fig [6a], Fig [6b], Fig [6c] and Fig [6d]. In group 2 consider 2-bit RCA with one full and half adder for the input $C_{in}=0$. Instead of second 2-bit RCA a 3-bit AOI is used with the same input $C_{in}=1$ and includes one to the output. The group 2 gate count is obtained as follows.

Group 2: FA=11(11*1); HA=5(5*1); NOT=3; AND=4; OR=2; MUX=12(3*4).

Similarly, other groups of gate counts are obtained. In groups, the verification is done that from RCA the 2-bit input sum is arrived when $c_1=0$ and if $c_1=1$ then the input will arrive from the AOI.

Gate count = Sum (Full adder, Half adder, MUX)

In this paper, we proposed an area-efficient based adder for consumption of area and power. It process by sharing the logical terms of common Boolean. For each summation operation required single XOR and Inverter gate in the circuit of sharing partial after the simplification of logic. As well as same gates are needed in each operation of carry-out. According to carry-in signal state of logic the correct output results are selected through multiplexer. In this way, in carry select adder (32-bit) the count of transistor is reduced from 1947 to 960. Moreover, the power reduction is from 1.26mw to 0.37mw and the delay product of the power is reduced from 2.14mw*ns to 1.28mw*ns.

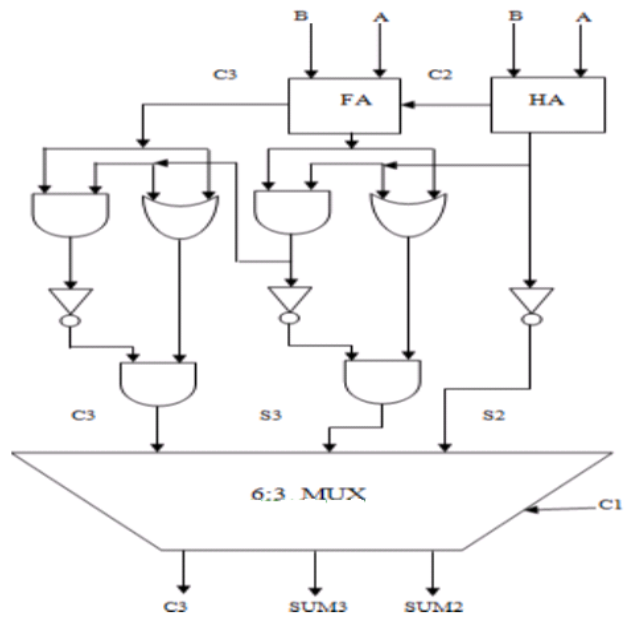


Figure 6a: Group 2

Table 1: The Group Count of Area And Delay

Group	Delay	Area
Group1	10	22
Group 2	13	37
Group 3	15	56
Group 4	18	75
Group 5	21	94

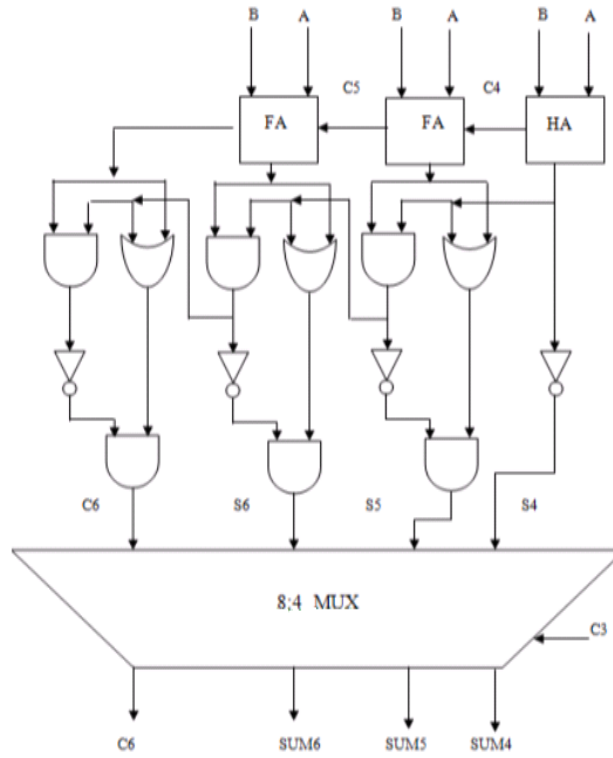


Figure 6b: Group 3

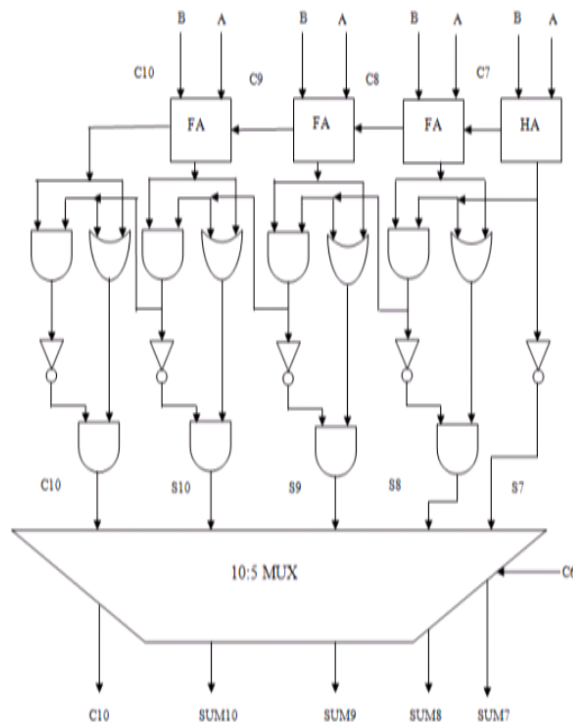


Figure 6c: Group 4

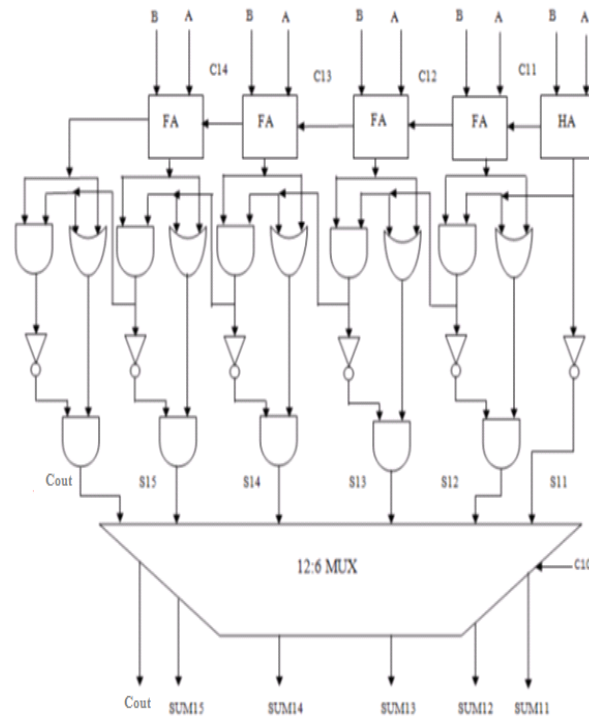


Figure 6d: Group 5

ASIC Implementation Results

The proposed design in this research work has been developed and implemented using Verilog-HDL and synthesized the design in Cadence RTL compiler using typical libraries of TSMC 0.18 um technology. The respective and synthesized design is imported from the Verilog net list and the constraints file (SDC) to Cadence SoC Encounter. Then the automated layout is generated from the routing, placement and standard cells. Using Encounter's Native RC extraction tool the parasitic extraction is performed. For static time analysis in the platform of encounter the extracted parasitic RC (SPEF format) is interpreted back to Common Timing Engine. For power simulations of the adder each count size of word is evaluated and all conditional input possibilities are generated the common value changed dump (VCD) file, as well as imported it to Cadence Encounter Power Analysis.

Table I exhibits the CSLA simulation results in terms of delay and area. The total design cell area is indicated as area and the total power of internal, switching and leakage are indicated as power. Fig [7a] and Fig [7b] shows the Register Transfer Level (RTL) design or dataflow design of the proposed circuit adder and MUX function. Fig [8] shows the performances of area reduction of the proposed modified circuit with the comparison analysis of other CSLA and the comparison analysis of power reduction of the circuit is in Fig [9]. Fig [10] shows the Simulation results of MA-CSLA.

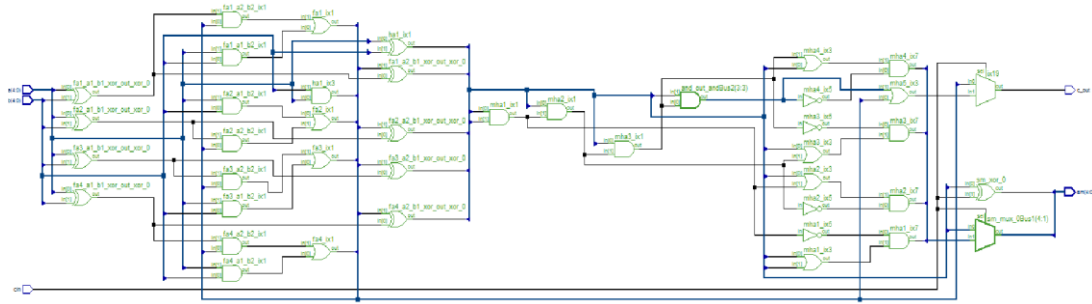


Figure 7a: RTL Diagram – Proposed Adder MUX Function

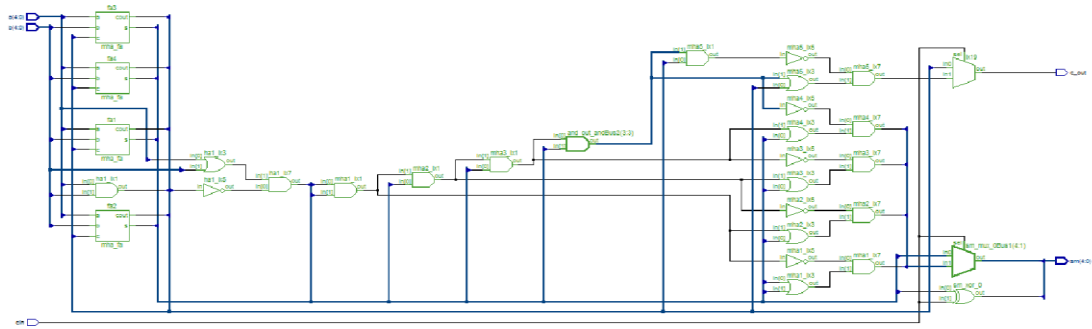


Figure 7b: RTL Diagram – Proposed Adder Circuit

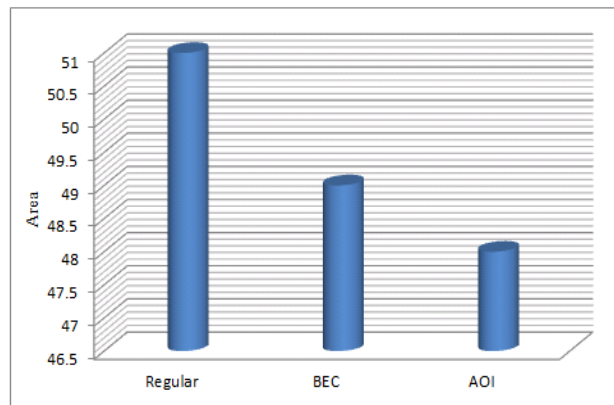


Figure 8: Performances Analysis – Area Of MA-CSLA

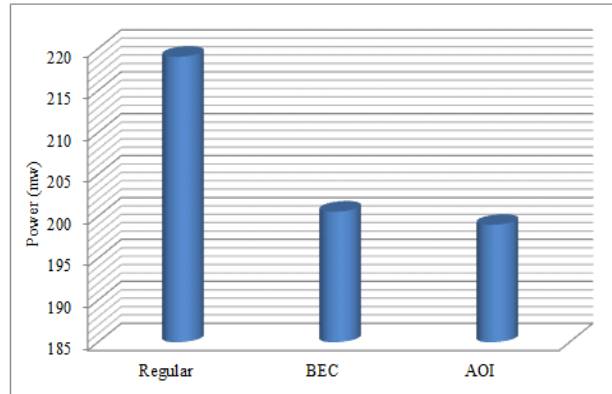


Figure 9: Performances analysis – Power of MA-CSLA

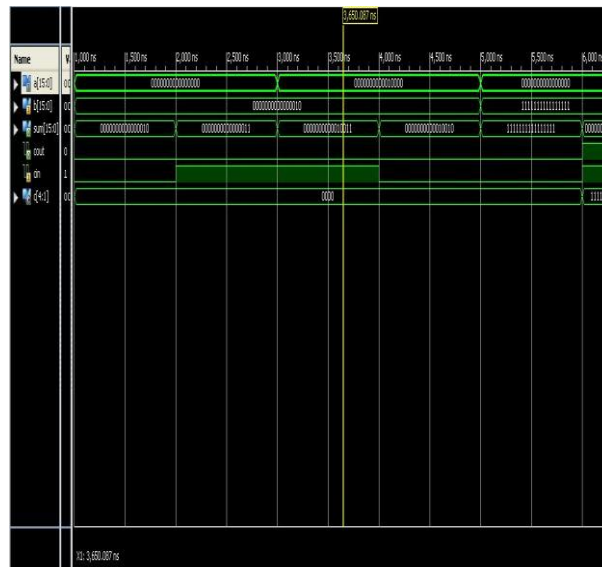


Figure 10: Simulation Results of MA-CSLA

Therefore, the proposed SQR CSLA clearly shows the performances that the area of the 8, 16, 32, and 64-bit is reduced. Similar the power consumptions show the reduction improvement with the bit size. Interestingly, exhibits the delay overhead is decreasing similarly with bit size. The product of power–delay of 8-bit proposed CSLA is higher and the product of area–delay is lower than the existing. However, the proposed 16, 32 and 64bits product of area–delay and power–delay is reduced.

Conclusion and Future Work

In this paper, Modified 16-bit SQR with Modified Area Efficient CSLA is proposed to reduce power, delay and area. The reduced of number of gates provides better performances than the existing in terms of delay, area and power. The compared

results analysis shows that the proposed modified SQRT CSLA has improved and provides low consumption of power and area. The product of power-delay and area-delay of the proposed design has been improved and indicates the method improvement but not a delay of mere tradeoff for power and area. Therefore, the proposed circuit shows the efficiency and the performances with less area, low power, efficient and simple for VLSI hardware implementation. Future more think to extend the work of design and to test the design with modified 128-b SQRT CSLA. Also improve the parameters level of the modified CSLA for better consumption.

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