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Low Power Bist on Memory Interface Logic

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Abstract

Built in Self Test using a random test pattern generation for memory devices with a differentiable logic of Automatic Test pattern generation (ATPG) will helps in tracing the CUT (circuit under test) is perfect or error. This BIST is a scan chain process based on shift operation and the ATP clock. The output verification is processed by SCAN based test with LFSR (Linear feedback shift register) to attain the low power values of test patterns and LPLFSR. This architecture is proposed for a low power consumption application of MEMORY operation based on Read, Write operations. Based on the Read and Write operation along Shift bit activation and deactivation BIST generation is obtaining for tracking the error. Comparison of power is processed between LFSR and LPLFSR along with SCAN test.

Index Terms: BIST, Random, Automatic Test Pattern Generation, Circuit Under Test, Low Power-Linear Feedback Shift Register, Memory, Finite State Machine, Read, Write and Power.

Introduction

Power utilization is the major contra following the chip designing world microcontrollers has to be replaced by using these chips with their low power applications. BIST is mainly used for testing the circuits whether is worth enough to place on a chip and helps in identifying the error propagating region of bit which differs in the logic orientation. This BIST is of various types they are LBIST, BIST, ATPG, Self heating elements etc.

The disadvantage of BIST is that it impacts silicon area and timing. BIST engine for generating data patterns and result comparison at high speed, the routing resources from all memory interfaces to the BIST engine has adequate cost. The impact of BIST

on timing is that all memory interface signals needs to multiplex between BIST signals and functional signals [1].

Applications of BIST are for On-Board diagnostics with high reliability, Aviation, Integrated circuits, Automotive Electronics e.t.c.

Table 1: Procedure followed by the authors in various papers

Authors & Title	**Procedure Approached**
Manohar Ayinala, Parhi, "High speed parallel architecture for linear feedback shift registers"	LFSR with cyclic redundancy was explained BCH encoders operation of an IIR filter. This helps in feed forwarding and back warding with pipelining that can be applied to any generator polynomial[3]
Sachin Dhingra," Comparison of LFSR and CA for BIST"	Testing itself indicates or explains the concept of built in self. Here a comparison between LFSR and CA (cellular automata) for test pattern generations with test response analysis with design for testability technique [4].
Sinbh. B, Khosl. A, Bindra. S, "Power optimization of Linear feedback shift register for low power BIST"	LFSR test pattern generation technique with reducing power dissipation during testing and correlations consecutive patterns during normal mode during testing by reducing the transactions generated by conventional LFSR [5].
Mohammad Teharnipoor, Mehrdad Nourani, Nisar Ahmed, "Low Transition LFSR for BIST based applications".	Scan based Bist architecture were explained with BIST using Circuit under test between consecutive patterns [6].

The rest of the paper is organized as follows in the section II TPG is discussed with low power generation and automatic pattern will also discussed in this section, in the section III memory interfacing along with read, write operation will be discussing, in section IV memory is exposed with the proposed architecture and in section V, VI were helps in explaining the results along with the concluding attention.

Low-Power Test Pattern Generator

Various approaches were followed for generating test patterns here scan chain is designed for testing the circuits in a sequential order. Pattern generators that are D-algorithm, Path Oriented Decision Making algorithm (PODMA), Fan out oriented, Pseudo random test generation and Wavelet automatic spectral pattern generator are used.

In this paper Pseudo random test generation is used for BIST. Randomness is observed by the mathematical analysis provided below is uniform distribution $U_K \in \{0,1\}^K$where U is the uniform distribution and K is the level of distribution.$T: \{0,1\}^l \rightarrow \{0,1\}^n$ With $l \leq n$ where "l" is the seed length and "n" is the

test pattern generation level. Randomness with the finite set is represented as $F = \{f: s \to t\}$ based on the statistical distance between the distributions. Based on the clock signal in and out of scan chain arbitrary process of flip-flop connected to long shift register is accessed.

Low Power BIST

We know that mainly BIST is used to test itself its ciruitary without any need of external equipments. It is mainly applicable to sequential circuits because of their complex designs. Here low-power BIST is nothing but to generate low power by using different generation techniques. In this we used LFSR and LP-LFSR(low-power linear feedback shift register) using 8-bit generators. We can also use ATPG or Scan Chain.

LFSR (linear feedback shift register): It is mainly depends upon the polynomial equations of feedback. It is used to generate the patterns in a sequence based on the e-xor gate. The use of this e-xor is based on the bits will get shifted in order to obtain the original bit sequence. Use of LFSR results accurate and high performance so that we can perform the testing in a short span of time.

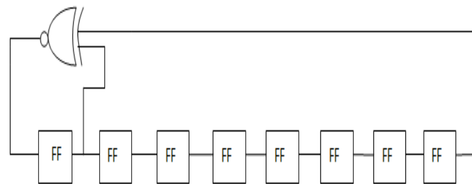


Figure 1: a) Architecture of 8-bit LFSR

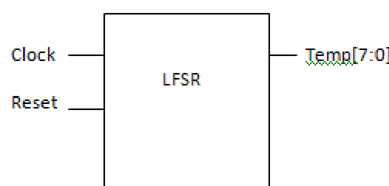


Figure 1: b) Block diagram of 8-bit LFSR

LP-LFSR (low-power linear feedback shift register): The additional part to LFSR is MUX which finally produces a Low power LFSR. The relation for multiplexer and this LP-LFSR is multiplexer contains n-inputs and single output. Because of the selection line one bit will get detected so that the circuitary will be less. Based on the last output bit of lfsr the selection line will get activate or deactivate i.e if it is 1 then it swaps the bits and if it is 0 it will remains same. Because of this swapping intermediate patterns will get generated .So as the area consumption is less the delay

will gets reduces and power consumption will also gets reduces that's why it is said to be a low power lfsr.

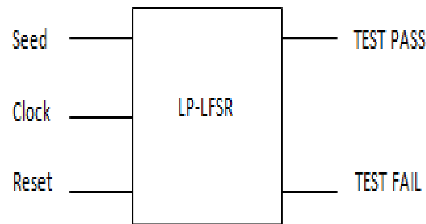


Figure 2: Block diagram of 8-bit LP-LFSR

BIST architecture taken in this paper mainly contains Test pattern generator,and two circuit under test, and comparator.

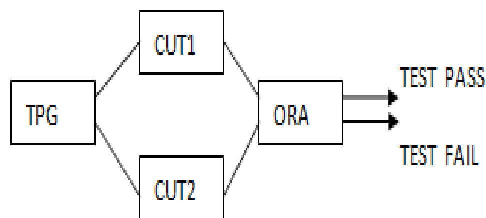


Figure 3: Architecture of BIST

In this paper LFSR and LP-LFSR are comparing with powers between them .Here in the place of automatic test pattern generator we are generating 8-bit LFSR and 8-bit LP-LFSR and in the place of circuit under test we opt 4-bit Multiplier and the comparator is used to compare the patterns coming from the two cut's and gives the output.If the two patterns are same it will gives output 1 if not it gives 0. Figure 2, 3 & 4 defines the block schematics of LFSR CIRCUIT UNDER TEST and LP-LFSR CIRCUIT UNDER TEST.

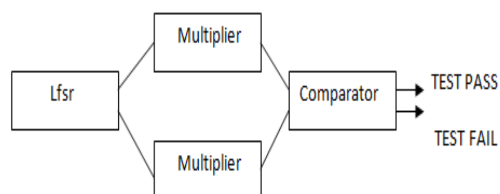


Figure 4: a) Architecture of LFSR_BIST

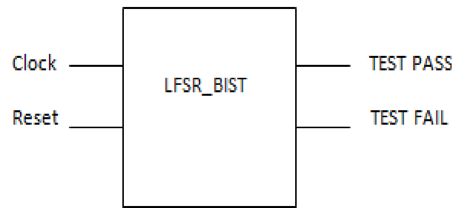


Figure 4: b)Block diagram of LFSR_BIST

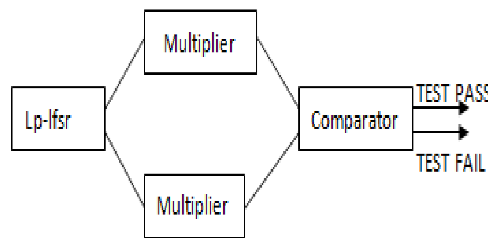


Figure 5: a) Architecture of LP-LFSR_BIST

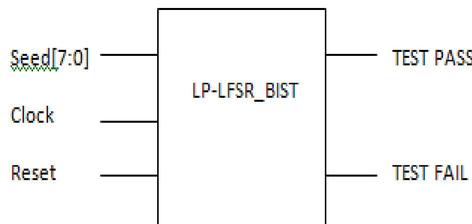


Figure 5: b) Block diagram of LP-LFSR_BIST

Ram Using Bist

RAM is for temporary storage of large quantities of information. Ram IP typically finds usage in cache solutions, temporary buffers or whatever large memory instances are required in an SOC(system-on-chip design). It mainly contains Row decoder, Column decoder, Address generator, clock, Reset, Read/Write and sense Amplifiers. In this paper RAM using BIST mainly deals with the testing of memory by using LFSR and LP-LFSR and comparing the powers generated by both of them. The RAM here we are considering is 8-bit which contains 64 storage cell locations .It is only a single port RAM just for analyzation we took only the single port so that it has single set of address and controls and it can only have single access i.e(read/write) at a time.

Read/Write

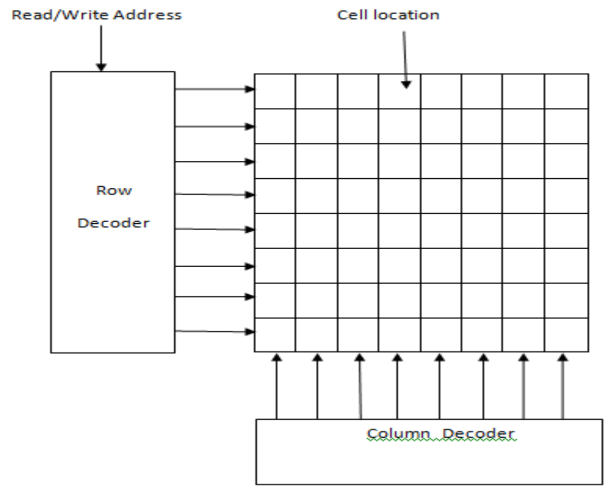


Figure 6: a) Architecture of RAM with single

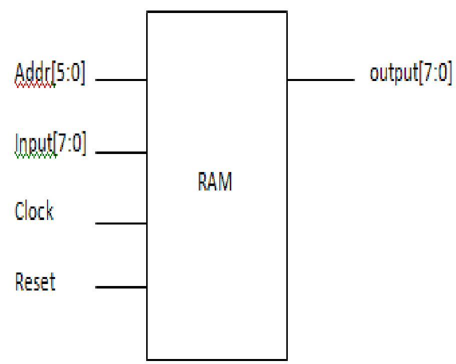


Figure 6: b) Block diagram of RAM

Memory testing is nothing but testing the each and every cell even though the data is present or not.

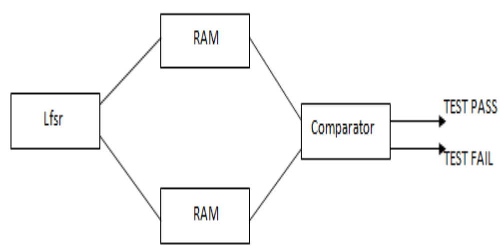


Figure 7: a) Architecture of RAM_BIST_LFSR

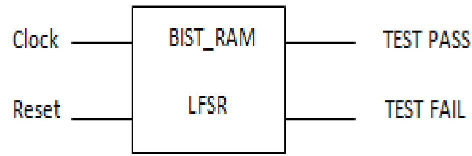


Figure 7: b) Block diagram of BIST_RAM_LFSR

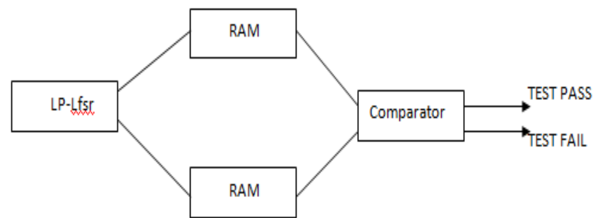


Figure 8: a) Architecture of RAM_LP-LFS_BIST

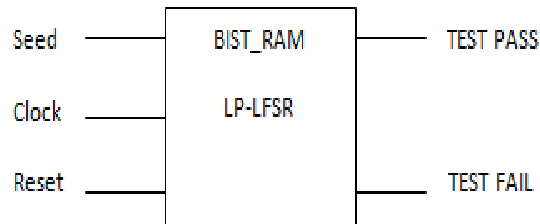


Figure 8: b) Block diagram of BIST_RAM_LP-LFSR

By testing each and every cell even though the data is present or not is a time consumption thing so that in the next section V it will describes about the testing of memory accurately .

Memory Interfacing Logic

This is extracted from [1].

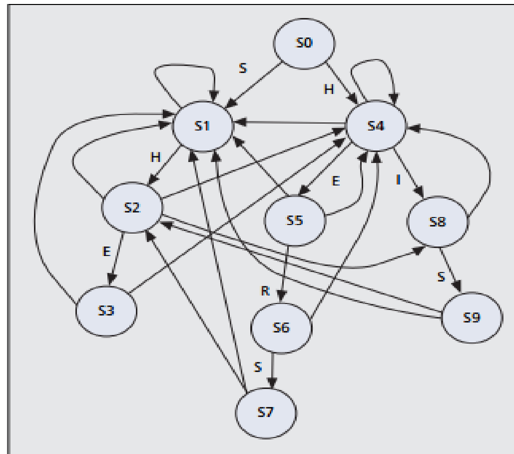


Figure 9: Example of FSM charts under matching conditions

Deterministic finite automata (DFA) can match multiple strings simultaneously this helps in introducing LFSR and LP-LFSR, in worst-case time linear to the size of a packet. Figure 9 show an example DFA matches "HIS, HERS and SHE". Initializing at state S0, the state machine is shifted to state S1 or S4 depends the input character "S" or "H". When end state is reached, a string has to be matched.

In the example in Figure 9, if state S7 is activated, string "HERS" will match. Each state in the machine has pointers to other states in the Finite State machine. If input character is the next character in a string that is currently being matched, the algorithm moves to the next state in that string; otherwise, the algorithm follows a failure pointer to the first state of another string that begins with that character or to the initial state of the machine if no other strings begin with that character.

An example of this can be seen in Figure 9. If the current state is S5, the last input characters would be "HE." If the next input character were to be "R," then the next state would be S6. If the next input character were not "R," but instead, "S," then the next state would follow a failure pointer to state S1, which is the starting point for the string "SHE."

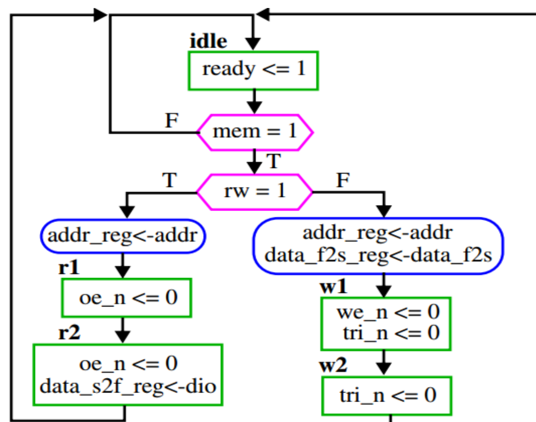


Figure 10: FSM chart for read and write operation in the memory

In figure 10 FSM charts for read and write operations are explained as initial operations are in ideal condition the if the data is read/write operated in memory and then read/write will be accessed if read is activated then memory will be read from memory or if write is activated then data will write into memory at the location of address.

Memory Built In Self Test

BIST is still important and provides a comprehensive coverage in testing the memory core with the basic address, data in, data out, READ, and WRITE control signals. However, BIST does not cover some of the shadow logic that may be embedded in the memory interface logic. Herein, the proposed approach seeks to enable the memory array to do WRITE and READ in the same cycle during ATPG. As such the complex multicycle sequential patterns requirements to prevent x propagation will not be needed. From circuit point of view, the READ and WRITE operations can occur in the same cycle. Further, memory in this mode will pass the WRITE data into the output data through the memory bitline. As long as the WRITE driver is stronger than the bitcell, it will always direct the bitline to what the WRITE data value is [2]. For memory built in self test the schematic consists of memory read and write with memory sub-array using address generator block along with two shifter block using LFSR or LPLFSR random test pattern generators for BIST operation mode of activity. Most of the memory related BIST papers in the literature focus on optimizing BIST and memory repair. For example, Cao et al. [7] focused on BIST in designing an efficient built-in self-repair strategy which can store each fault address only once.

The added complexity is due to the need for any READ operation to be preceded by a WRITE operation to the same address, otherwise the READ data will be unknown (X). Functional testing is done by porting some of the high coverage tests used in verification phase of the design into test vectors. These tests are categorized as quality tests that focus on basic functionality of the chip. The challenge in functional testing is in debugging failing tests. The failing point can be observed several cycles after the actual failure occurs. Even though the actual failure might not be identified, functional failure can give input to “LFSR or LPL FSR” based test to do further testing [1]. The control signals will be modified accordingly to activate READ operation when WRITE operation is active, only during BIST mode. The data signal is OR-ed internally in the sub-array to generate READ clock.

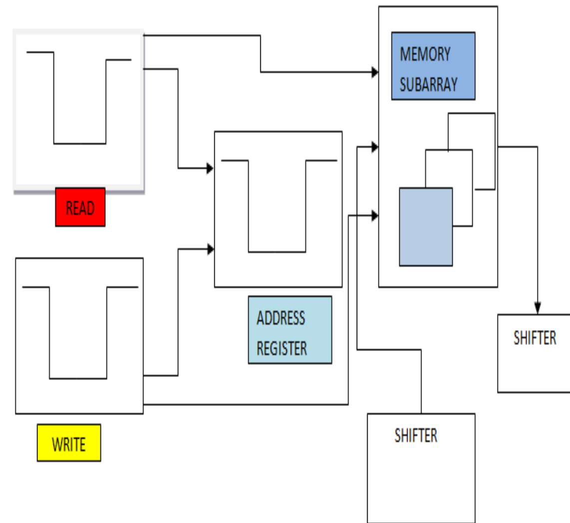
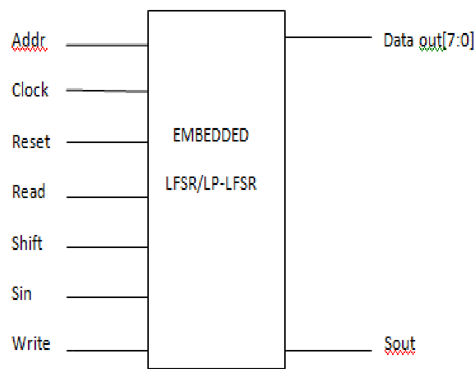
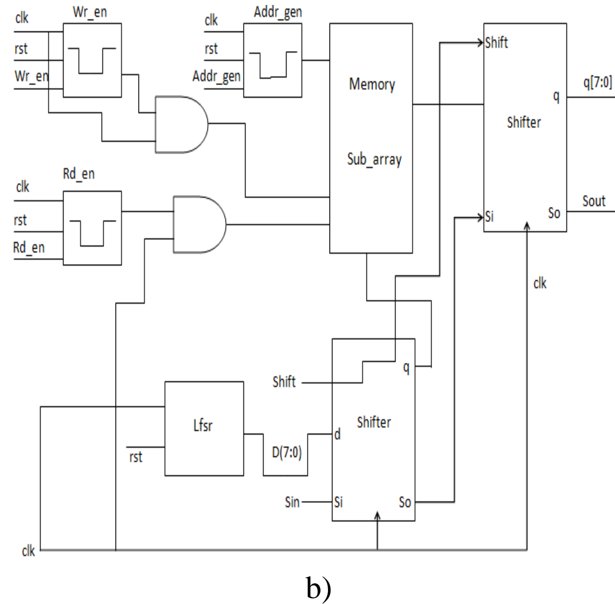


Figure 11: Proposed scheme to enable READ and WRITE operation to cover interface logic

The process of read/write the bits and shifting and comparing the bits will be done only whenever the R/W ,clock, Sin is1. The data which is used for shifting is coming from the LFSR and LP-LFSR. The whole model of this proposed method is to generate low power and compare it with the RAM_BIST powers. BIST is for sequential , TPG is for combinational logic bounded by flip-flops, and signature analysis is for basic functionality. However, there is a space in the existing methodologies in testing the memory interface and the glue logic around it. For example, alignment logic in caches such as in [8] is not fully tested by BIST.



a)



b)

Figure 12: a) figure a shows the block diagram and b)Proposed scheme to enable READ and WRITE operation during TPG using LFSR or LPLFSR to cover interface logic.

Results

FPGA XILINX Simulations for Power Comparisions.

Device Configurations	Power Utilizations
SPARTAN-3E	0.034 Watts
SPARTAN-6	0.014 Watts
SPARTAN-6E Low Power	0.011 Watts
Virtex-4	0.172 Watts

Conclusion

Here the BIST operation is performed by using shifter bit activation along read and write cycle on the memory. Selecting and scanning all the data in the memory bit by bit is performed and the changes were also obtained tabulated and power analyzied in the results. These results shows the power utility of LFSR and LPLFSR under different temperatures and on different FPGA device configurations. This rated testing helps in increasing the product quality along with memory interfaced logic fault coverage.

Future Scope

In future these can be extended to huge number of memory blocks under different test pattern generations produced by the LPLFSR circuit. i. e here in this the BIST testing is done for single SOC. Furthur it can also used for testing the multiple sub-array memories.

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