

High Efficiency Design of Switched-capacitor based Charge Pumps in Cadence 180 nm Process

Amritpal Singh¹, Pawandeep Kaur², Raman Kumar³, Irfan Ahmad Pindoo⁴

*Department of Electronics and Communication, Lovely Professional University
Phagwara, Punjab, India*

*er2amrit@gmail.com¹, pawandeep.kaur@lpu.co.in²,
raman.kumar2@lpu.co.in³, irfan.pindoo@gmail.com⁴*

Abstract

In this paper, a low power charge pump with high power efficiency is presented. It describes the factors governing the output voltage, power efficiency, output resistance, frequency, power dissipation and the capacitors of the charge pump. The proposed circuit is designed and simulated in Cadence virtuoso tool in 0.18 μ m CMOS technology. The output voltage of the proposed charge pump after using two stages is 8.16 Volts with low settling time. In this paper various techniques have been used to achieve the required output voltage. Various types of charge pumps have been compared with the proposed charge pump in terms of the power dissipation. The equations used to design the charge pump has been presented in the paper.

Keywords— DC to DC converter, Charge pump, Charge Transfer Switch.

I. INTRODUCTION

The whole world has been crowded by the electronic means comprising of portable devices. As the portable devices are low voltage and low power devices, their internal circuitry need higher voltages to operate such as flash memories, SRAM, DRAM, power IC and continuous time filters [1]. But for the requisite of higher voltages, battery or supply cannot be scaled up due to the portability constraints. So it is desired to use an efficient charge pump (CP) which can meet the requirements of portable devices. Low power consumption and high voltage efficient circuit designs play a key role in these portable devices.

Power converters consisting of switches and capacitors have long been known to develop circuits like diode-capacitor, AC-DC and DC-DC voltage multipliers [2]. In contrast to the power converter where both inductive and capacitive energy storing

parts are used, SC converters are inductor less, hence conceivable integration and high power density can be achieved. There are few implementations where switches and control hardware are integrated [3-7] on to a single chip. It is possible that even the capacitors could be merged on the chip, which would prompt further upgrades in size, dependability and expense of the converters. Operation down to zero head is conceivable with no requirement for a complex or dummy control technique.

Dickson charge pump is the most popular approach for the charge pump analysis because they are switched-capacitor networks and can be implemented with integrated circuits on the same chip. Diode based Dickson charge pump was introduced by J. Dickson for On-chip [8] high-voltage generation. Later on various techniques had been presented by the authors for improving the performance of charge pumps. It was further proceeded by an improved voltage multiplier [2] technique. Synthesis and reliability conditions of switched-capacitor DC to DC voltage multiplier circuits designed from [9] voltage doublers with more sophisticated clocking scheme and least number of capacitors were presented. They have also introduced the concept of voltage regulation with frequency regulation [10]. In [11], authors have considered the effect of threshold voltage drops and used the charge transfer switches in parallel to design a new charge pump using static charge transfer switches (CTS). Further, reverse charge sharing effect limitation due to improper biasing of charge transfer switches was improved by introducing the voltage controller [12] and further they introduced the cross coupled stage at output to improve results. The alternate solution to eliminate the reverse charge sharing effect is to use dynamic charge transfer switches. It requires some auxiliary circuit made up of PMOS and NMOS so that the charge transfer switches could be completely turned off. Because of that auxiliary circuit, reverse charge sharing effect is completely eliminated [13]. Authors in [14] did not suffer with the gate-oxide reliability issue and were able to suppress the backward leakage current. As a result, smaller output ripple voltage and better pumping efficiency was achieved. Moreover, four-phase clock generator expressively improves the pumping gain of the four-phase charge pump for supply voltage nearby to the threshold voltage of MOS transistor. The single clock charge pump presented by Muhammad Adeel Ansari, Waqar Ahmad and Svante R. Signell in [15] achieved similar results after using equal number of stages as that of the Dickson charge pump.

In this paper, section II describes about the basic Dickson charge pump. Section III introduces various charge pumps. Section IV presents the proposed charge pump. Section V discusses the results and conclusion of various techniques with respect to the proposed charge pump.

II. VARIOUS CHARGE PUMPS

A. *Diode based Dickson charge pump analysis*

The basic Dickson charge pump consisted of diodes and capacitors in the pumping chain forming a switched-capacitor network. Diodes based Dickson charge pump is shown in Fig. 1. Diode connected MOSFETs like PMOS are utilized to build up the Dickson charge pump [8]. PMOS is used as switch and capacitors are used for storing and transferring the charge. So the capacitor charging and discharging comes under

process. Capacitor charging and discharging equations are given as below.

The capacitor charging equation is given as below.

$$V_c = V_{in} (1 - e^{-\frac{t}{\tau}}) \tag{i}$$

The capacitor discharging equation is given as below.

$$V_c(t) = V_0 e^{-\frac{t}{\tau}} \tag{ii}$$

Where “ τ ” is the charging time constant and “ t ” is the charging time of the capacitor. The time constant “ τ ” can be calculated as shown below.

$$\tau = RC \tag{iii}$$

Where C is the capacitance in series to the resistance R.

The output voltage of the Dickson charge pump is given as below.

$$V_{out} = GV_{dd} - R_{out} I_{out} \tag{iv}$$

Where G is the number of stages used, R_{out} is the output resistance and I_{out} is the total output current. All these factors have been discussed in the next section.

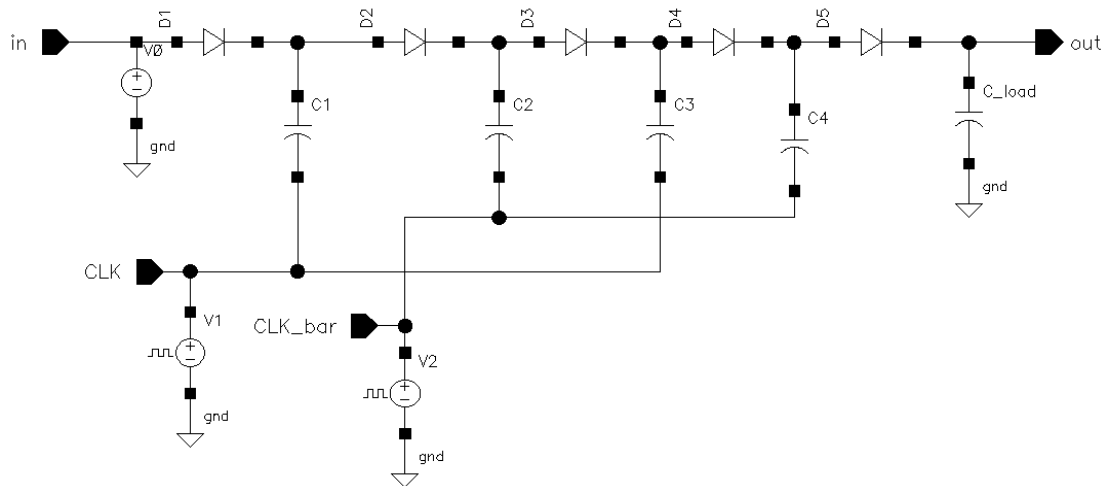


Fig. 1 Schematic of Diodes based Dickson charge pump.

Dickson charge pump (CP) using PMOS as a diode is shown in Fig. 2. It is driven by two input clocks which are out of phase to each other. MOSFETs connected in diode configuration work as switches with its time period depending on the clock signal. As the CLK goes low the PM1 will be conducting. So voltage at node 1 will be:

$$V_1 = V_{in} - V_{df} \quad (v)$$

Where V_{df} is diode forward voltage. As CLK goes high, the capacitor will be charged. The voltage amplitudes of both clocks as well as input signals are same. Now, as the capacitor gets charged, the voltage at node 1 will be:

$$V_1 = V_{in} + V_{in} - V_{df} \quad (vi)$$

As CLK_bar goes low, MP2 will be ON. So, voltage at node 2 will be:

$$V_2 = (V_{in} + V_{in} - V_{df}) \quad (vii)$$

Now, as CLK_bar goes high again, then capacitor gets charged again and the voltage at node 2 will be:

$$V_2 = V_{in} + 2(V_{in} - V_{df}) \quad (viii)$$

Hence, the output after N stages will be given by:

$$V_{out} = V_{in} + N(V_{in} - V_{df}) \quad (ix)$$

Here the effect of stray capacitances has been ignored. In the presence of load, the output voltage will be given by:

$$V_{out} = V_{in} + N(V_{in} - V_{df} - \frac{I_{out}}{2\pi C \cdot f_{osc}}) \quad (x)$$

By this point we got to know about how to size the capacitors to meet our requirements. Now, the parameter capacitor, output resistance and frequency (f_{osc}) will be analyzed.

$$f_{osc} = \frac{I_{OUT} N}{C \Delta V} \quad (xi)$$

Where I_{OUT} is the output current and N is the number of stages, C is the pumping capacitance and " ΔV_{tot} " is

$$\Delta V_{tot} = (N+1)(V_{in} - V_{df}) - V_{out} \quad (xii)$$

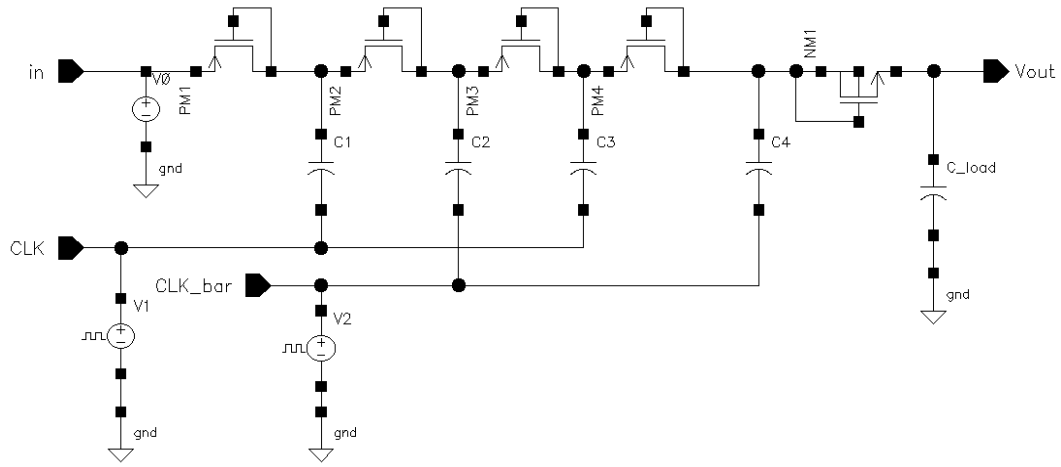


Fig. 2 Schematic of Charge pump using MOSFETs.

The output resistance [16], [18] can be calculated as given below

$$R_{OUT,min} = \frac{1}{fC} + \frac{1}{2} fC_{OUT} \tag{1}$$

$$R_{OUT,max} = \frac{1}{fC} + \frac{1}{fC_{OUT}} \tag{2}$$

$$R_{OUT,avg} = \frac{1}{fC} + \frac{3}{4} fC_{OUT} \tag{3}$$

Considering the effect of N stages [16] and also the effect of parasitic [18] capacitance, R_{out} is given as below.

$$R_{OUT,avg} = \frac{N}{fC(1+\beta)} + \frac{3}{4} fC_{OUT} \tag{4}$$

Where “ β ” is given as the ratio of parasitic capacitance (C_p) to that of the pumping capacitance (C).

$$\beta = \frac{C_p}{C} \tag{5}$$

To achieve our validations, these effects must be considered. Further improvement has been done regarding the performance under capacitive load [18].

The power efficiency [18] is also a factor considered while designing a charge pump. The power efficiency is given as below.

$I_{DM6, \min}$ needs to be set accordingly for transistors M3, M4 and M5. The equation is given by:

$$I_{DM6, \min} = \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L}\right) (V_{GS} + V_{TP})^2 \quad (2)$$

The Voltage Controller is shown in Fig. 4. The voltage controller (VC) has been added at each stage. Charge pump using VC is [12] shown in Fig. 5. The VC is used to control the gate biasing voltage.

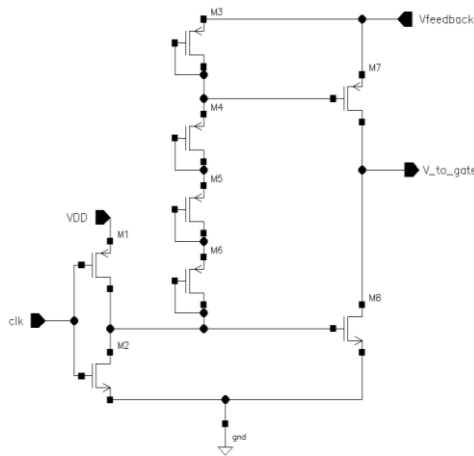


Fig. 4 Schematic of Voltage Controller.

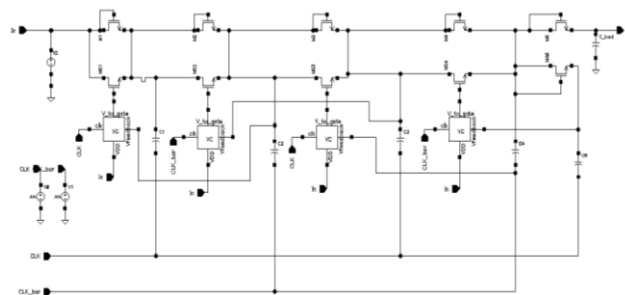


Fig. 5 Schematic of Charge pump using static CTS with VC.

The switch M5 is having the threshold voltage drop presented in [12]. To eliminate this voltage drop across M5 switch, cross coupled (CC) stage at the output is connected. The circuit diagram for cross couple charge pump is shown in Fig. 6. The circuit diagram for the charge pump using CTS with VC and CC is shown in Fig. 7.

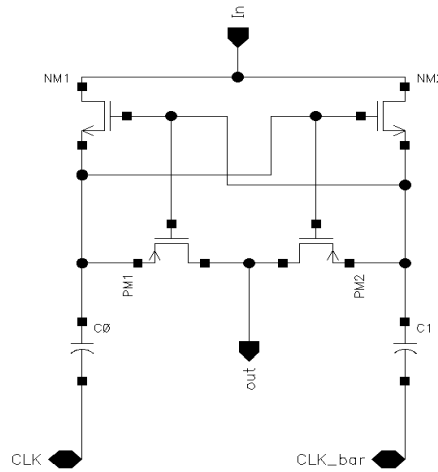


Fig. 6 Schematic of Cross Coupled charge pump.

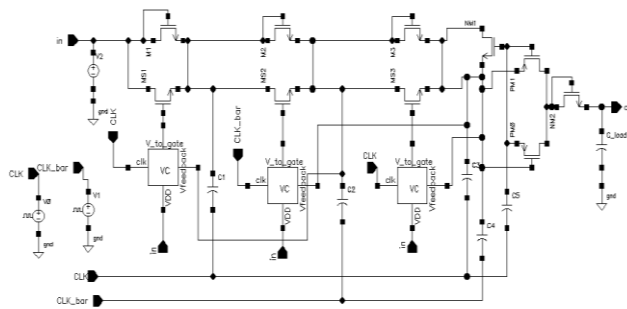


Fig. 7 Schematic of Charge pump using static CTS with VC and CC.

The reverse charge sharing problem can also be overcome by using auxiliary PMOS and [13] NMOS switches. Circuit diagram of charge pump using dynamic CTS is shown in Fig. 8. The shunted switches are further controlled by an inverter made up of PMOS and NMOS. By using auxiliary [13] switches the gate terminal can be properly shut off. Hence the reverse charge sharing effect has been eliminated.

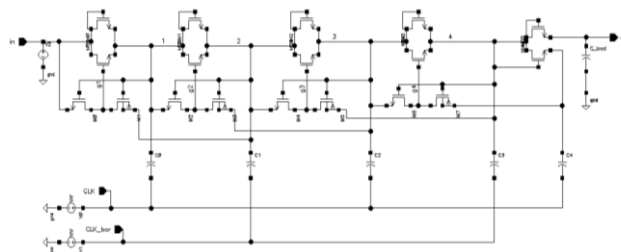


Fig. 8 Schematic of Charge pump using dynamic charge transfer switch.

C. Single Clock Charge Pump

The basic block circuit diagram is shown in Fig. 9. PM1 is in diode configuration [15]

mode. The bulk connections has also to be properly maintained. So the output voltage for the first stage [15] is given as below.

$$V_{n2prev} = V_{NM1} + V_{PM1} - V_{dsNM2} - V_t \tag{1}$$

$$V_{out} = V_{in} - V_{dsPM2} + V_{n2prev} \tag{2}$$

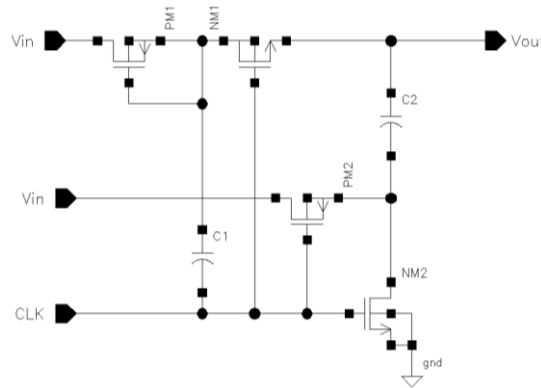


Fig. 9 Schematic of Single clock charge pump basic block.

V_{n2prev} is the voltage stored [15] in a capacitor when CLK is high. This equation also provides the gain of a single stage charge pump. The circuit diagram for two stage charge pump is shown in Fig. 10.

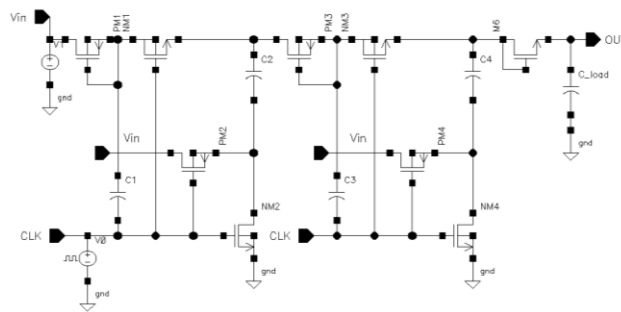


Fig. 10 Schematic of Single clock charge pump.

V_{dsPM2} is drain to source voltage of PM2 which is used as a switch. As evident from Fig. 9, every stage of a proposed charge pump there are two parts. First one is PM1 and C1, to pump up the voltage, second part is NM2 in chain with C2 and an [15] additional PM2 is used to provide the pumped up voltage to the next stage. This has been presented in [15].

It has been observed that 2 stages of a single clock charge pump are giving equivalent results of 4-stages of the Dickson charge pump.

Fig. 11. Transistor M4 has $W=1\mu$ and $L=180\text{nm}$. Two stages for the proposed charge pump is shown in Fig. 12.

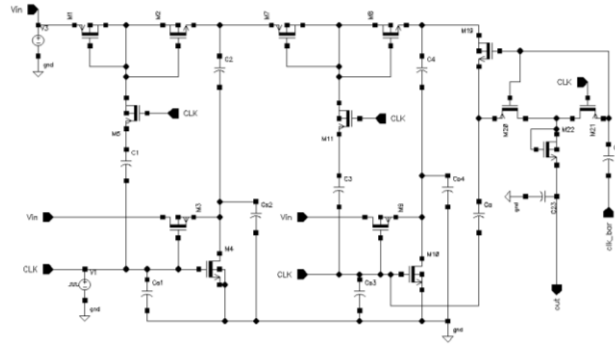


Fig. 12 Schematic of Proposed charge pump.

The output voltage is now achieving up-to the required levels. Addition of cross coupling the output stage covers its threshold voltage drops. The output equation will be given as.

$$V_{out} = (N + 1)V_{in} - V_{TNM19} \tag{2}$$

IV. RESULTS AND DISCUSSIONS

All the techniques discussed above have been simulated using $0.18\mu\text{m}$ technology in Cadence Virtuoso. The circuits has been simulated using 1MHz frequency and the applied DC input voltage is 1.8V. All the techniques discussed above have been compared with the proposed technique. Fig. 13 shows the comparison graph for output voltages.

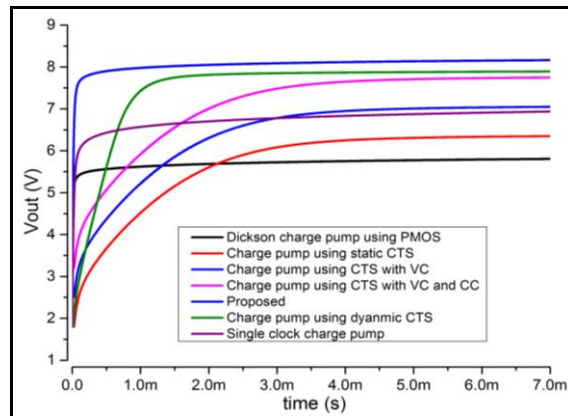
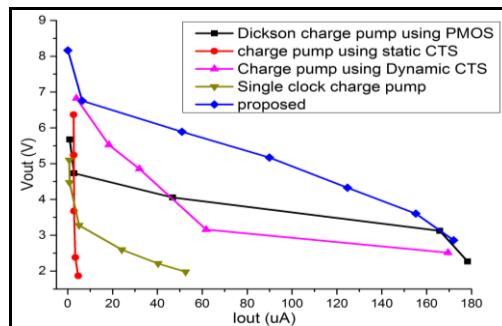


Fig. 13 Transient analysis of Charge Pumps.

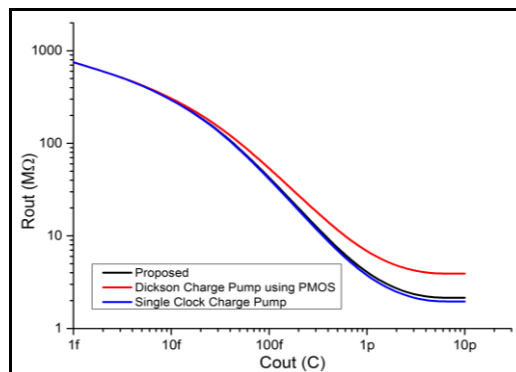
TABLE I. COMPARISON OF PARAMETERS AT 1MHZ FREQUENCY

Name	No. of stages	Output Voltage (V)	Gain G	Power Dissipation (W)
Dickson Charge Pump using PMOS	4	5.8	3.22	2.34 μ
Charge pump using static CTS	4	6.4	3.55	6.54m
Charge pump using static CTS with VC	4	7.0	3.89	4.6m
Charge pump using static CTS with VC and CC	4	7.7	4.28	4.35m
Charge pump using dynamic CTS	4	7.8	4.33	1.292m
Single clock charge pump	2	6.9	3.88	2.077m
Proposed charge pump	2	8.2	4.56	686.7 μ

From the comparison graph it's clear that the proposed charge pump is more efficient. As its generating output voltage as 8.2V using 2 stages only. Below the V_{out} vs I_{out} curves are shown in Fig. 14 for 1pF load capacitor. The analysis for V_{out} vs I_{out} has been done using 1 MHz frequency for clk and clk_bar.

**Fig. 14 V_{out} vs I_{out} .**

The comparison graph for R_{out} vs C_{out} is shown in Fig. 15. The analysis has been done using different load capacitors but with same 1 MHz frequency.

**Fig. 15 R_{out} vs C_{out} .**

The comparison graphs for gain (G) and Power Dissipation are shown in Fig. 16 and Fig. 17 respectively. The analysis for gain has been done for 1 MHz frequency with 1pF load capacitor.

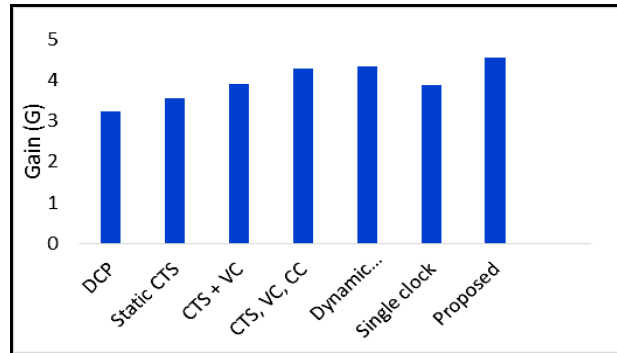


Fig. 16 Comparison of Gain for different charge pumps.

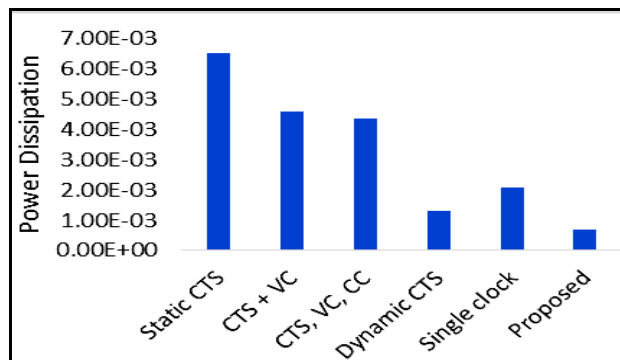


Fig. 17 Power consumption analysis for different charge pumps.

Response of output voltage at different loads is shown below in Figure 18.

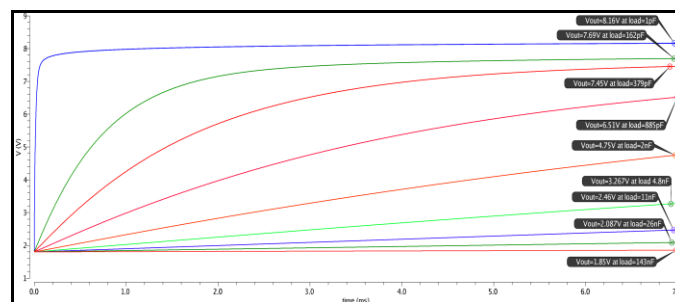


Fig. 18 Proposed charge pump output for different capacitive loads.

Response of output voltage with different input frequencies is shown below in Fig. 19.

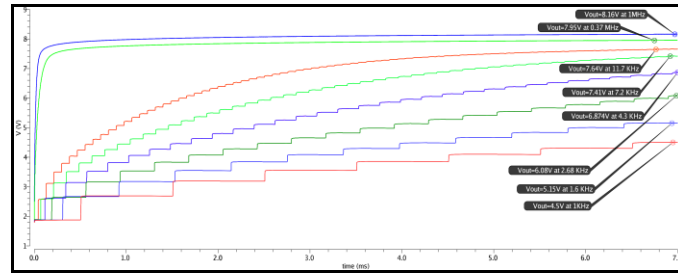


Fig. 19 Proposed charge pump output voltage for different input frequencies.

The efficiency curve of the proposed charge pump is shown below in Fig. 20. The graph is showing the curve between efficiency and the load current. The efficiency curve has been considered from different load and current values.

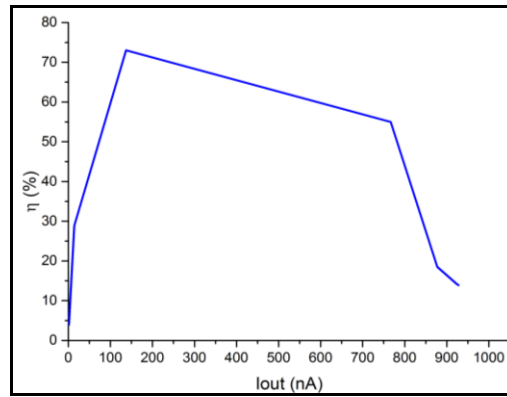


Fig. 20 Efficiency vs Iout.

We have performed the corner analysis of proposed circuit to check its performance at all the process corners. The circuit has been processed at 5 different corners available in gpdk 180 kit. As show in table 2. As evident from Fig. 22, output voltage is maximum when transistors are operating in SF corners. Similarly Fig. 21 demonstrates that the power dissipation is maximum when transistors are operating in FF corners.

TABLE II. PROCESS CORNERS IN GPDK180

NMOS	PMOS	Corner
Typical	Typical	stat
fast	Fast	FF
Slow	Slow	SS
Slow	Fast	SF
Fast	Slow	FS

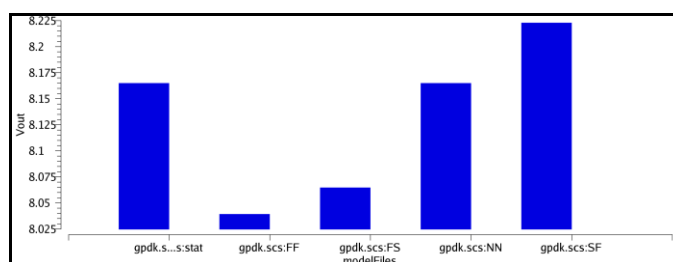


Fig. 21 Corner analysis demonstrating output voltage of proposed charge pump.

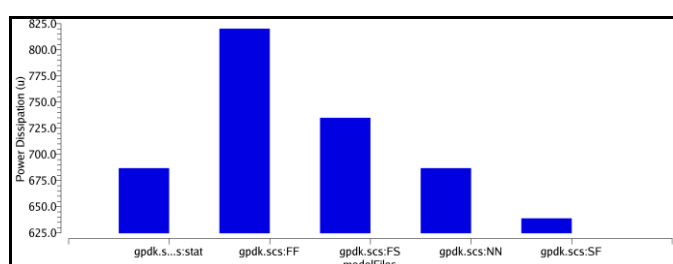


Fig. 22 Corner analysis demonstrating power dissipation of proposed charge pump.

V. CONCLUSION

To increase the efficiency of the charge pump, two methods were introduced. One of the methods was the replacement of the PN junction diodes by high voltage MOSFETs and the other being cross-coupled stage at the output. Simulations and analysis have confirmed that the output voltage of the proposed charge pump is 8.16V at 1.8V input supply voltage and 1MHz frequency. An accurate analysis for designing a charge pump has been provided for various design constraints like frequency, capacitance and the output resistance. The proposed charge pump shows better results at different load capacitances and frequencies. The efficiency of the proposed charge pump is higher than the other current charge pumps. Moreover, it can be used for high voltage generation by using multiple stages.

REFERENCES

- [1] Richelli, A.; Mensi, L.; Colalongo, L.; Kovacs, Z.; Rolandi, P.L., "A 1.2V-5V High Efficiency CMOS Charge Pump for Non-Volatile Memories, " *IEEE International Symposium on Circuits and Systems, ISCAS 2007*, pp. 2411-2414, 27-30 May 2007.
- [2] Makowski, M.S., "Realizability conditions and bounds on synthesis of switched-capacitor DC-DC voltage multiplier circuits, " *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol.44, no.8, pp. 684-691, Aug 1997.

- [3] Vinko, Davor, Tomislav Svedek, and Vanja Mandrić, "Modification of the Dickson charge pump clocking scheme for improved performance under capacitive load, " *31st international convention on information and communication technology, electronics and microelectronics*, MIPRO, 2008.
- [4] Yamazoe, Takanori, Hisanobu Ishida, and Yasutaka Nihongi, "A charge pump that generates positive and negative high voltages with low power-supply voltage and low power consumption for non-volatile memories, " *IEEE International Symposium on Circuits and Systems*, ISCAS, pp. 988-991, IEEE, 2009.
- [5] Hoque, M. R., T. Ahmad, T. R. McNutt, H. A. Mantooth, and M. M. Mojarradi, "A technique to increase the efficiency of high-voltage charge pumps, " *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 5, pp. 364-368, 2006.
- [6] Shin, Jongshin, In-Young Chung, Young June Park, and Hong Shick Min, "A new charge pump without degradation in threshold voltage due to body effect [memory applications], " *IEEE Journal of Solid-State Circuits*, vol. 35, no. 8, pp. 1227-1230, 2000.
- [7] Ker, Ming-Dou, Shih-Lun Chen, and Chia-Shen Tsai, "Design of charge pump circuit with consideration of gate-oxide reliability in low-voltage CMOS processes, " *IEEE Journal of Solid-State Circuits*, vol. 41, no. 5, pp. 1100-1107, 2006.
- [8] Ansari, Muhammad Adeel, and Waqar Qiang Chen Li-Rong Zheng, "Diode based charge pump design using 0.35 μm technology, " NORCHIP, pp. 1-4, 2010.
- [9] Cataldo, G.D.; Palumbo, G., "Double and triple charge pump for power IC: dynamic models which take parasitic effects into account, " *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol.40, no.2, pp.92-101, Feb 1993.
- [10] Aaltonen, Lasse, and Kari Halonen, "On-chip charge-pump with continuous frequency regulation for precision high-voltage generation, " *Research in Microelectronics and Electronics*, PRIME 2009. Ph. D., pp. 68-71. IEEE, 2009.
- [11] Miin-Shyue Shiau; Zong-Han Hsieh; Chi-Chieh Hsieh; Han-Yuen Liu; Don-Gey Liu, "A Novel Static CTS Charge Pump with Voltage Level Controller for DC-DC Converters, " *IEEE Conference on Electron Devices and Solid-State Circuits*, EDSSC-2007, pp. 481-484, 20-22 Dec. 2007.
- [12] Shiau, M.S., et. Al., "Static gate control for charge-transfer switches in DC-DC conversion, " *15th International Conference on Mixed Design of Integrated Circuits and Systems*, MIXDES-2008, pp. 537-541, 19-21 June 2008.
- [13] Zong Han Hsieh; Nan Xiong Huang; Miin Shyue Shiau; Hong Chong Wu; Shui-Yuan Yang; Don Gey Liu, "A novel mixed-structure design for high-efficiency charge pump, " *Mixed Design of Integrated Circuits & Systems*, MIXDES-09, MIXDES-16th International Conference, pp. 210-214, 25-27 June 2009

- [14] Na Li; Zhangcai Huang; Minglu Jiang; Inoue, Y., "High efficiency four-phase All PMOS charge pump without body effects, " *International Conference on Communications, Circuits and Systems, ICCAS 2008.*, pp. 1083-1087, 25-27 May 2008.
- [15] Ansari, M.A.; Ahmad, W.; Signell, S.R., "Single clock charge pump designed in 0.35 μ m technology, " *Mixed Design of Integrated Circuits and Systems (MIXDES), 2011 Proceedings of the 18th International Conference*, pp. 552-556, 16-18 June 2011.
- [16] Cabrini, A.; Gobbi, L.; Torelli, G., "Theoretical and experimental analysis of Dickson charge pump output resistance, " *Proceedings on IEEE International Symposium on Circuits and Systems, ISCAS-2006*, no. 4, pp. 2749-2752 May 2006.
- [17] Wu, Jieh-Tsorng, and Kuen Long Chang, "MOS charge pumps for low-voltage operation, " *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 592-597, 1998.
- [18] Khouri, Osama, Stefano Gregori, Rino Micheloni, Dario Soltesz, and Guido Torelli, "Low output resistance charge pump for Flash memory programming, " *IEEE International Workshop on Memory Technology, Design and Testing*, pp. 99-104, 2001.

Authors biography

Amritpal Singh was born in Ludhiana, Punjab, India. He received his B. Tech. Degree in Electronics and Communication from Continental Institute of Engineering and Technology, Fatehgarh Sahib. Currently, he is pursuing his M. Tech. in VLSI Design from Lovely Professional University. His areas of interest are Analog and Digital VLSI Design and Low Power VLSI Circuits.



Pawandeep Kaur was born in Punjab, India. She has done her B.Tech and M.Tech in Electronics and Communication. Currently she is working as an Assistant professor in Lovely Professional University. Her areas of interest are Analog and Digital VLSI Design and Nanotechnology (QCA).



Irfan Ahmad Pindoo was born in Srinagar, Jammu and Kashmir, India. He received his B. Tech. Degree in Electronics and Communication from Islamic University of Science and Technology, Awantipora. Currently, he is pursuing his M. Tech. in VLSI Design from Lovely Professional University. His research areas are Analog and Digital VLSI Design and Low Power VLSI Circuits.