

## **Power Savings and Delay Analysis of Adiabatic Adders in Cadence 180nm CMOS Process**

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### **Abstract**

In this paper, an advanced low power method known as Adiabatic Logic is used to implement Adiabatic 4-bit Ripple Carry Adder (RCA) and Adiabatic 4-bit Carry Look ahead Adder (CLA). The technique used is Two Phase Clocked Adiabatic Static CMOS Logic (2PASCL). Circuit analysis has been done in terms of the total power dissipation and the corresponding delay of the circuit. We have compared the results of 2PASCL adder circuits with the conventional CMOS adder circuits. Simulations have been performed in CADENCE gpdk180 CMOS technology. The results prove that about 68.69% power savings in 4-bit RCA and 63.38% power savings in 4-bit RCA are possible using this technique and are hence are suitable for implementation of low power VLSI circuitry.

**Key Words**— CMOS, low power VLSI, Adiabatic circuits

## **I. INTRODUCTION**

As the semiconductor electronics has stepped in the nano-technology scale, transistor count on a single Integrated chips is also increasing proportionally. The mobile and the other portable equipments that we are using today has increased the logic and clock speeds in order to satisfy the requirements of energy efficiency. This has increased the dynamic power dissipation of the circuits. In conventional CMOS devices the techniques that were used to minimize the power dissipation were by reducing the supply voltage, switching activity and the node capacitance. Although these methods have reduced the power consumption to some extent and some other promising techniques have been developed, but adiabatic logic principle appears to be a more practical solution for reducing the dynamic power dissipation [1-4].

Adiabatic Logic Circuits are based on the energy recovery principle, in which the charging and the discharging of capacitors occurs at a very slow speed, so that small amounts of power is wasted and recycling the energy stored on their load capacitors is provided back to the vary power supply. Instead of the fixed voltage, a varying supply voltage is used here. The voltage provide also acts as a clock. The power clock given to the circuit can be a trapezoidal waveform or a sinusoidal waveform. Initially, the power clock that is given to the circuit will charge the capacitor adiabatically during the instant it is going up and when power supply is ramping down the energy stored in the load capacitor will be given back to the power supply [5-7].

Adiabatic circuits are of two types: Fully Adiabatic and Partially Adiabatic logic circuits. In case of fully adiabatic circuits, there are ideally no losses. But the circuitry required to form fully adiabatic circuits is very complex. Moreover, the designing of a power clock generator for them is a difficult task. While as, there are some non-adiabatic losses in Partially Adiabatic circuits but the circuitry required to design partially adiabatic circuits is easier. Non adiabatic losses refer to the trapping of a charge in the nodes of a circuit.

In recent years, various adiabatic logic techniques have been studied to achieve the low power goal. Some among these used trapezoidal waveform at the supply, which is difficult to generate [8-10]. QSERL uses two complementary sinusoidal signals. Few limitations of these techniques were with respect to the floating nodes, depletion of charge at the node capacitances, the fan in of the adiabatic logic gates. Also, the use of diodes in certain logic families puts a limitation on their use due to degraded output amplitude and the power dissipation of the diodes at the charging path [11-16].

In this paper, we have designed and simulated a 4-bit Ripple Carry Adder (RCA) and a 4-bit Carry Look ahead Adder (CLA) using 2PASCL topology. But before designing such large adder circuits we have designed and simulated basic gates like NOT, NAND and XOR followed by 1- bit full adder using 2PASCL technique. Then, we have compared their output with the conventional CMOS gates in terms of the power consumption.

The rest of the paper has been segmented into V sections. Section II describes the working of basic adiabatic logic circuits. Section III is about the working details of 2PASCL circuits. While as, Section IV and V are about the simulation results and

discussion and the Conclusion, respectively.

## II. PRINCIPLE OF ADIABATIC LOGIC CIRCUITS

Here we will discuss the principle of operation of adiabatic logic circuits. We shall also compare its operation with that of conventional switching.

### A. Conventional Switching

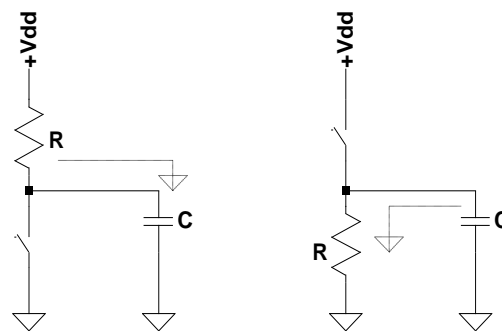
The two major sources of Power dissipation in conventional CMOS circuits are static and dynamic power dissipation. Dynamic power dissipation is due to low-to-high and high-to-low signal switching in circuits. Static power dissipation is governed by the logic states of the circuit. It does not depend on signal switching.

Static power dissipation occurs due to diode leakage currents, gate oxide leakage currents and subthreshold leakage currents. Leakage power is an important issue because it is dominating active leakage power components in deep submicron technology. The expression for the leakage power is given by

$$P_{lkg} = I_{lkg} V_{dd} \quad (1)$$

Dynamic power dissipation occurs due to the charging and discharging of capacitances. During charging the energy drawn from the power supply is equal to  $CV_{dd}^2$ . Half of this is dissipated straightaway in the PMOS transistors and its interconnect. While as, the other half is stored on the load capacitance, C. The energy stored in the capacitor gets dissipated across the NMOS and its interconnect. The short circuit power dissipation occurs because of the slow transition of an input from 0 to  $V_{dd}$  or  $V_{dd}$  to 0 volts. As a result there is a flow of a short circuit current between the supply and the ground terminal. The equivalent circuits of CMOS logic for charging and discharging is shown in Fig. 1. The expression for total power dissipation is given by

$$P_{total} = \alpha CV_{dd}^2 f_{clk} + I_{sc} V_{dd} + I_{lkg} V_{dd} \quad (2)$$



**Fig. 1. Conventional CMOS switching**

### B. Adiabatic Switching

Here we assume that the time constant of the circuit  $RC$  is much smaller than the voltage ramp period  $T$ , i.e.,  $RC \ll T$ . Hence the voltage at the capacitor closely follows the supply voltage resulting in a potential difference very close to zero across resistor  $R$ . The voltage at the capacitor  $V_c$  is also a constant ramp with slope  $V/T$  where  $V$  is the swing of the supply voltage and  $T$  is the power-clock phase period. The charging current of the adiabatic circuit is:

$$i_c = C \frac{dV_c}{dt} = \frac{CV}{T}$$

And the energy dissipated in the resistor is:

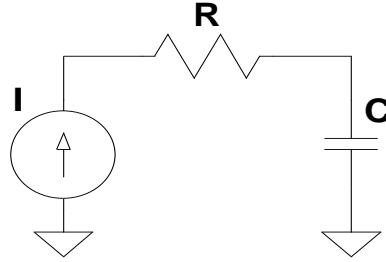
$$E = i_c^2 RT = \left(\frac{CV}{T}\right)^2 RT = \left(\frac{RC}{T}\right) CV^2$$

The equivalent circuit for discharging as shown in Fig. 2, is similar to that of charging except that the supply voltage ramps down.

Because  $RC \ll T$ , we have

$$E = \left(\frac{RC}{T}\right) CV^2 \ll \frac{1}{2} CV^2 \quad (3)$$

It means the energy stored in the capacitor is more than that dissipated by the resistor during charging or discharging. This indicates that during discharging, some energy stored in the capacitor is actually returned to the energy source.



**Fig. 2. Adiabatic Switching**

### III. 2PASCL CIRCUITS

Two phase clocked Adiabatic Static CMOS Logic (2PASCL) contains two additional transistors in the circuit. One is placed between the output node and the power clock, while as the other is adjacent to the NMOS logic circuit and connected to the other power source. In 2PASCL voltage source  $V_{dd}$  and  $V_{ss}$  are replaced by PHI and PHI\_BAR respectively, as shown in Fig. 3. It uses two complementary split-level

sinusoidal waveforms for a power clock generator. The circuit operation is divided into two phases: *evaluation* and *hold* [17-18].

**1) Evaluation phase:**

- a) When the output node Y is LOW and the PMOS tree is turned ON, CL is charged through the PMOS transistor, and hence, the output is in the HIGH state.
- b) When node Y is LOW and NMOS is ON, no transition occurs.
- c) When the output node is HIGH and the PMOS is ON, no transition occurs.
- d) When node Y is HIGH and the NMOS is ON, discharging via NMOS and D2 causes the logic state of the output to be “0”

**2) Hold phase:**

- a) When node Y is LOW and the NMOS is ON, no transition occurs.
- b) At the point when the preliminary state of the output node is HIGH and the PMOS is ON, occurs discharging via D1 occurs.

#### IV. RESULTS AND DISCUSSION

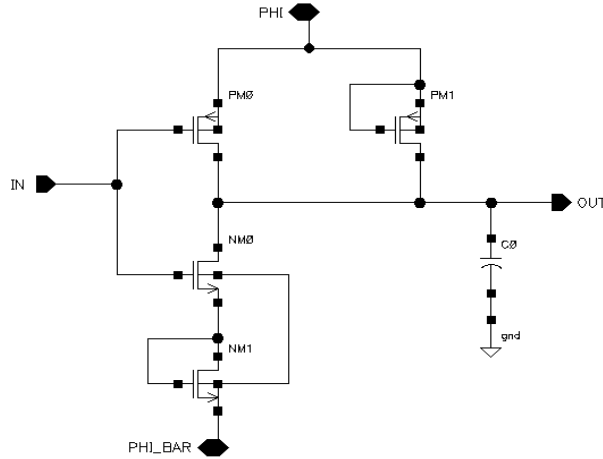
In this section, we have first examined the output logic function and the power dissipation of a simple inverter circuit. The output waveforms of the circuits are verified by performing its transient analysis. The results prove that the 2PASCL topology can reduce the power consumption by about 60% to 70% in adder circuits. Next, we have performed the parametric analysis by varying the input transition frequency from 10 MHz to 100 MHz range. It has been observed that the power savings are on an average 70%. We have designed and simulated the circuits using CADENCE VIRTUOSO and SPECTRE with 180nm CMOS technology gpdk-180 kit. The width W and the length L of NMOS and PMOS transistors are 600nm and 180nm, respectively. The supply voltage provided for the conventional CMOS circuits is 1.8 volts. Whereas, for the 2PASCL circuits the splitted sinusoidal voltage is in the form of 0 to 0.9 volts for NMOS and 0.9 to 1.8 volts for PMOS.

##### A. Inverter Circuit

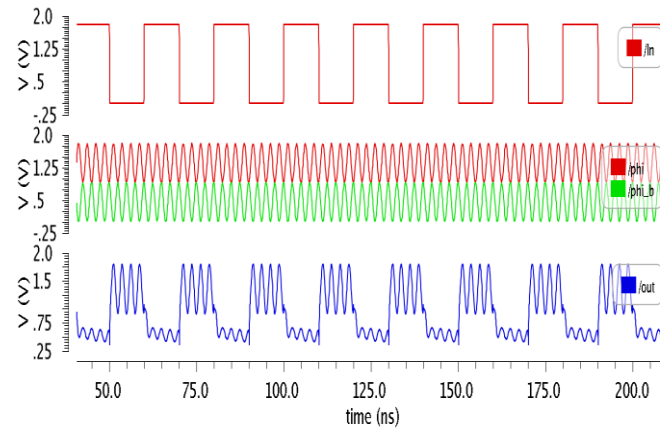
The output waveform for the splitted sinusoidal signal given at  $V_{dd}$  and ground are in the form of PHI and PHI\_BAR, as shown in Fig. 3. The frequency provided at the phase clock generator is 400MHz. Input transition frequency is kept at 50MHz for transient analysis. Output transient analysis results are given in Fig. 4.

- 1) *Comparison of Power Dissipation at different frequencies:* The parametric analysis is done by varying the input transition frequency from 10 MHz to 100 MHz range. The comparison graph shown in Fig. 5 demonstrates that with 2PASCL inverter, the power dissipation is reduced by 2.29 times in comparison to conventional CMOS circuits.
- 2) *Comparison of Power Dissipation at different Capacitive loads:* Here the transient analysis is done by varying the output load capacitance from 10fF to 500fF. The comparison graph shown in Fig. 6 demonstrates that the power

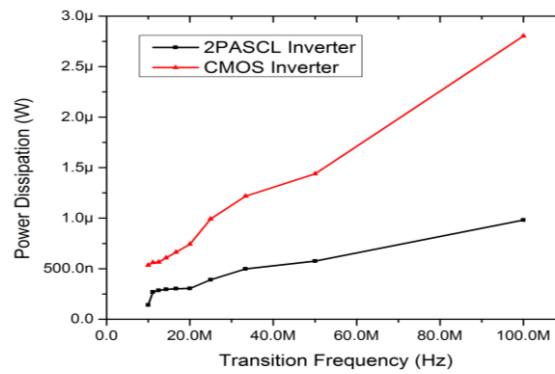
dissipation in the 2PASCL inverter is at an average 2.11 times lower than that of conventional CMOS circuits.



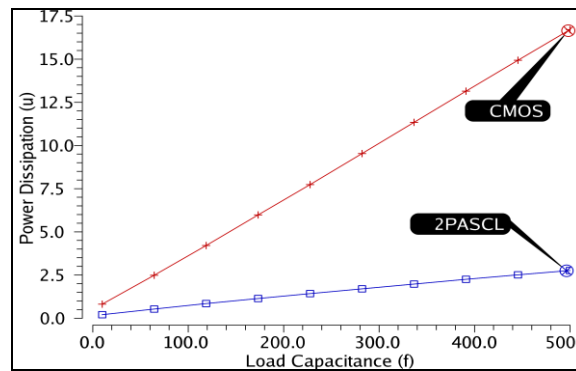
**Fig. 3. Schematic of 2PASCL Inverter.**



**Fig. 4. Transient analysis of 2PASCL Inverter.**



**Fig. 5. Comparison of power dissipation of 2PASCL and CMOS Inverter with respect to transition frequency.**

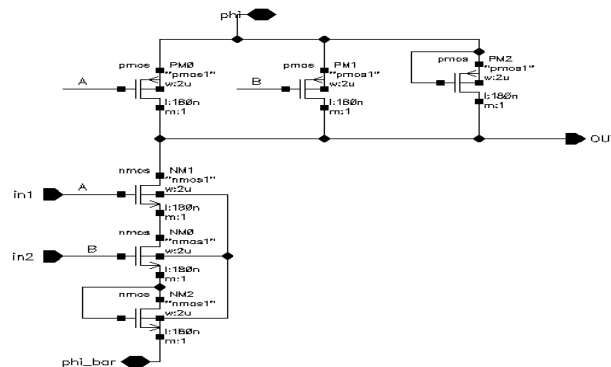


**Fig. 6. Comparison of power dissipation of 2PASCL and CMOS Inverter with respect to load capacitance.**

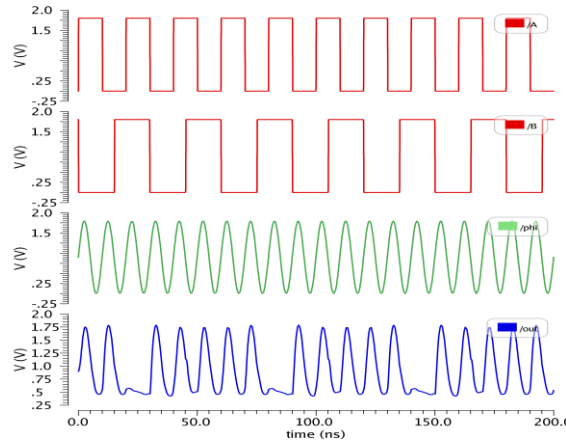
**B. Combinational Logic Circuits**

Since our main aim is to design the 4-bit adder circuits, so logic gates which are necessary for building of basic cells for the implementation of adder circuits are required. The gates designed here are 2PASCL based NAND and XOR gates.

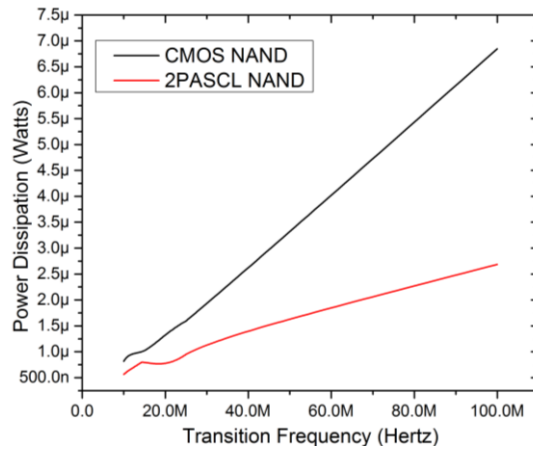
- 1) *Comparison of Power Dissipation at different frequencies:* Again transient analysis of NAND and XOR gate is done by varying the input transition frequencies from 10 MHz to 100 MHz. The schematic is shown in Fig. 7 and Fig. 11 and respective output simulation graphs are given in Fig. 8 and Fig. 12. When transient analysis is done by varying the input transition frequency of 2PASCL NAND and XOR, the power dissipation is reduced to 68.69% and 61.30% in comparison to conventional CMOS circuits as given in Fig. 9 and Fig. 13 .
- 2) *Comparison of Power Dissipation at different Capacitive loads:* The parametric analysis is done by varying the output load capacitance from 10 fF to 500fF. Comparison graphs shown in Fig. 10 and Fig. 14 demonstrate that with 2PASCL NAND and XOR, the power dissipation is reduced to 61.21% and 56.39% in comparison to conventional CMOS circuits.



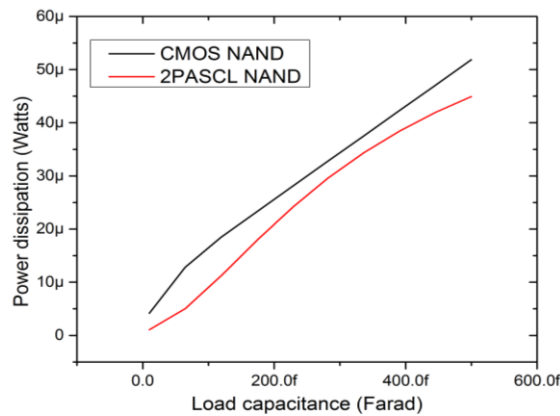
**Fig. 7. Schematic of 2PASCL NAND.**



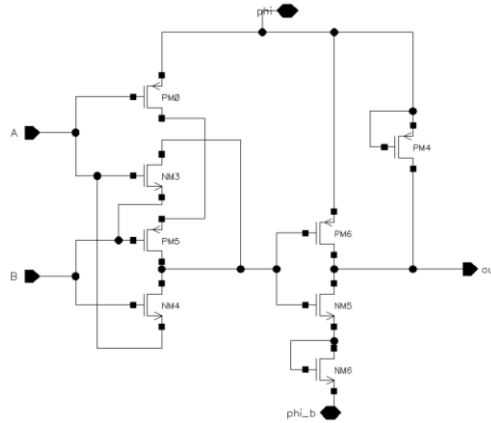
**Fig. 8. Transient analysis of 2PASCL NAND.**



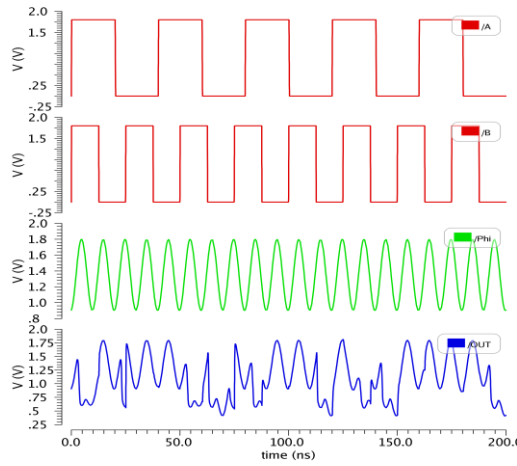
**Fig. 9. Comparison of power dissipation of 2PASCL and CMOS NAND with respect to transition frequency.**



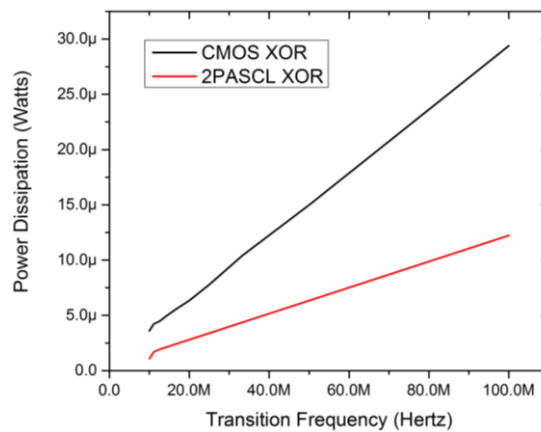
**Fig. 10 Comparison of power dissipation of 2PASCL and CMOS NAND with respect to load capacitance.**



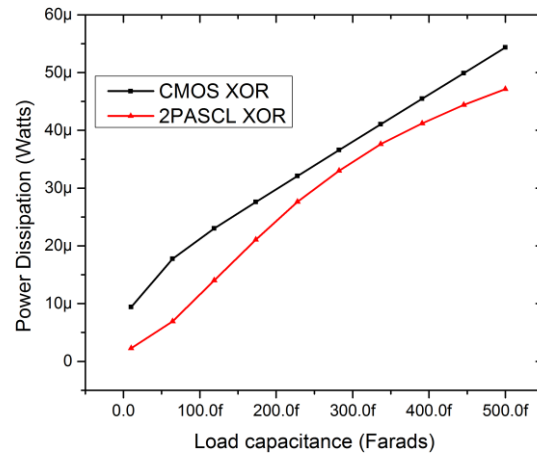
**Fig. 11. Schematic of 2PASCL XOR.**



**Fig. 12. Transient analysis of 2PASCL XOR.**



**Fig. 13. Comparison of power dissipation of 2PASCL and CMOS XOR with respect to transition frequency.**

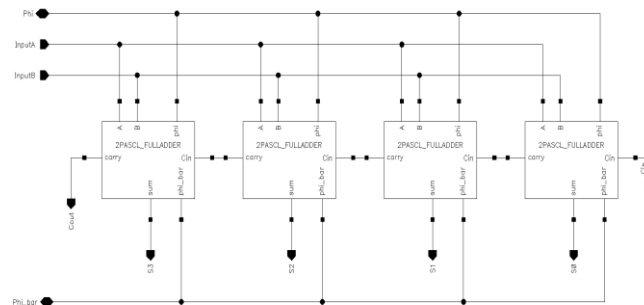


**Fig. 14. Comparison of power dissipation of 2PASCL and CMOS XOR with respect to load capacitance.**

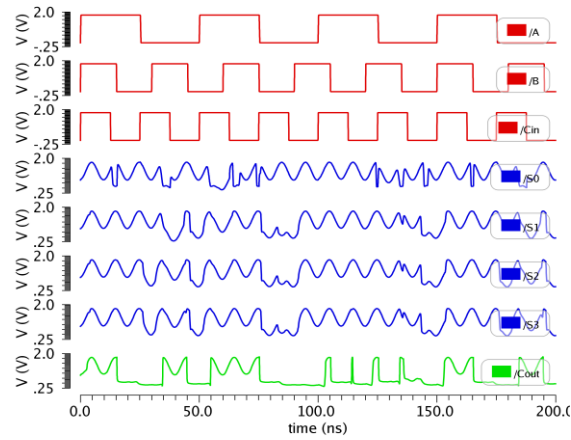
### C. 4-Bit Ripple Carry Adder

To design a 4-Bit Ripple Carry Adder, the first step is to build a 1-bit 2PASCL full adder circuit using 2PASCL XOR and NAND gates. Next level of abstraction was to use the chain of four 1-bit full adder circuits to construct 4-bit RCA. The schematic diagram of 4-bit 2PASCL RCA using 1-bit 2PASCL full adder cells is shown in Fig. 15. The output waveforms are given in Fig. 16.

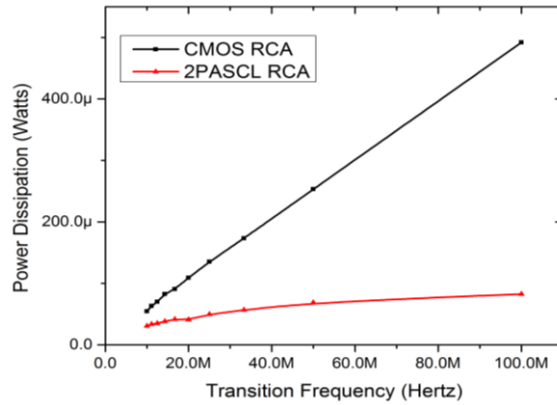
- 1) *Comparison of Power Dissipation at different frequencies:* The transient analysis is done by varying the input transition frequencies from 10 MHz to 100 MHz. Comparison graph shown in Fig. 17 demonstrates that with 2PASCL, the power dissipation is reduced to 68.69% in comparison to conventional CMOS circuits.
- 2) *Comparison of Delay analysis at different frequencies:* The delay between one of the input lines and the output signal is calculated at different frequencies by performing the parametric analysis. Comparison graph shown in Fig. 18 demonstrates that with 2PASCL RCA, the delay is degraded by 1.72 times in comparison to its corresponding conventional CMOS circuit.



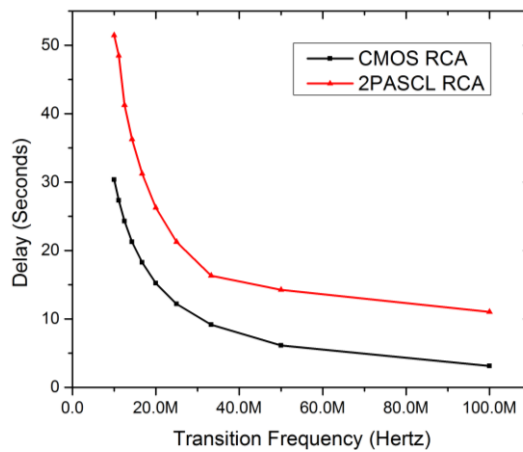
**Fig. 15. Schematic of 2PASCL Ripple Carry Adder (RCA).**



**Fig. 16.** Transient analysis of 2PASCL Ripple Carry Adder (RCA).



**Fig. 17.** Comparison of power dissipation for 2PASCL and CMOS Ripple Carry Adder (RCA) with respect to transition frequency.



**Fig. 18.** Comparison of Delay for 2PASCL and CMOS Ripple Carry Adder (RCA) with respect to load capacitance.

#### D. 4-Bit Carry Look ahead Adder

To design a 4-bit Carry Look-ahead Adder, basic building blocks needed are Carry Generator and Propagation Generator. Both these abstraction level gates require basic 2PASCL combinational gates. The problem with RCA circuits is that under the worst case scenario the carry propagates from the input to the output. So, in order to reduce the delay CLA is used. The circuit given in Fig. 19 defines two variables P and G, given by:

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

where P denotes a *carry propagate* signal and G denotes the *carry generate* signal. The output sum and carry are governed by the following expressions:

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i .$$

Thus, the equation of carry for 4-bit CLA is given by:

$$C_2 = G_1 + P_1 C_1$$

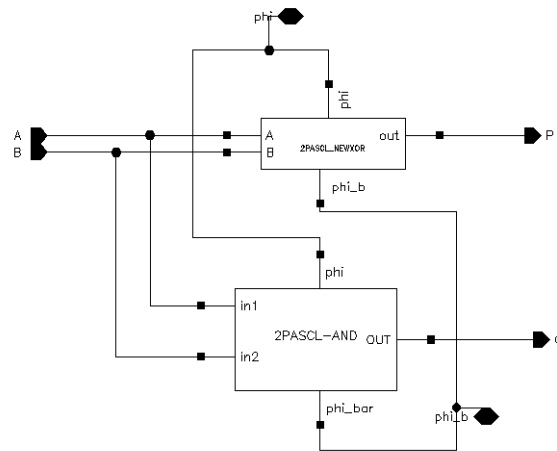
$$C_3 = G_2 + P_2 G_1 + P_2 P_1 C_1$$

$$C_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1$$

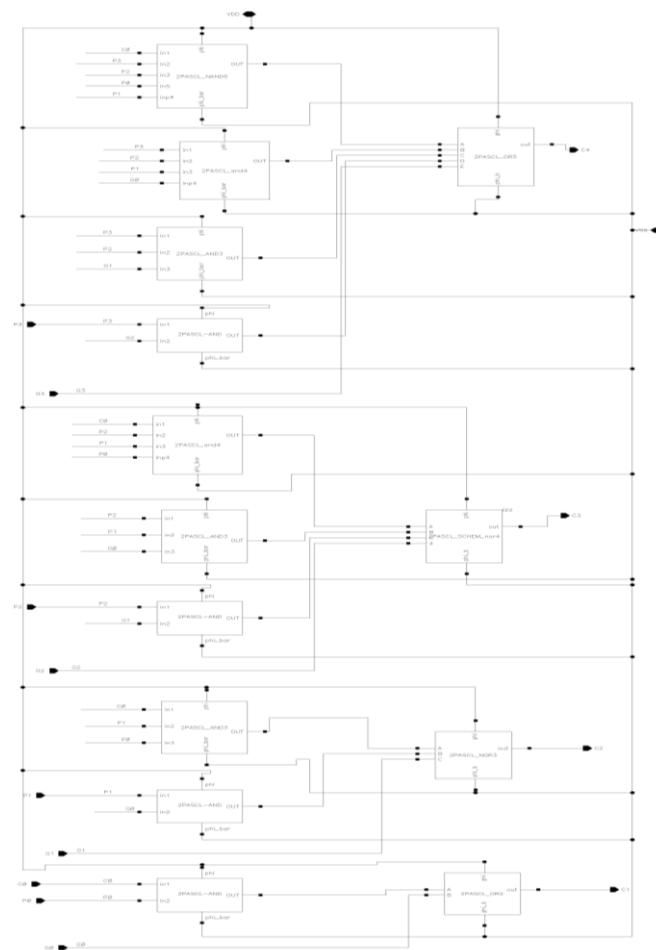
The logic diagram for carry generator is shown in Fig. 20. When P and G signals settle into their steady values, all output carries are generated after a delay of two levels of gates. Thus, the outputs  $S_2$  through  $S_4$  have equal propagation delay times.

The construction of a 4-bit parallel adder with carry look-ahead scheme is shown in Fig. 21 and the output waveforms are depicted in Fig. 22.

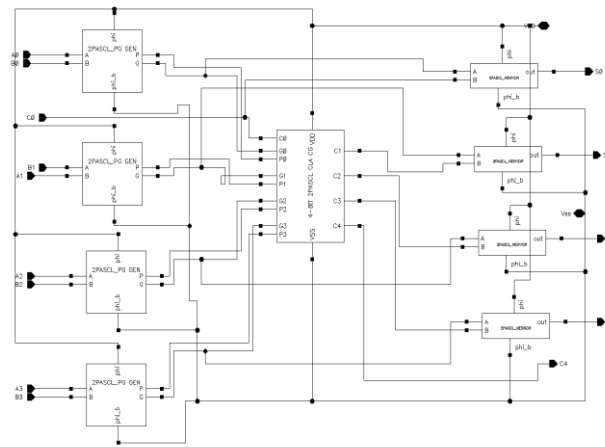
- 1) *Comparison of Power Dissipation at different frequencies:* The transient analysis is done by varying the input transition frequencies from 10 MHz to 100 MHz. comparison graph shown in Fig. 23 demonstrates that with 2PASCL, the power dissipation is reduced to 63.68% in comparison to conventional CMOS circuits.
- 2) *Comparison of Delay analysis at different frequencies:* The delay between one of the input lines and the output signal is calculated at different frequencies by performing the parametric analysis. . Comparison graph shown in Fig.24 demonstrates that the delay is degraded by 1.808 times with 2PASCL RCA, in comparison to conventional CMOS circuits.
- 3) *Advanced Simulations in terms of Power Dissipation.:* We have performed the corner analysis of 4-bit CLA circuit to check its performance at all the process corners. The circuit has been processed at five different corners available in gpdk 180 kit, as shown in Table. I. As evident from Fig. 25, power dissipation is maximum when transistors are operating in FF corners.



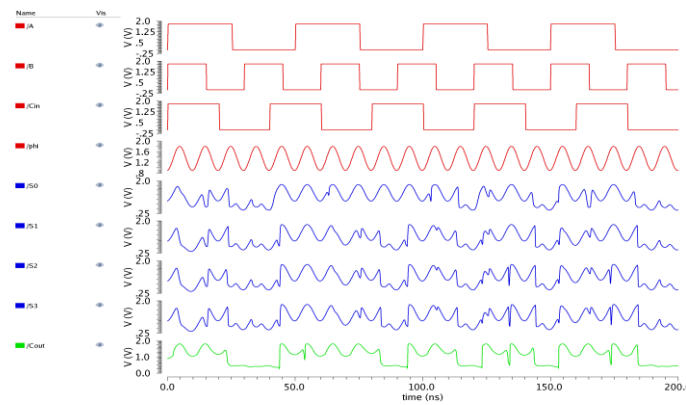
**Fig. 19. Schematic of Propagation Generator for Carry Look ahead Adder (CLA)**



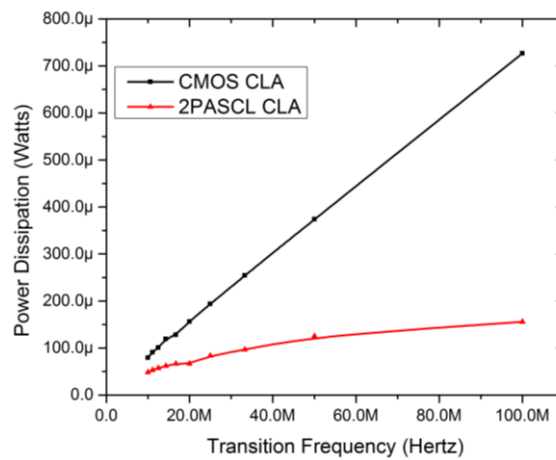
**Fig. 20. Schematic of Carry Generator for Carry Look ahead Adder (CLA)**



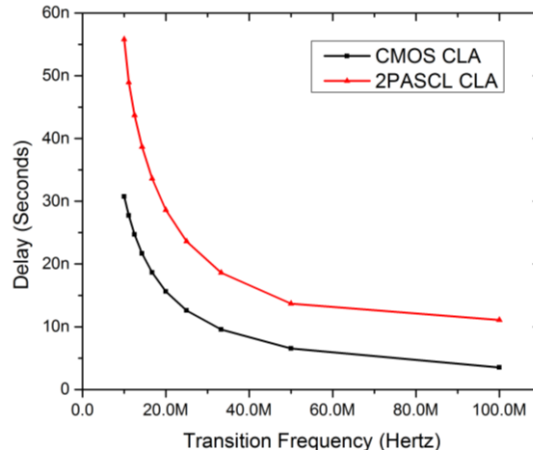
**Fig. 21. Schematic of Carry Look ahead Adder (CLA)**



**Fig. 22. Transient analysis of 2PASCL Carry Look ahead Adder (CLA).**



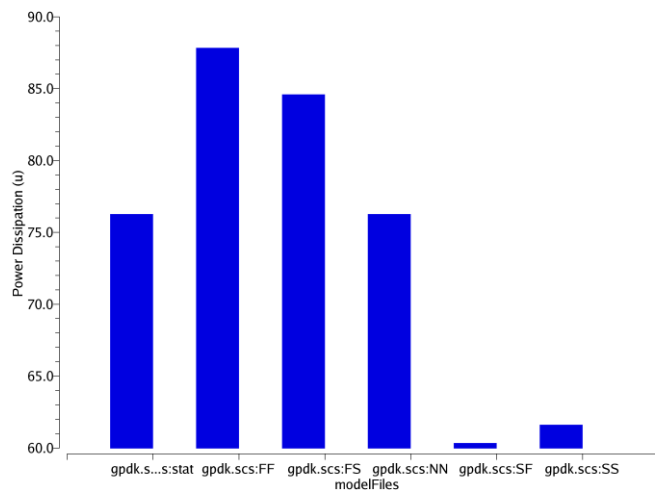
**Fig. 23 Comparison of power dissipation for 2PASCL and CMOS Carry Look ahead Adder (CLA) with respect to transition frequency.**



**Fig. 24. Comparison of Delay for 2PASCL and CMOS Ripple Carry Adder (CLA) with respect to transition frequency.**

**Table I. PROCESS CORNERS IN GPDK180**

NMOS	PMOS	Corner
Typical	Typical	stat
fast	Fast	FF
Slow	Slow	SS
Slow	Fast	SF
Fast	Slow	FS



**Fig. 25. Corner Analysis demonstrating Power Dissipation of 4-Bit 2PASCL Carry Look ahead Adder (CLA).**

The summarized values of the different parameters for input transition frequency of 10 MHz and the load capacitance of 0.01pF for an inverter and the basic

combinational gates are given in Table II. For RCA and CLA circuits, the power dissipation and the delay are summarized in Table III.

**TABLE II. POWER DISSIPATION RESULTS FOR BASIC GATES**

Gates	Power dissipation v/s Frequency ( $\mu\text{W}$ )		Power Dissipation v/s Load Capacitance (pF)	
	CMOS	2PASCL	CMOS	2PASCL
Inverter	0.534	0.140	2.5	0.5
NAND	0.816	0.563	4.13	1.16
XOR	3.6	1.392	8.16	3.64

**TABLE III. POWER DISSIPATION AND DELAY ANALYSIS FOR ADDER CIRCUITS**

Adder circuit	Power dissipation ( $\mu\text{W}$ )		Delay (ns)	
	CMOS	2PASCL	CMOS	2PASCL
4 bit RCA	253	68.8	6.131	14.242
4 bit CLA	374	125	6.5294	13.68

## V. CONCLUSION

In this paper we have compared various adiabatic logic gates and adder circuits with the conventional CMOS circuits. The power dissipation of the adiabatic circuits are much lesser than the CMOS circuits, even when the input transition frequency is varied from 10 MHz to 100 MHz. Results further affirm that with increasing the load capacitance from 10fF to 500fF, power dissipated by 2PASCL circuits still remain low. From the simulation results, it was verified that 4-bit 2PASCL RCA and 4-bit 2PASCL CLA techniques dissipate a minimum of 31.35% and 38.62% of the energy dissipated by a static CMOS RCA and CLA circuits. Hence they are deemed as fit for low power VLSI circuitry. However, the circuit delay puts some valid constraints on the topology that can be further improved.

## REFERENCES

- [1] Athas, W.C.; Svensson, L.J.; Koller, J.G.; Tzartzanis, N.; Ying-Chin Chou, E., "Low-power digital systems based on adiabatic-switching principles," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol.2, no.4, pp. 398-407, Dec. 1994
- [2] Kramer, A.; Denker, J.S.; Avery, S.C.; Dickinson, A.G.; Wik, T.R., "Adiabatic Computing with the 2n-2n2d Logic Family," *VLSI Circuits, 1994. Digest of Technical Papers., 1994 Symposium on*, vol. 25, no. 26, pp. 9-11, June 1994
- [3] G. Dickinson and J. S. Denker, "Adiabatic dynamic logic," *IEEE J. Solid-State Circuits*, vol. 30, pp. 311-315, 1995

- [4] S. G. Younis and T. F. Knight, "Asymptotically zero energy split-level charge recovery logic," *Proc. Int. Workshop Low Power Design*, pp. 177-182, 1994
- [5] Yeap, G. K. (1998). *Practical low power digital VLSI design*. Kluwer Academic Publishers.
- [6] Teichmann, P. (2011). *Adiabatic logic: future trend and system level perspective* (Vol. 34). Springer Science & Business Media.
- [7] S.Kang and Y.Leblebici (2003), *CMOS Digital Integrated Circuits – Analysis and Design*, McGraw- Hill.
- [8] Yeh, C.C.; Lou, J.H.; Kuo, J.B., "1.5 V CMOS full-swing energy efficient logic (EEL) circuit suitable for low-voltage and low-power VLSI applications," *Electronics Letters*, vol.33, no.16, pp.1375,1376, 31 Jul 1997.
- [9] Joonho Lim, Dong-Gyu Kim, Soo-Ik Chae, "A 16-bit carry-lookahead adder using reversible energy recovery logic for ultra-low-energy systems," *IEEE Journal of Solid-State Circuits*, vol.34, no. 6, pp. 898-903, Jun 1999.
- [10] Sompur, S.; Yong-Bin Kim, "An investigation into adiabatic circuits," *Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems, MWSCAS 2001*, vol.1, pp.294-297, 2001.
- [11] Yibin Ye; Roy, K., "QSERL: quasi-static energy recovery logic," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 2, pp. 239-248, Feb 2001.
- [12] Amirante, E.; Bargagli-Stoffi, A.; Fischer, J.; Iannaccone, G.; Schmitt-Landsiedel, D., "Adiabatic 4-bit adders: comparison of performance and robustness against technology parameter variations," *The 2002 45th Midwest Symposium on Circuits and Systems, MWSCAS-2002*, vol. 3, no. 3, pp. 644 - 647, 4-7 Aug. 2002.
- [13] Amirante, E.; Fischer, J.; Lang, M.; Bargagli-Stoffi, A.; Berthold, J.; Heer, C.; Schmitt-Landsiedel, D., "An ultra low-power adiabatic adder embedded in a standard 0.13/ $\mu\text{m}$  CMOS environment," *Proceedings of the 29th European Solid-State Circuits Conference, ESSCIRC-03*, vol. 599, no. 602, pp. 16-18, Sept. 2003.
- [14] Junyoung Park, Sung Je Hong; Jong Kim, "Energy-saving design technique achieved by latched pass-transistor adiabatic logic," *IEEE International Symposium on Circuits and Systems, ISCAS 2005*, vol. 5, pp.4693-4696, 23-26 May 2005.
- [15] Reddy, N.S.S.; Satyam, M.; Kishore, K.L., "Minimization of energy dissipation in glitch free and cascadable adiabatic logic circuits," *IEEE Region 10 Conference TENCN-2008*, vol. 1, no. 1, pp. 19-21, Nov. 2008.
- [16] Jing Dai, Jianping Hu, Weiqiang Zhang and Ling Wang, "Adiabatic CPL Circuits for Sequential Logic Systems," *49th IEEE International Midwest Symposium on Circuits and Systems, MWSCAS-06*, vol. 1, pp.713-717, 6-9 Aug 2006.
- [17] Anuar, N.; Takahashi, Y.; Sekine, T., "4-bit ripple carry adder of two-phase clocked adiabatic static CMOS logic: A comparison with static CMOS," *European Conference on Circuit Theory and Design, ECCTD 2009*, vol. 65, no. 68, pp. 65-68, 23-27 Aug. 2009.
- [18] Anuar, Nazrul, Yasuhiro Takahashi, and Toshikazu Sekine. "Two phase

clocked adiabatic static CMOS logic and its logic family,” *Journal of semiconductor technology and science*, vol. 10, no. 1, pp. 1-10.

- [19] Starosel skii and Victor I., “Adiabatic logic circuits: A review,” *Russian Microelectronics* vol. 31, no. 1, pp. 37-58, 2001.



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