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Low-Power Power Amplifier for 77-GHz Automotive Radars

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Abstract
In this paper we present low-power 77-GHz power amplifier (PA) for the long range automotive radar. The proposed amplifier is designed using TSMC 0.13-μm RF CMOS (f_T/f_{max}=120/140 GHz) technology, and it is powered by a 1.5-V supply. To reduce power dissipation, we consider bias voltage, transistor size optimization, matchings and layout optimization. To improve power gain of the amplifier, it has a 2-stage cascode scheme. The proposed circuit showed the lowest power dissipation of 66.45 mW and the highest saturated power gain (P_{sat}) of 23 dBm as compared to recently reported research results.

Keywords: 77-GHz, RF power amplifier, CMOS, long range automotive radar.

Introduction

The growth in wireless communication systems has rapidly resulted in a strong motivation toward developing GHz-band high performance RF (radio frequency) systems. These systems have a lot of applications such as various portable products, automotive collision avoidance radars, wireless local networks, local multi-point distribution service (LMDS), etc. The radar-based ACC (autonomous cruise control) first introduced from Mercedes-Benz in 1999 is widely available in many high and mid class automotive models. The ASV (Advanced Safety Vehicle) consists of LRR (long range radar) with coverage up to 150 meters and SRR (short range radar) with coverage up to 30 meters. In the last 15 years, silicon-based automotive radars have been investigated both by industry and academia [1]-[5]. The most commonly used frequency in W-band (75~110 GHz) transceivers is 77 GHz. Recently the 77-GHz automotive radars became popular and can be found in literature [6]-[10]. This system using W-band radar sensor offers safety functions such as pre-crash sensing and collision. Most of well-known car companies and supplies are already working on the development of the next generation vehicle known as ASV.

In this paper, we present low-power 77-GHz power amplifier (PA) for the long range automotive radar. The proposed circuit is fabricated using TSMC 0.13-μm RF CMOS process. It is powered by a 1.5-V supply. It is implemented using a 3-stage cascode scheme to improve power gain of the amplifier. We used the layout optimization technique for 77-GHz band to reduce parasitic capacitances.

Power Amplifier Analysis

Lower intrinsic gain of transistors makes it more difficult to achieve low power and high gain at very high frequency of 77GHz, so RF PA design and analysis require several novel techniques.

A. Proposed Class-A PA Design Considerations and Methodology

The proposed power amplifier (PA) is implemented using TSMC 0.13-μm RF CMOS technology. The unity current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) have 120 GHz and 140 GHz, respectively. Successful integration of the PA at 77 GHz depends on minimization parasitic capacitances and losses to maintain adequate gain, designing with low voltage swings for low breakdown devices, and achieving sufficient linearity required for spectrally efficient and variable envelope modulation scheme [11-12].

The main design goals for the 77-GHz PA are related to the PA FoM as expressed in Equation (1), which links the output power (P_{out}) with the gain (G) and power-added efficiency (PAE), while the f^2 term reflects the degradation in transistor gain and output power with the increase of frequency.

$$FoM_{PA} = P_{out} \times G \times PAE \times f^2 \qquad (1)$$

Important performance parameters of RF PA contain power gain (S21), output-referred 3rd-order intercept point ($OIP3$) to test linearity, maximum power-added efficiency (PAE) over the whole band of interest, saturated output power (P_{sat}), reverse isolation ($S12$), input/output return loss ($S11$/$S22$), power consumption and die size.

Figure 1 shows the proposed 77-GHz CMOS power amplifier. The PA consists of common-source stage with inter-stage conjugate matching operating in Class-A mode, and it is powered by a 1.5-V supply. This circuit also has 2-stage cascade structure to achieve higher gain due to the larger output impedance and the alleviated miller capacitance. We designed optimization in width and length of T-lines to supply stable DC power at the drain regions using $T_4 \sim T_6$ and $T_{10} \sim T_{12}$. Series T-line pairs T_4 and T_5, and T_{10} and T_{11} improve isolation between the each path by resonating out the parasitic capacitances at drain terminals of the second-stage and the third-stage cascade transistors which, in turn, resulting in an increase in the amplifier gain.

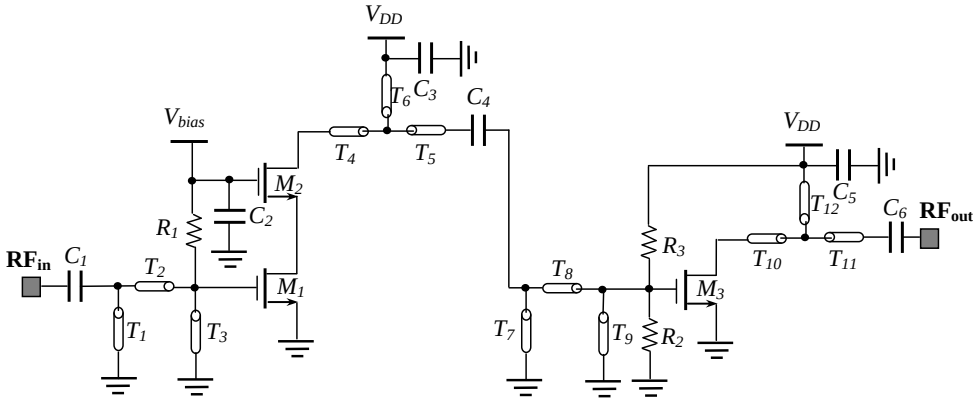

Figure 1: 77-GHz CMOS power amplifier

Results

The circuit is simulated using Agilent ADS and full-wave EM analysis is performed for all the passive structures. The speed of the bias mechanism is determined by the bias resistor and gate-source parasitic capacitor at the gate of the lower FET, and the settling time is about 4 ns based on the time-domain simulation when the input power of the PA changes from 5 to -5dBm. The amplifier is tested with a power supply of 1.5 V, and the DC current drawn with no RF input signal applied is 43.3 mA.

S-parameters (S11, S12, S21 and S22) of the amplifier in the test are plotted in Figure 2. The PA achieves an excellent peak gain (S21) of approximately 20.3 dB at 77 GHz, and the S12 indicates that the reverse isolation from the output to the input is also excellent, exceeding –36 dB in the 77 GHz. The S11 and S22 indicate how well the input and output are matched to 50 Ω, respectively. The S11 showed excellent value of -22 dB in the 77 GHz, but it was not designed for an input match to 50 Ω for the entire 74~80-GHz band. It should be noted that the requirement on S11 can be relaxed if the amplifier is integrated with the transmitter stages. Both S11 and S22 are < -5 dB in the range of 76~79 GHz.

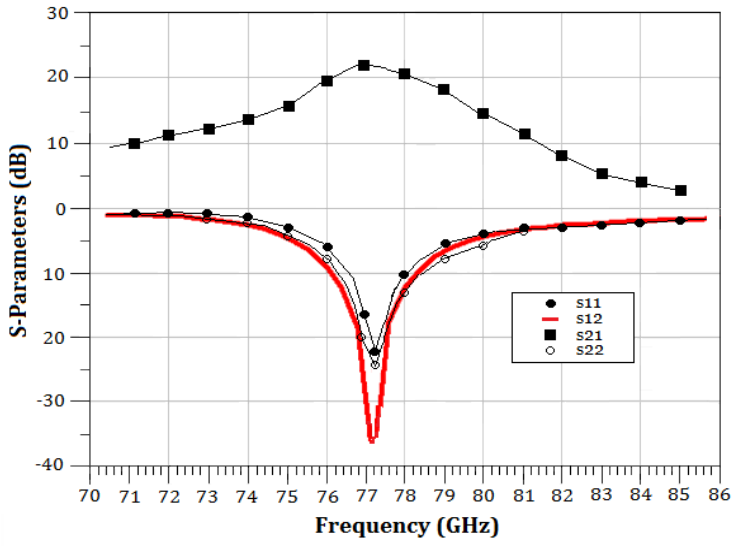

Figure 2: The results of simulated S-parameters for the PA.

Figure 3 shows power-added efficiency (PAE) and saturated output power (P_{sat}) versus input power when the amplifier is operating under saturated output power condition driven by a 14-dBm input. Maximum output power of 23 dBm (200 mW) is achieved at 77 GHz. At 77 GHz, the final gain stage of the power amplifier achieves a maximum output power density (power per source area) of 2 mW/μm^2. The PAE exceeds 6 % between 74 and 80 GHz. The amplifier has power gain of more than 20 dB from 67 to 82 GHz with 3-dB gain flatness. Over 15-dB gain at maximum output power level facilitates integration of the amplifier in a transceiver as fewer pre-driver stages are required. When biased at 21.65 mA (i.e., 50 % of 43.3 mA DC current with no RF signal applied), there is less than 3-dB reduction in output power and slightly power PAE, despite the transistor trans-conductance g_m being reduced by half for all three stages. As shown in Figure 3, the PA showed high saturated output power of 23 dBm and maximum PAE of 17 %, respectively.

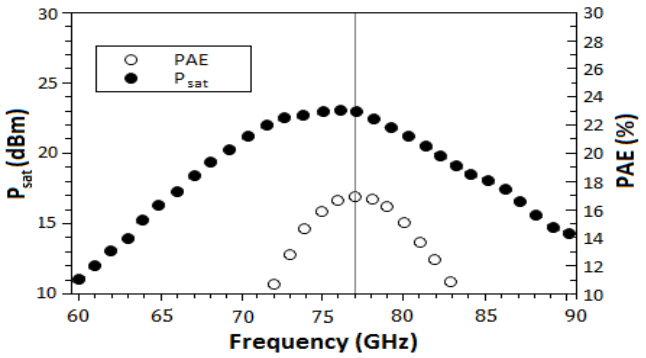

Figure 3: Saturated power(P_{sat}) and PAE versus input power.

Table 1 shows comparison results for recently reported 77-GHz power amplifiers. To test the linearity of the amplifier, a two-tone test was performed with a tone spacing of 100 MHz. As described in Table 1, the proposed circuit showed lower power dissipation of 66.45 mW, the highest saturated power gain (P_{sat}) of 23 dBm, and the lowest input/output return loss of -22 dB/-24 dB as compared to recently reported research results in [9-12].

Table 1: Comparison to recently reported 77-GHz power amplifiers.

Reference	[7]	[8]	[9]	[10]	[11]	[12]	This work
Frequency (GHz)	77	77	79	77	60	60	77
Technology (μm)	0.1 HEMT	0.065 CMOS	0.18 BiCMOS	0.12 BiCMOS	0.09 CMOS	0.09 CMOS	0.13 CMOS
P_{sat} (dBm)	20.1	12.83	NA	17.5	8.4	9.3	**23**
S11 (dB)	< -10	-16	NA	NA	< -12	< -10	**-22.0**
S22 (dB)	< -10	-17	NA	NA	< -12	< -10	**-24.0**
Power Consumption (mW)	NA	236	< 330	297	54	> 39.75	**66.45** (V_{DD}=1.5V, I_{DD}=44.3mA)

Conclusion

This paper proposed 77-GHz power amplifier with a low power for the long range automotive radar. The proposed circuit was implemented using TSMC 0.13-μm RF CMOS (f_T/f_{max}=120/140 GHz) process, and it was powered by a 1.5-V supply. The proposed CMOS power amplifier showed lower power dissipation of 66.45 mW and the highest saturated power gain (P_{sat}) of 23 dBm as compared to recently reported research results. This circuit demonstrates the potential of nanoscale CMOS for low-power applications.

Acknowledgments

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