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Advance Control of Cascaded H Bridge Multi-Level Inverter For Harmonic Mitigation: Simulation And Experimental Evaluation-I

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Abstract

One of the major problems in electric power quality is the harmonic contents. Various switching techniques have been used in static converters to reduce the output harmonic content. Multilevel inverters are increasingly being considered for high power applications because of their ability to operate at higher output voltages along with less voltage stress across switches. In this paper, harmonic mitigation is carried out using cascaded h bridge multi-level inverter. Pulse Width Modulation (PWM) techniques for multilevel inverters have been extensively used in recent years. Sinusoidal PWM (SPWM) techniques for multilevel inverters have been properly deduced from that of two-level inverter. Systematic step by step analysis of cascaded H bridge multilevel inverter has done for harmonic mitigation. Simulation is carried out in Atmel Studio and MATLAB. Results were presented for heating and induction motor application for cascaded h bridge It is observed that harmonics are mitigated for both loads at different load conditions.

Keywords: Cascaded H-Bridge, Harmonic Mitigation, MATLAB, Multi-level Inverter.

1. Introduction

Numerous industrial applications demands higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative solution in high power and

medium voltage situations. Subsequently, several multilevel converter topologies have been developed. This paper demonstrates use of the Cascaded H-bridge multilevel inverter topology. For such inverter, IGBTs and MOSFETs are used as switching devices to make the comparison with other multi-level inverter more realistic. The switches that are used for different inverters topologies are the same for all of the inverters. If the power losses are important, the 5-level diode clamped is the best choice since it has the lowest power losses between all other inverter topologies. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. The multilevel inverter reduces voltage stress; the switching frequency can be reduced for the same switching losses; the higher output current harmonics are reduced by the same switching frequency.

Multilevel inverter topologies have been proposed during the last two decades. Moreover, three different major multilevel converter structures have been reported in the literature: cascaded H-bridges converter with separate dc sources, diode clamped (neutral-clamped), and flying capacitors (capacitor clamped). Referring to the literature reviews, the cascaded multilevel inverter (CMLI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. [1], [2]. At present these inverters are highly visible in all Medium voltage drives, grid connected systems and FACTS devices. It is clear that, multilevel inverters are one of the best option for Medium and high power applications. [2], [5], [8], [9], [10], [11]. The cascaded multilevel inverter has following advantages compared to others, like the simplicity of regulation of the DC bus, modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately, the least number of components among all multilevel converters to achieve the same number of voltage levels and Soft-switching can be used in this structure to avoid bulky and lossy resistor Capacitor-diode snubbers.

2. Methodology

2.1 Multilevel Inverters

a. Multilevel inverter includes an array of power semiconductor devices and capacitor voltage sources, the output of which generates voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages to obtain high voltage at the output, while the power semiconductors have to withstand only reduced voltages.

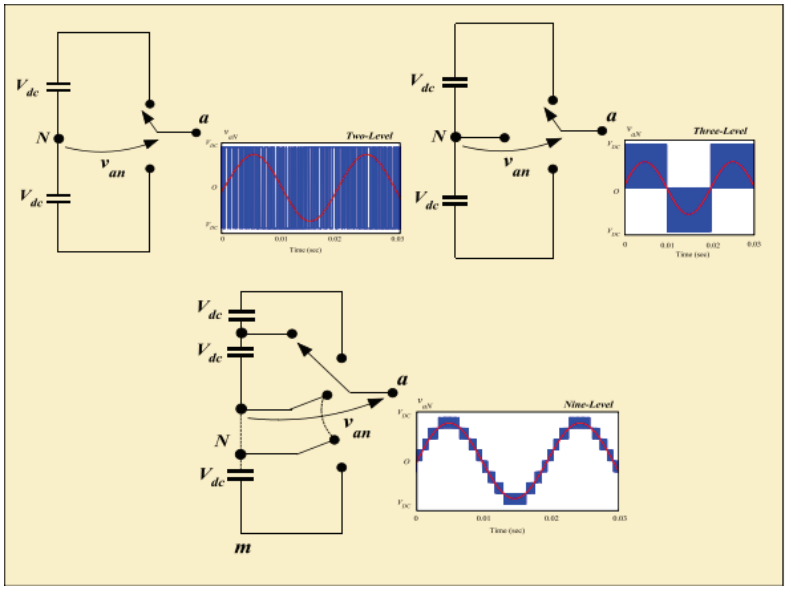

Figure 1. Inverter output voltage waveform a) two level b) three level c) n level

Fig.1. shows a schematic diagram of one phase leg of inverters with different number of levels, for which the action of power semiconductors is represented by an ideal switch with several positions. From Fig.1 we can observe a two level inverter generates an output voltage with two values (levels) with respect to negative terminal of the capacitor. While the three level inverter generates three voltages, and n-level inverter generates a n- level output voltages. In all cases this devices are not arranged in series but they are arranged in such way that, they gain the capability to generate such kind of voltages. Herein, we should remember one important thing i.e. as the number of steps increases in the output waveforms; harmonic content comes down. Thus power quality of such waveforms will increase drastically. However, in order to generate step kind of waveforms in output side, different multilevel based archetypes are successfully built and verified. But general principle of multilevel inverters is the synthesis of the ac voltage from several different voltage levels on the dc bus. As the number of voltage levels on the input dc side increases, the output voltage adds more steps. Which approach the sinusoidal wave. However, from above thought, to present a general idea about the steps in the output waveform, consider **m** to be the number of steps of the phase voltage with respect to the negative terminal of the inverter, and then the number of steps in the voltage between two phases of the load K is given by equation 1.1and 1.2

$$K = 2m+1 \quad (1.1)$$

And the number of steps P in the phase voltage of a three phase load in wye connection is

$$P = 2k -1 \quad (1.2)$$

The term multilevel starts with the three-level inverter introduced by the Nabae et al. However topologically, multilevel inverters are largely divided into many configurations. The most common multilevel
Converter topology is Cascade H-Bridge (CHB) Multilevel inverter.

2.2 Cascaded Multilevel Inverter (CMLI)

Cascaded H-Bridge (CHB) configuration has recently become very popular in high power AC supplies and adjustable-speed drive applications. A cascade multilevel inverter consists of a series of H-bridge (single-phase full bridge) inverter units in each of its three phases. Each H-bridge unit has its own dc source, which for an induction motor would be a battery unit, fuel cell or solar cell. Each SDC (separate DC source) is associated with a single phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. Through different combinations of the four switches, S1-S4, each converter level can generate three different voltage outputs, +Vdc, -Vdc and zero. The AC outputs of different full bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters (i.e. diode clamped and flying capacitor). In this topology, the number of output-phase voltage levels is defined by m= 2N+1, where N is the number of DC sources. A seven-level cascaded converter, for example, consists of three DC sources and three full bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels. Each H- bridge unit generates a quasi-square waveform by phase shifting its positive and negative phase legs‟ switching timings. Each switching device always conducts for 180° (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method makes all of the switching devices current stress equal. In the motoring mode, power flows from the batteries through the cascade inverters to the motor. In the charging mode, the cascade converters act as rectifiers, and power flows from the charger (ac source) to the batteries. The cascade converter scan also acts as rectifiers to help recover the kinetic energy of the vehicle if regenerative braking is used. The cascade inverter can also be used in parallel HEV configurations. This new converter can avoid extra clamping diodes or voltage balancing capacitors.

The combination of the 180° conducting method and the pattern-swapping scheme make the cascade inverters voltage and current stresses the same and battery voltage balanced. Identical H-bridge inverter units can be utilized, thus improving modularity and manufacturability and greatly reducing production costs. Battery-fed cascade inverter prototype driving an induction motor at 50% and 80% rated speed both the voltage and current are almost sinusoidal. Electromagnetic interference (EMI) and common mode voltage are also much less than what would result from a PWM inverter because of the inherently low dv/dt and sinusoidal voltage output.
The main advantages of using the cascade inverter in an induction motor include:
(1) It makes induction motor more accessible/safer and open wiring possible for most of an induction motor power system.

(2) Traditional 230 V or 460 V motors can be used, thus higher efficiency is expected as compared to low voltage motors.
(3) No EMI problem or common-mode voltage/current problem exists.
(4) Low voltage switching devices can be used.
(5) No charge unbalance problem exists in both charge mode and drive mode.

Cascade inverters are ideal for an induction motor that has many separate dc sources (batteries) available for the individual H-bridges, these inverters are not an option for series hybrid induction motors because cascade inverters cannot be easily connected back-to-back. For series-configured induction motors where an onboard combustion engine generates ac power via an alternator or generator, a multilevel back-to-back diode clamped converter drive can best interface with the source of ac power and yet still easily meet the high power and/or high voltage requirements of the induction motor.
Induction motors generally have an ac voltage source from an alternator or combustion-engine generator. A rectifier converts this ac voltage to dc for the electric energy storage devices on board – batteries or ultra-capacitors. An inverter converts the dc voltage to variable voltage variable frequency ac in order to drive the main induction motor.
The multilevel converter can act as an inverter in drive mode when energy is being sent to the motor that drives the wheels and as a rectifier during regenerative braking or during charge mode when the vehicle is plugged into an external ac source.
The reduction in dv/dt can prevent motor windings and bearings from failure. The staircase output voltage waveform approaches a sine wave, thus having no common-mode voltage and no voltage surge to the motor windings.
A cascaded multilevel inverter is discussed to eliminate the excessively large number of
(1) Bulky transformers required by conventional multi pulse inverters,
(2) Clamping diodes required by multilevel diode-clamped inverters, and
(3) Flying capacitors required by multilevel flying-capacitor inverters.
Also, it has the following features:
1.It is much more suitable to high-voltage, high-power applications than the conventional inverters.
2. It switches each device only once per line cycle and generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.
3. Since the inverter structure itself consists of a cascade connection of many single-phase, full bridge inverter (FBI) units and each bridge is fed with a separate DC source, it does not require voltage balance (sharing) circuits or voltage matching of the switching devices.
4. Packaging layout is much easier because of the simplicity of structure and lower component count.
5. Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor- diode snubbers.

These advantages are our motivation to work on the harmonic analysis of cascaded five-level induction motor drives.

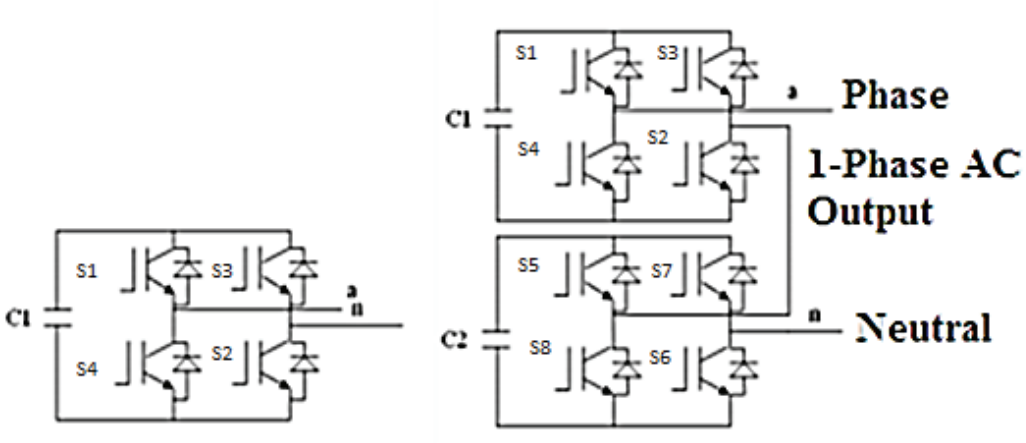

Figure 2. Single Phase Structures of Cascaded Inverter (a) 3-level, (b) 5-level.

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975 [7]. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of VAR can simply increase without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMLI topology is essentially composed of three identical phase legs of the series-chain of H bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

The converter topology is based on the series connection of single-phase inverters with separate dc sources. Fig. 2 shows the power circuit for one phase leg of a three-level, five level and seven-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This

is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc with five-level and -3Vdc to +3Vdc with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering.

Table-1: Switching State of the Five- Level Cascaded Multilevel Inverter.

Voltage V_{ao}	Switch State							
	S1	S2	S3	S4	S5	S6	S7	S8
V_{dc}	1	1	0	0	1	1	0	0
Vdc/2	1	1	0	0	0	1	0	1
0	0	0	0	0	0	0	0	0
-Vdc/2	0	1	0	1	0	0	1	1
-Vdc	0	0	1	1	0	0	1	1

3. Proposed Cascaded H Bridge Multi-Level Inverter

The controller used to provide switching signals to all eight switches (IGBT) so as to control speed and toque is shown in figure 4. Switching signals are generated by microcontroller Arduino Mega -ATMEGA 2560 with ability to program with i/o digital and analog pins with operating at very high speed approaching 1 MIPS per MHz. Inbuild PID controller is used to generate error for speed which will act as modulating signal for generation of pulses by inphase deposition SPWM. Program is written in ATMEL Studio and loaded in microcontroller Arduino Mega. Then using MCT6 optocoupler isolation of signals ae carried out and given to driver circuit of IR2110 single phase driver of International rectifier to drive IGBT used. IR2110 is capable of driving one leg (upper and lower) of H-bridge as seen in figure 3. However separate optocouplers are required for each switching signals. Separate 5 V power supply is required for optocoupler and 12 V supply is required for driver which can be taken from any of the single battery. The RL load is used to generate results. The program for generation of inphase deposition SPWM with PID controller is given below.

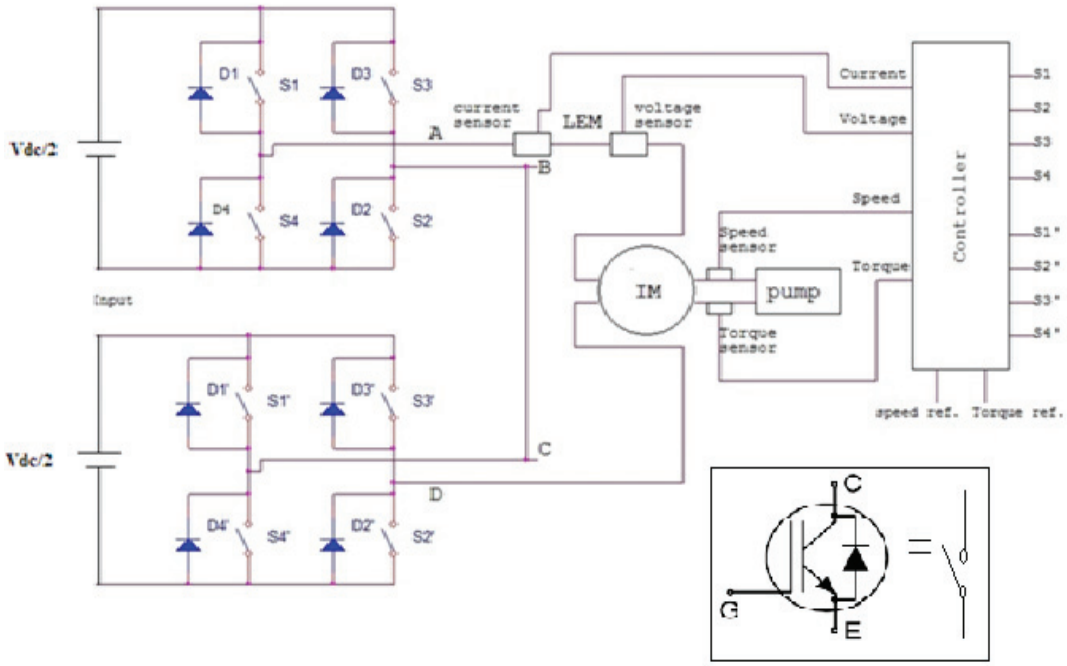

Figure 3. Circuit Diagram of 1-Phase Five Level Cascaded Multilevel Inverter Induction Motor Drives

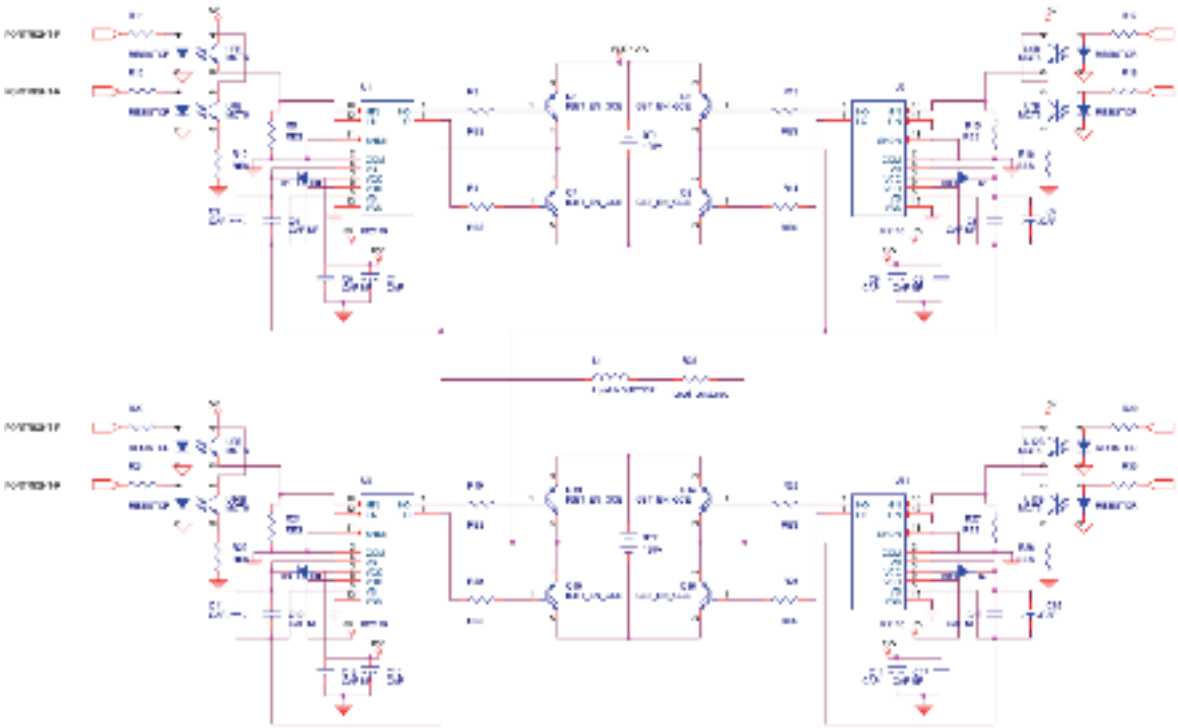

Figure 4. Control Diagram

4. Results and Discussion

This section presents the results obtained. These results are also discussed here.

4. 1. System Parameters:

Input parameters:
Vdc1 = Vdc/2= 120V,
Vdc2 = Vdc/2= 120V,
Output parameters:
Vac = 240 V,
Iac = 4.16 A,
Load = Single Phase, 1HP, 230V,1440 RPM, Induction Motor;
Simulation Tool: MATLAB

4. 2. Controller Design Parameters:

Kp = 0.0015688
Ki = 0.022212
Kd = 0.00001
Controller type: Discrete Parallel from PID
Sampling Time: $5x10^{-5}$ s
Tuning: Ziegler Nicholas Method

4. 3. PID controller results:

Model Parameters:
Vdc1 = 120V;
Vdc2 = 120V;
Motor – single phase 1hp CSCR motor;

4. 4. PID Parameters:

Kp = 0.0015688
Ki = 0.022212
Kd = 0.00001
Controller type : Discrete Parallel form PID
Sampling Time : 5x10-5 s
Tuning : Tuned by using matlab PID tuner app

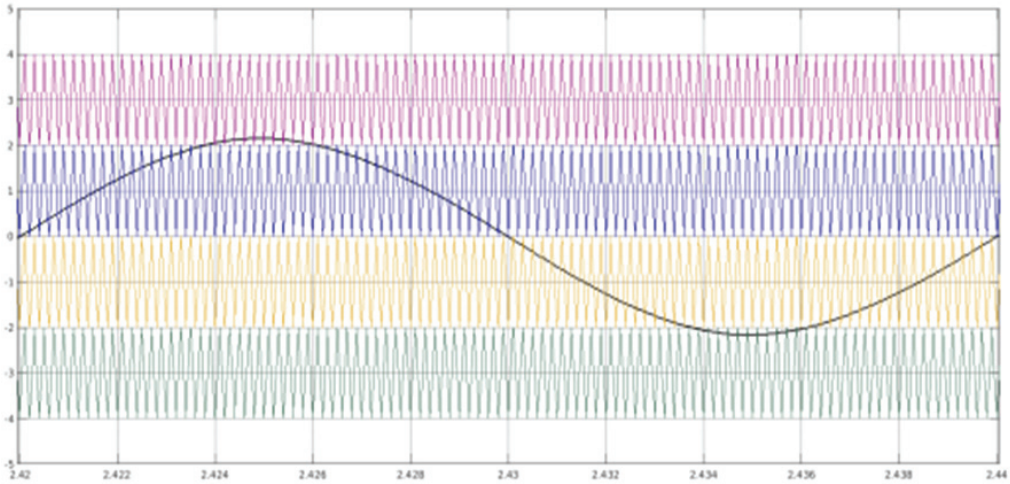

Figure 5. Triangular waves and sine wave signals used for IPD SPWM generation method.

Here 4 triangle generators are used for 4 level (zero level not considered). Switches corresponding to the level are triggered when sine amplitude is greater than triangle.

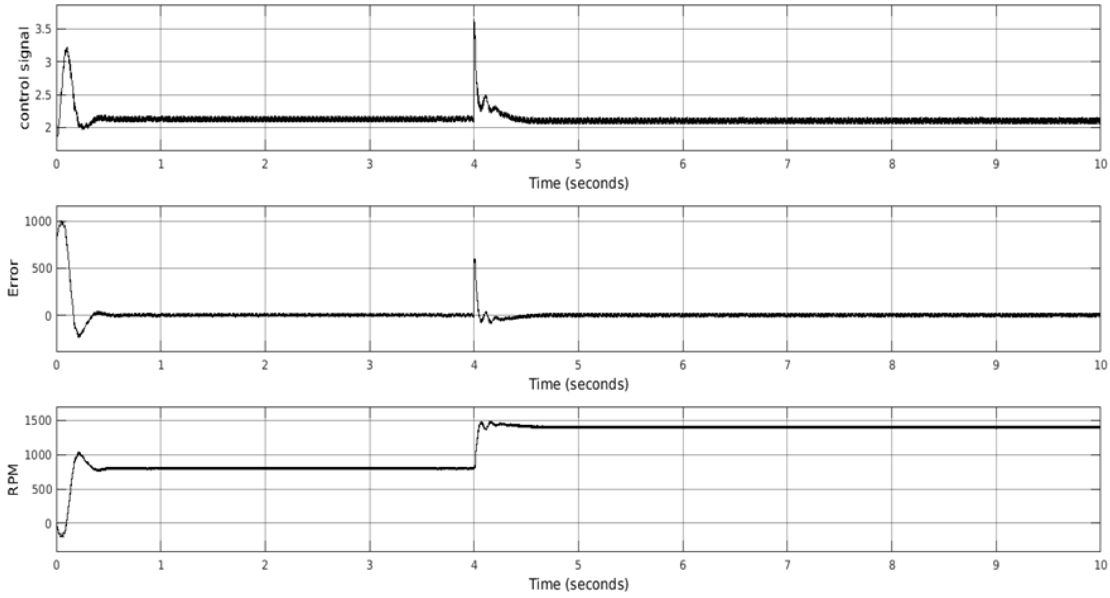

Figure 6. PID controller graphs.

In Fig. 6. (i) Represents the output control signal generated by the PID controller in order to reach set point. (ii) Is the error signal given to the PID input, which is difference between set point and actual speed. (iii) Graph of the actual motor speed in RPM, here RPM is varied in two steps. First at t=0 set point = 800 and then at t = 4 set point is 1400, hence the reference tracking can be seen with step change in set point

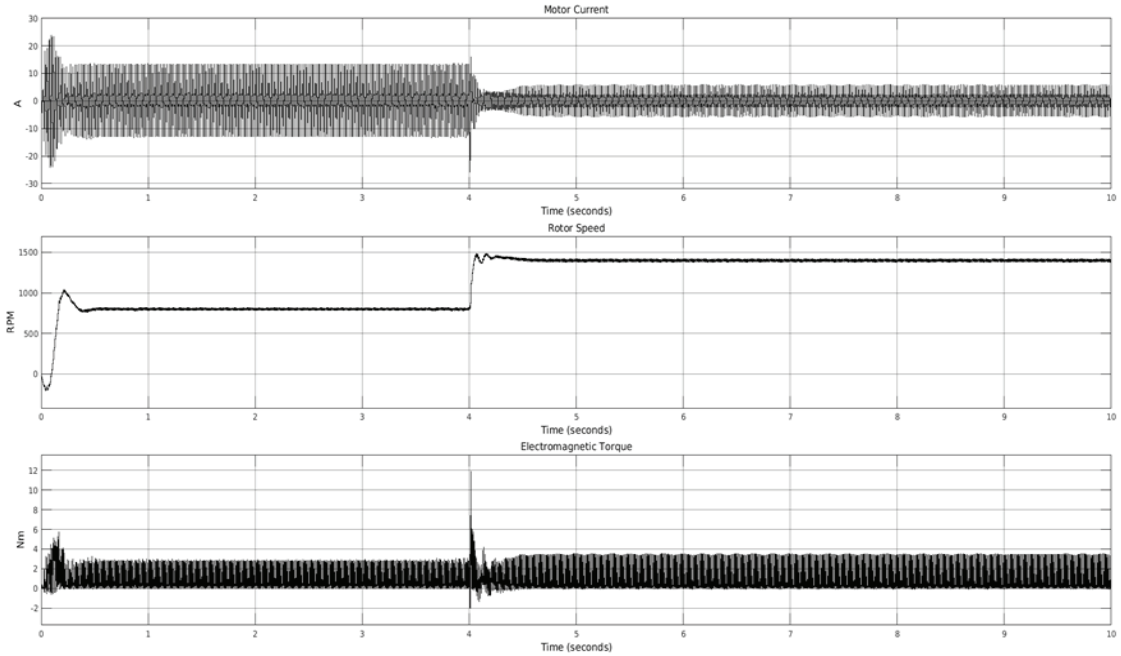

Figure 7. Motor data from measurement bus of motor block.

In Figure 7, (i) Graph of the current taken by stator winding of the motor in Amperes (ii)Rotor speed of the motor in RPM (iii) Electromagnetic torque generated on the rotor in Nm.

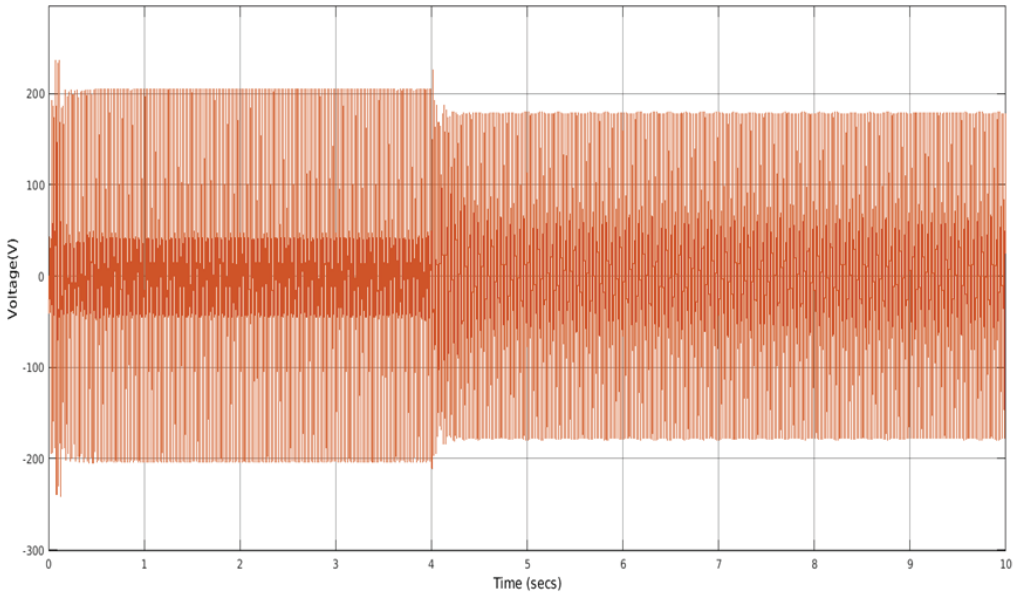

Figure 8. Voltage waveform of the five level inverter at the output of LC filters.

Next two figures show expanded view of the waveforms for different RPM's of motor.

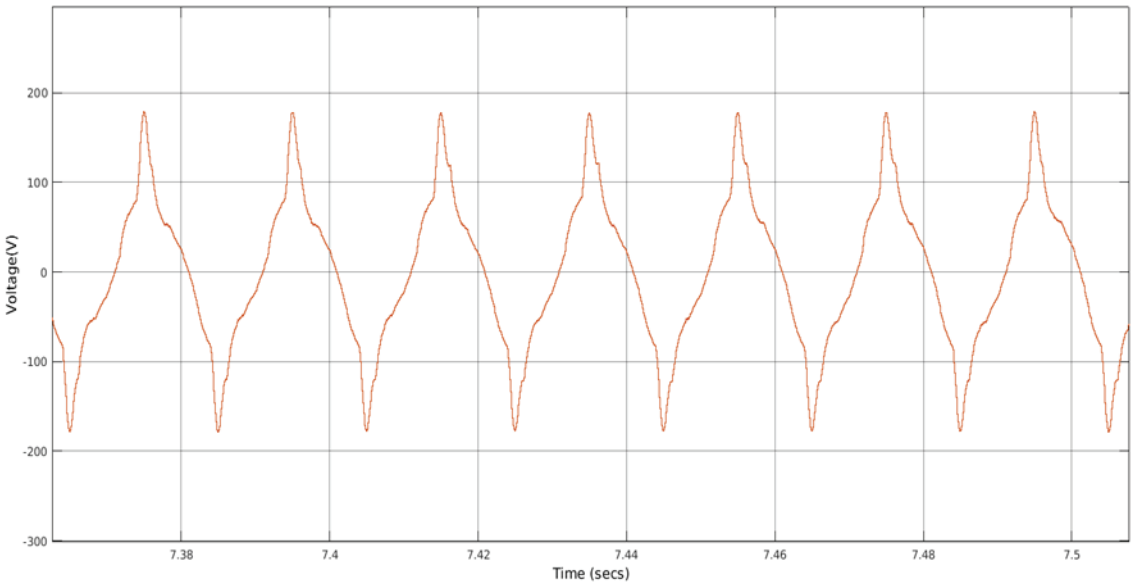

Figure 9. Expanded view of the motor voltage at 1400RPM

As seen from the above figures, motor voltage distortion reduces as the motor RPM reaches to its maximum level as motor gets every input as per its rated values. Same effect is observed in next simulation conditions where motor speed is varied in three steps 800RPM, 1000RPM and 1200RPM.

Two sets of 9 lead acid batteries of 12 V each with fully charged voltage of around 13.8 V, 40 Ah are used to get independent required input voltage Vdc1 and Vdc2. This source is connected to single phase five level cascaded bridge multilevel inverter. Single phase capacitor stat and run induction motor is connected as load. The circuit diagram of five level H bridge inverter is shown in figure 3. It consists of two H Bridge made up of IGBT with antiparallel diode as switch. Two bridges are connected in cascade and output is connected to single phase induction motor. Voltage and current sensors are used for sensing motor voltage and current and optical speed sensor is used for sensing speed as shown in figure 3.

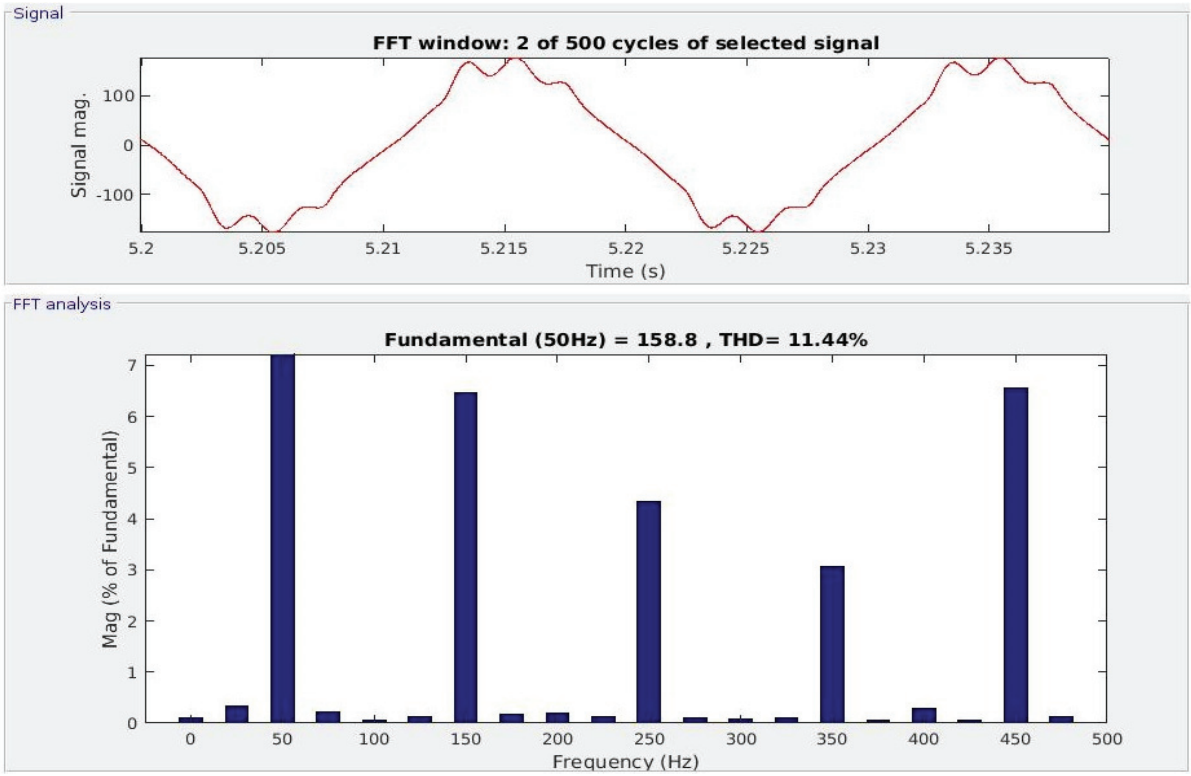

Figure 10. FFT PID Voltage THD Result

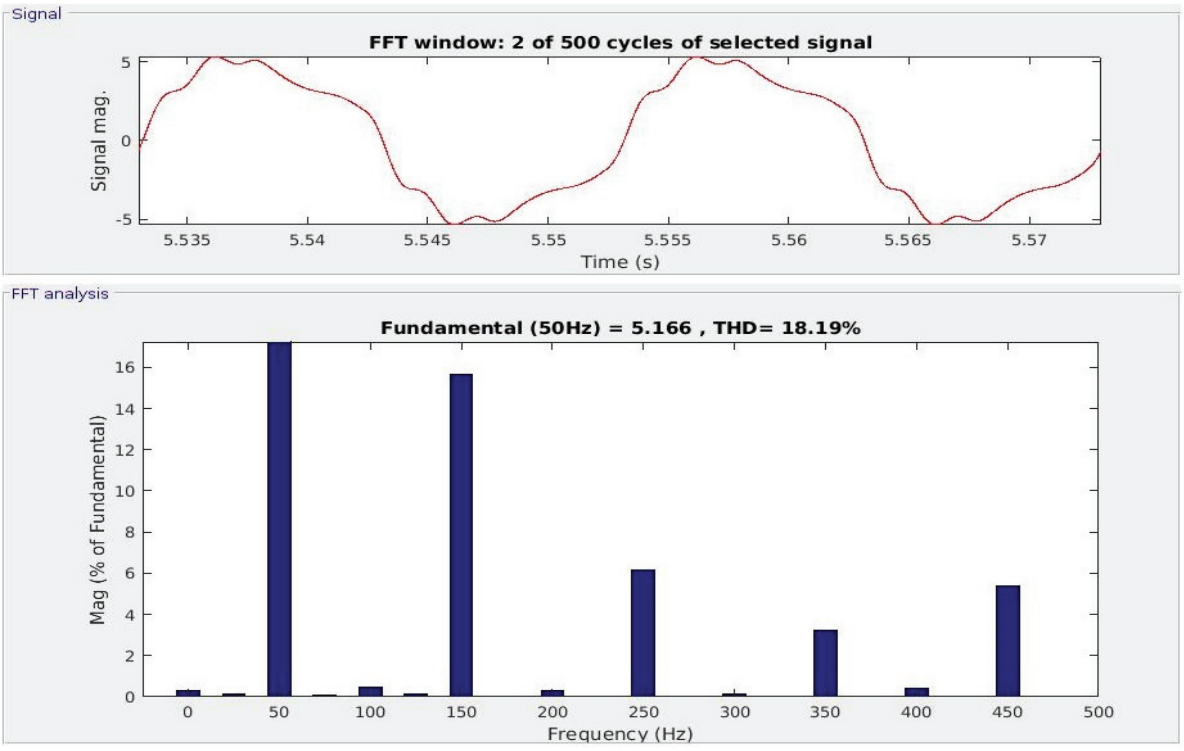

Figure 11. FFT PID Current THD Result

5. Conclusion

The paper demonstrates that the use of a cascaded H-bridge multilevel inverter with Sinusoidal Pulse Width Modulation (SPWM) is an effective approach for mitigating harmonic content in electric power systems. Multilevel inverter topology enables operation at higher output voltage levels while reducing voltage stress across switching devices, making it suitable for high-power applications. The systematic analysis and simulation carried out using Atmel Studio and MATLAB confirm that the proposed configuration significantly reduces harmonic distortion. The results obtained for both heating loads and induction motor applications under different load conditions show improved output waveform quality and reduced harmonic components. Therefore, the cascaded H-bridge multilevel inverter with SPWM provides a reliable and efficient solution for harmonic mitigation in practical power electronic applications.

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