International Journal of Applied Engineering Research
ISSN 0973-4562 Volume 14, Number 24 (2019) pp. 4579-4592

http://www.ripublication.com

ADVANCE CONTROL OF TRANSFORMERLESS CASCADED H BRIDGE MULTI-LEVEL INVERTER FOR HARMONIC MITIGATION: SIMULATION AND EXPERIMENTAL EVALUATION-II

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Abstract

Detailed step by step analysis of transformerless cascaded h bridge multi-level inverter has been carried out for harmonic mitigation [1]. A testing results for heating and induction motor applications were presented. The proposed hardware using MOSFET 541 and ATMEG controller is used in this paper for further evaluation of tranformerless cascaded h bridge multilevel inverter. An experimental evaluation for harmonic mitigation is carried out using Sinusoidal PWM (SPWM) techniques for multilevel inverters that has been properly deduced from two level inverter. A results of PID control technique is presented. Programming is carried out in ATMEG controller. Atmel simulation development board is used for program development. It is observed that harmonics are mitigated for both loads at different load conditions compared to conventional two level inverters. Also matching of hardware results with simulated one confirms effectiveness of strategy implemented.

Keywords: ATMEG, Cascaded H-Bridge, MOSFET, PID Control, Transformerless Multi-level Inverter, SPWM, Total Harmonic Distortion (THD)

1. Introduction

In recent years, the demand for high power electrical systems has increased rapidly. Many industrial applications such as motor drives, heating systems, and renewable energy systems require medium to high voltage levels. In such systems, power quality becomes an important issue. One of the major problems in power quality is the presence of harmonics in the output voltage and current. Harmonics cause additional losses, heating, and reduced efficiency of electrical equipment [1-6].

Therefore, harmonic mitigation is an important requirement in modern power electronic systems.

Conventional two-level inverters are widely used for DC to AC conversion. However, they produce high harmonic distortion in the output waveform. This leads to poor power quality and affects the performance of connected loads such as induction motors. To overcome these limitations, multilevel inverters have been introduced. Multilevel inverters generate output voltage in multiple steps, which makes the waveform closer to a sinusoidal shape. As a result, harmonic distortion is reduced and overall system performance improves [7-11].

Among different multilevel inverter topologies, the cascaded H-bridge (CHB) multilevel inverter is one of the most popular configurations [12, 13]. It uses separate DC sources and H-bridge units connected in series [14-17]. This structure provides high modularity and flexibility. It also reduces voltage stress on switching devices and improves efficiency [18-24]. Due to these advantages, CHB multilevel inverters are widely used in medium and high power applications.

In Part-1 of this work, a detailed analysis of cascaded H-bridge multilevel inverter was carried out for harmonic mitigation. The study included basic operation, switching strategies, and simulation using tools like MATLAB and Atmel Studio. Results were presented for both heating load and induction motor applications. It was observed that multilevel inverter significantly reduces harmonic content compared to conventional inverters. The use of Sinusoidal Pulse Width Modulation (SPWM) technique was also discussed, which helps in generating better output waveform [1].

Although simulation results provide useful insights, practical implementation is necessary to validate the performance of the system. Hardware testing helps to understand real-time behavior, switching losses, and control effectiveness. Therefore, in this work, an experimental evaluation of transformerless cascaded H-bridge multilevel inverter is carried out. The proposed system uses MOSFET switches and ATMEGA-based microcontroller for control implementation. The SPWM technique used in Part-1 is extended for hardware implementation.

In addition to SPWM, a PID control technique is also used in this work to improve system performance. PID controller helps in reducing error and maintaining desired output conditions. The controller is programmed using Atmel development tools. The switching signals are generated and applied to the inverter circuit through suitable driver circuits. The system is tested under different load conditions to evaluate its performance.

The main objective of this paper is to analyze and validate the harmonic mitigation capability of cascaded H-bridge multilevel inverter using hardware setup. The performance is compared with conventional two-level inverter. Both simulation and experimental results are analyzed and compared. This comparison helps to verify the effectiveness of the proposed method.

The results show that harmonic distortion is significantly reduced for different types of loads. The output waveform becomes more sinusoidal. Also, the hardware results closely match with simulation results. This confirms that the proposed control strategy and inverter configuration are effective for practical applications.

2. Methodology

2.1 Proposed Single Phase five level Cascaded Multilevel Inverter Transformerless Cascaded H Bridge Multi-Level Inverter

The circuit diagram of five level H bridge inverter is shown in figure 1. It consists of two H Bridge made up of IGBT- FGA15N120ANTD with antiparallel diode as switch. Two bridges are connected in cascade and output is connected to single phase induction motor. Voltage and current LEM sensors are used for sensing motor voltage and current and optical speed sensor is used for sensing speed as shown in figure 1.

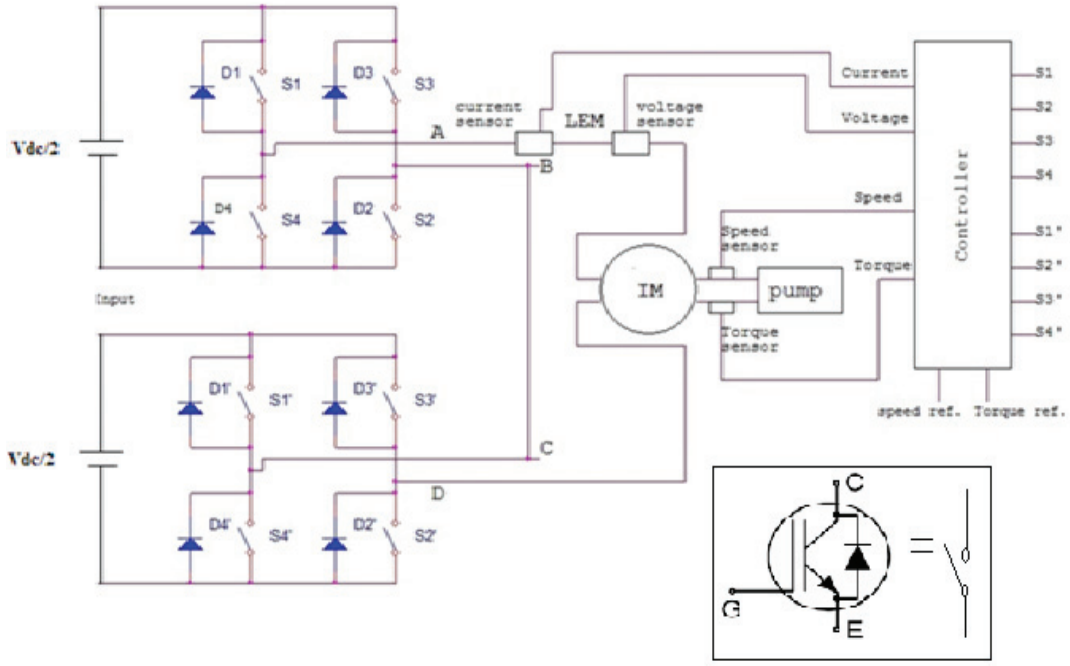

Figure 1. Circuit Diagram of 1-Phase Five Level Cascaded Multilevel Inverter Induction Motor Drives

2.2 Proposed Microcontroller based Controller of Transformerless Cascaded H Bridge Multi-Level Inverter for Harmonic Mitigation

The controller used to provide switching signals to all eight switches (IGBT) so as to control speed and toque is shown in figure 2. Switching signals are generated by microcontroller Arduino Mega -ATMEGA 2560 with ability to program with i/o digital and analog pins with operating at very high speed approaching 1 MIPS per MHz. Inbuild PID controller is used to generate error for speed which will act as modulating signal for generation of pulses by inphase deposition SPWM. Program is written in ATMEL Studio and loaded in microcontroller Arduino Mega. Then using MCT6 optocoupler isolation of signals ae carried out and given to driver circuit of IR2110 single phase driver of International rectifier to drive IGBT used. IR2110 is capable of driving one leg (upper and lower) of H-bridge as seen in figure 2. However separate optocouplers are required for each switching signals. Separate 5 V power supply is required for optocoupler and 12 V supply is required for driver which can be taken from any of the single battery.

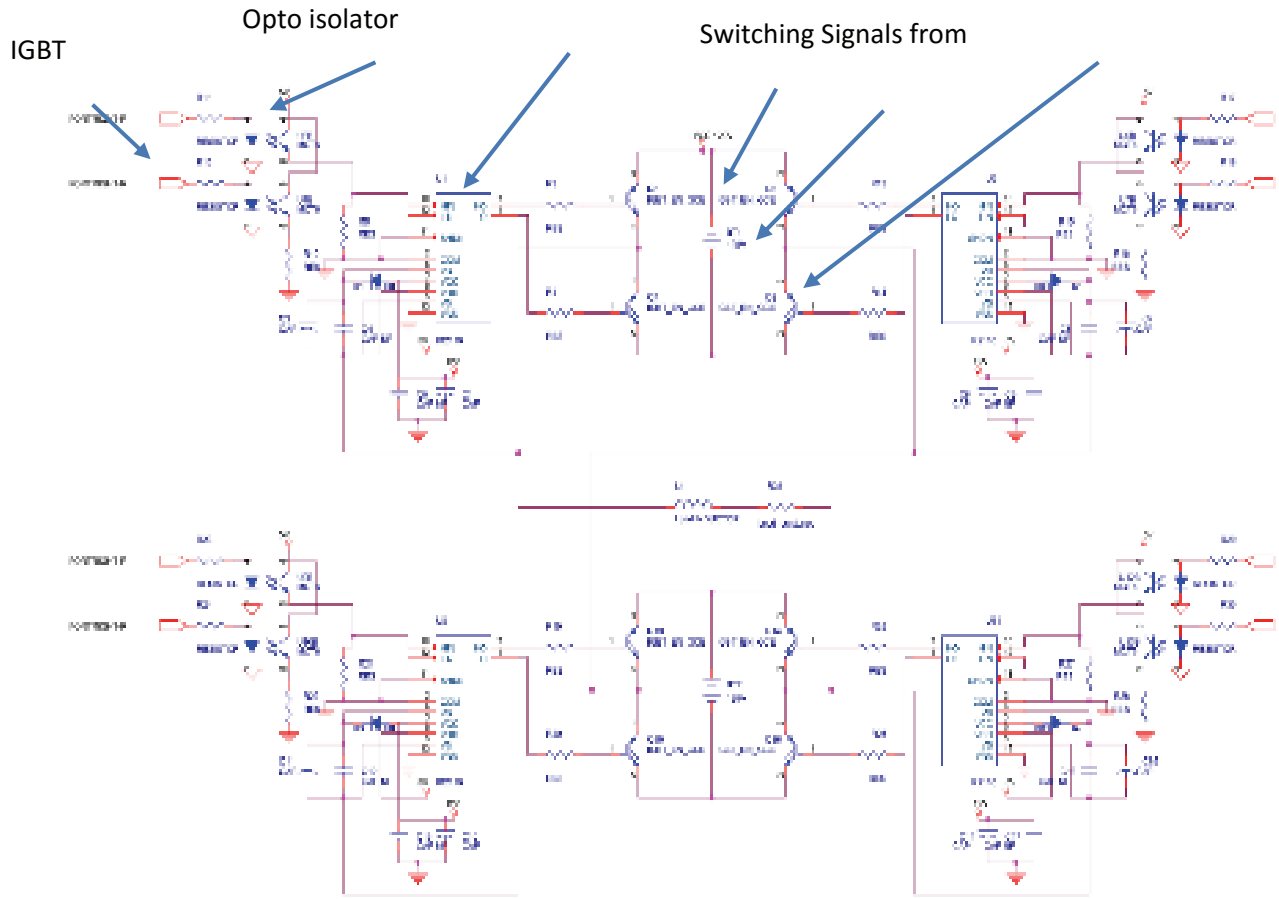

Figure 2. Control Diagram

2.3 Experimental Implementation of Single Phase five level Cascaded Multilevel Inverter.

Two sets of 9 lead acid batteries of 12 V each with fully charged voltage of around 13.8 V, 40 Ah are used to get independent required input voltage Vdc1 and Vdc2. This source is connected to single phase five level cascaded bridge multilevel inverter. Single phase capacitor stat and run induction motor is connected as load which is shown in experimental test bench (figurer 1). The circuit diagram of five level H bridge inverter is shown in figure 2. It consists of two H Bridge made up of IGBT- FGA15N120ANTD with antiparallel diode as switch. Two bridges are connected in cascade and output is connected to single phase induction motor. Voltage and current LEM sensors are used for sensing motor voltage and current and optical speed sensor is used for sensing speed as shown in figure 2.

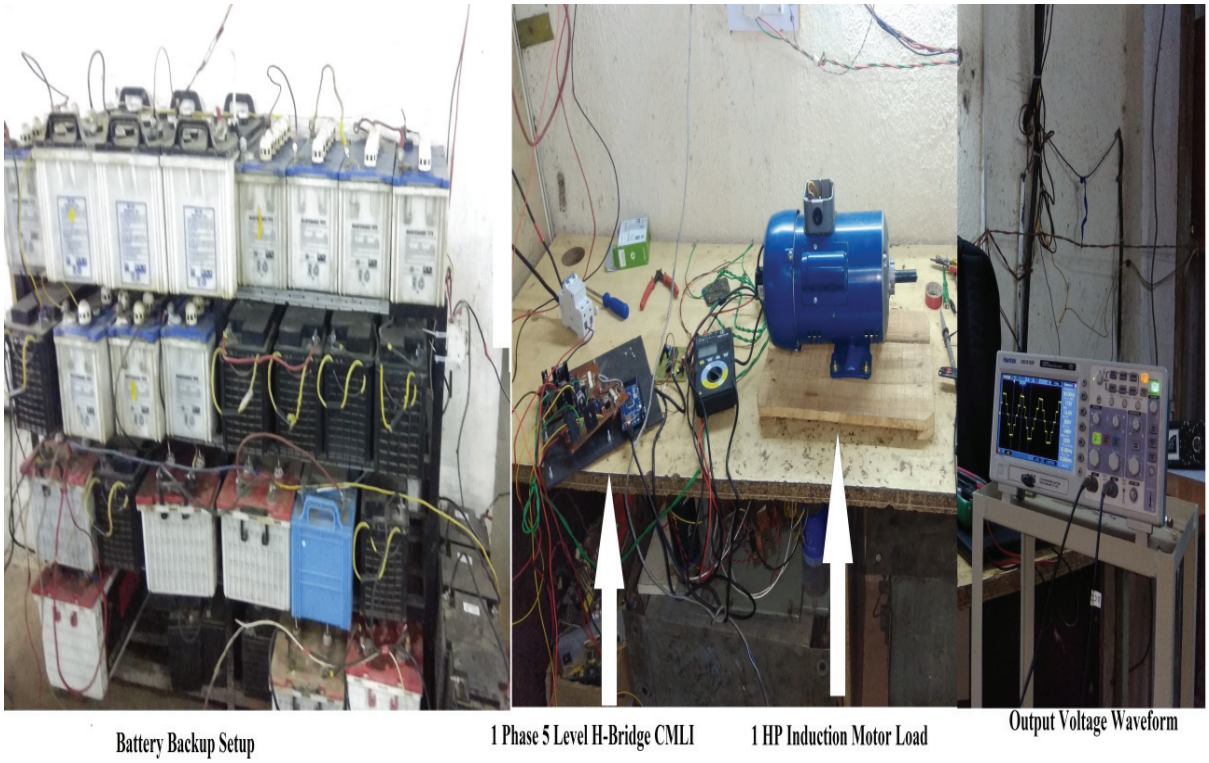

Figure 3. Experimental Setup of Single Phase five level Cascaded Multiphase Inverter

3. Five Level Cascaded H-bridge test results

A. High Voltage Test Results

Test conditions:
Vdc1 = 120V;
Vdc2 = 120V; (12V lead acid battery banks)
Load – Resistive (Filament Bulbs);
Measurement Equipment: Hantek DSO5102P
Power Switches: IGBT FGA15N120ANTD
Controller: ATMEGA 2560 (Arduino Mega Board)
Programming Environment: ATMEL Studio
IGBT Driver: IR2110
Opto-isolator: MCT6

The experimental results of the transformerless cascaded H-bridge multilevel inverter are presented in this section. The system is tested under different load conditions using resistive and R-L loads. The input DC voltages are maintained at Vdc1 = 120 V and Vdc2 = 120 V. Initially, the output voltage waveform without SPWM technique is observed, as shown in Fig. 4. The waveform shows stepped output with noticeable distortion. The waveform is not smooth and contains high harmonic components. This confirms the limitation of basic switching operation. When SPWM technique is applied, the output waveform improves significantly. The voltage waveform with SPWM for 100 W load is shown in Fig. 5. The waveform becomes smoother and closer to sinusoidal shape. The five-level structure is clearly visible. This indicates effective switching control. The current waveform corresponding to SPWM operation

for 100 W load is shown in Fig. 6. The current waveform is more sinusoidal compared to without SPWM. The distortion is reduced, which shows better power quality. Further, the system is tested at higher load conditions. The voltage waveform for 200 W load is shown in Fig. 7. It shows improved smoothness and stability. Similar improvement is observed for 300 W load, as shown in Fig. 8, and for 500 W load, as shown in Fig. 9. The waveform quality improves as load increases. The current waveform for 500 W load is shown in Fig. 10. It is observed that the current waveform is nearly sinusoidal and stable. This confirms proper operation of inverter under higher load. FFT analysis is carried out to evaluate Total Harmonic Distortion (THD). The voltage THD result is shown in Fig. 11, and current THD result is shown in Fig. 12. The THD values are significantly reduced with SPWM and PID control. The PID controller helps in maintaining stable output and reducing error. It improves dynamic response of the system under varying load conditions. The experimental results are also compared with simulation results. It is observed that both results are closely matching. This confirms correctness of the design and implementation.

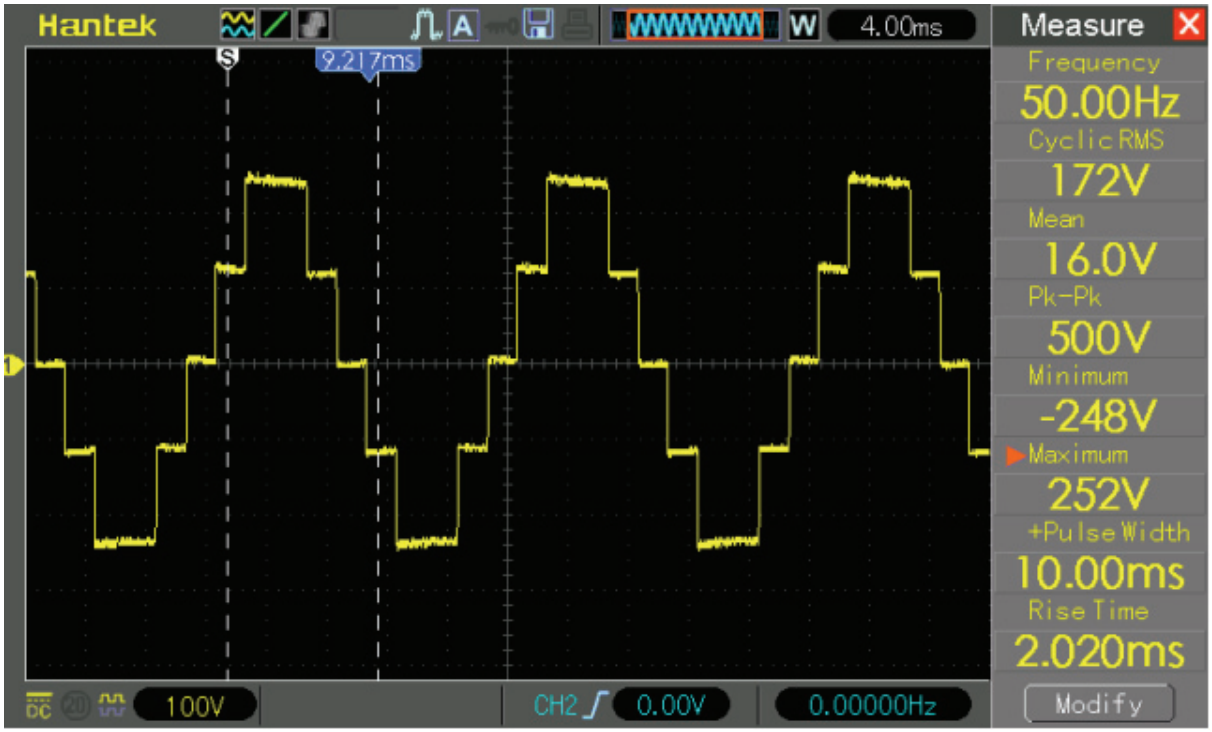

Figure 4. Voltage wave form of Five level generation without SPWM. Load 100W .

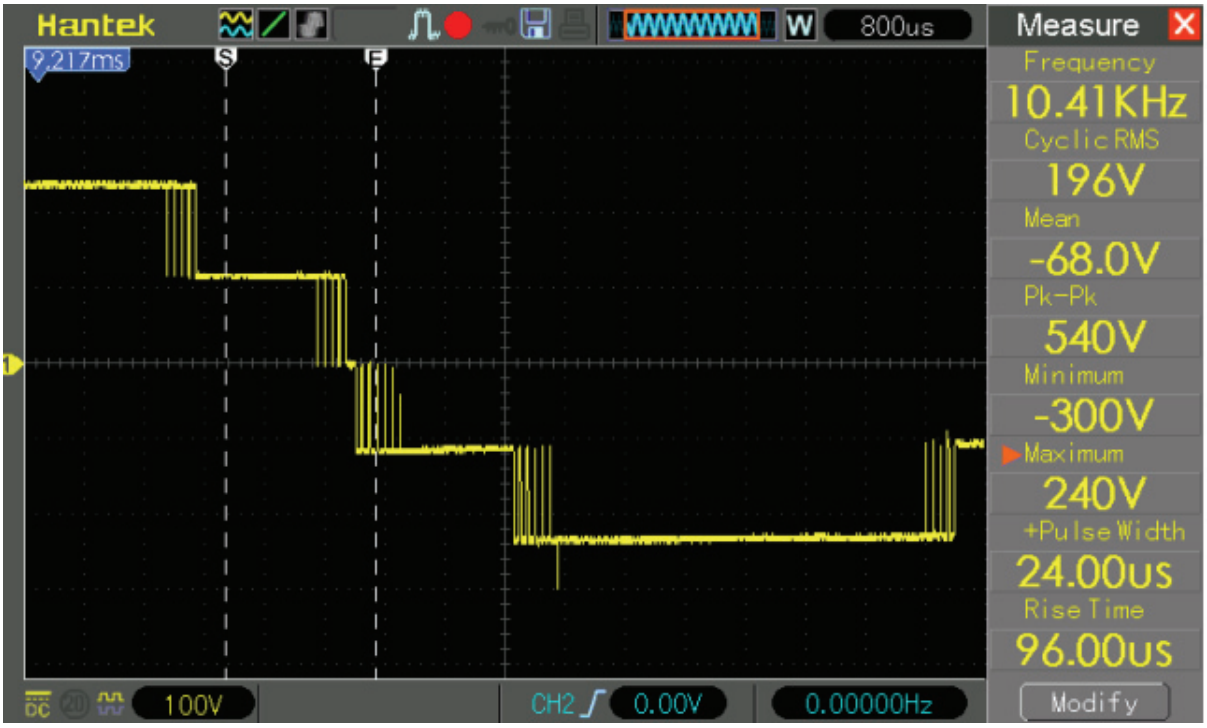

Figure 5. Fig.5. Voltage waveform of Five level generation with SPWM (Load 100W).

Figure 6. Current waveform of five level generation with SPWM (Load 100W).

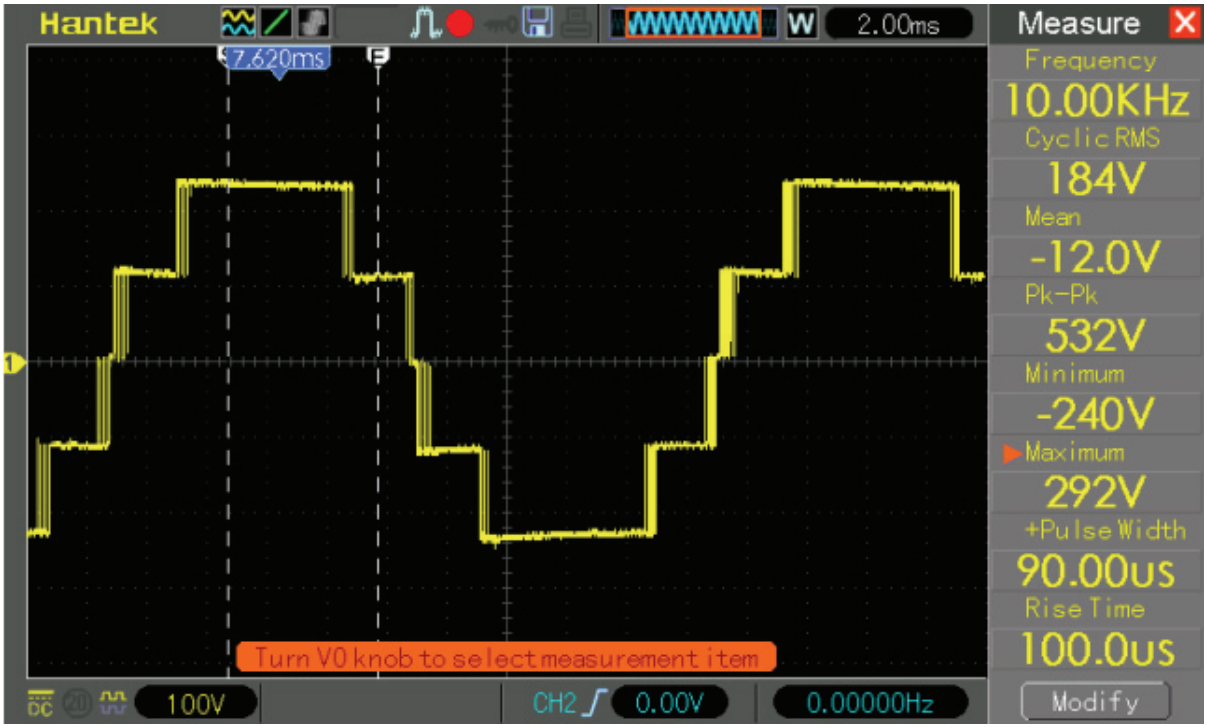

Figure 7. Voltage waveform of Five level generation with SPWM (Load 200W).

Figure 8. Voltage waveform of Five level generation with SPWM (Load 200W).

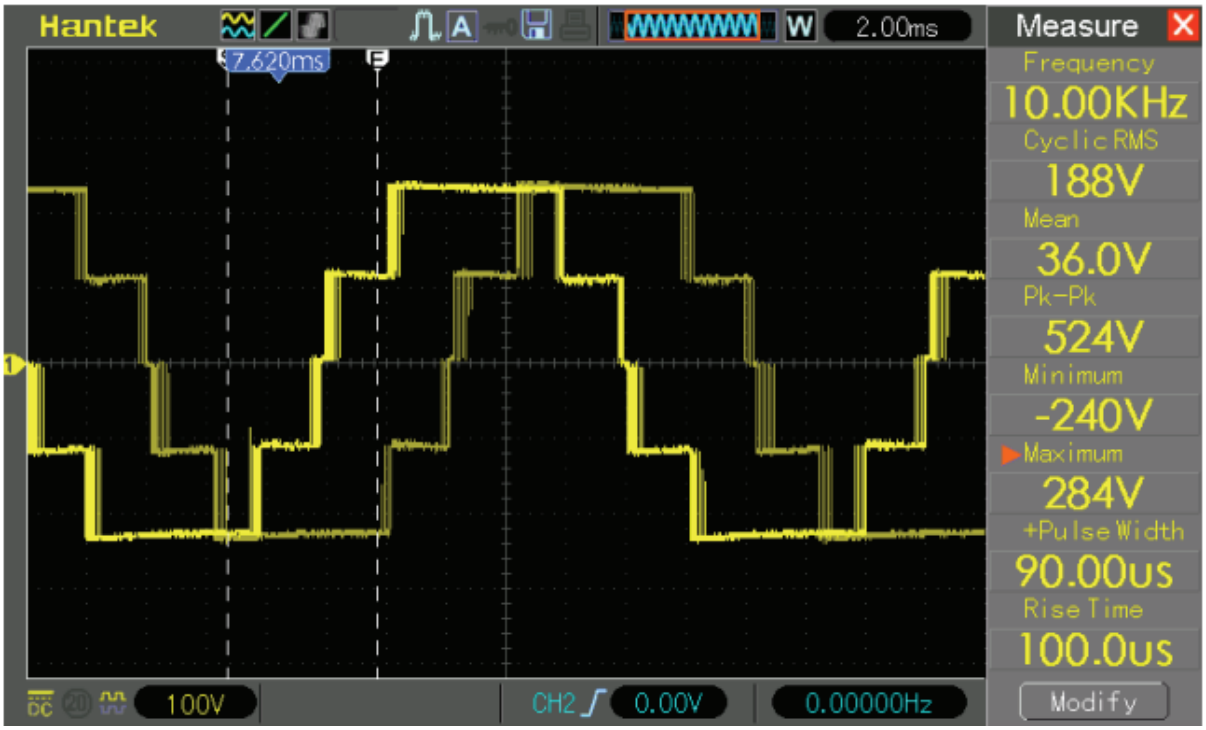

Figure 9. Voltage waveform of Five level generation with SPWM (Load 300W)

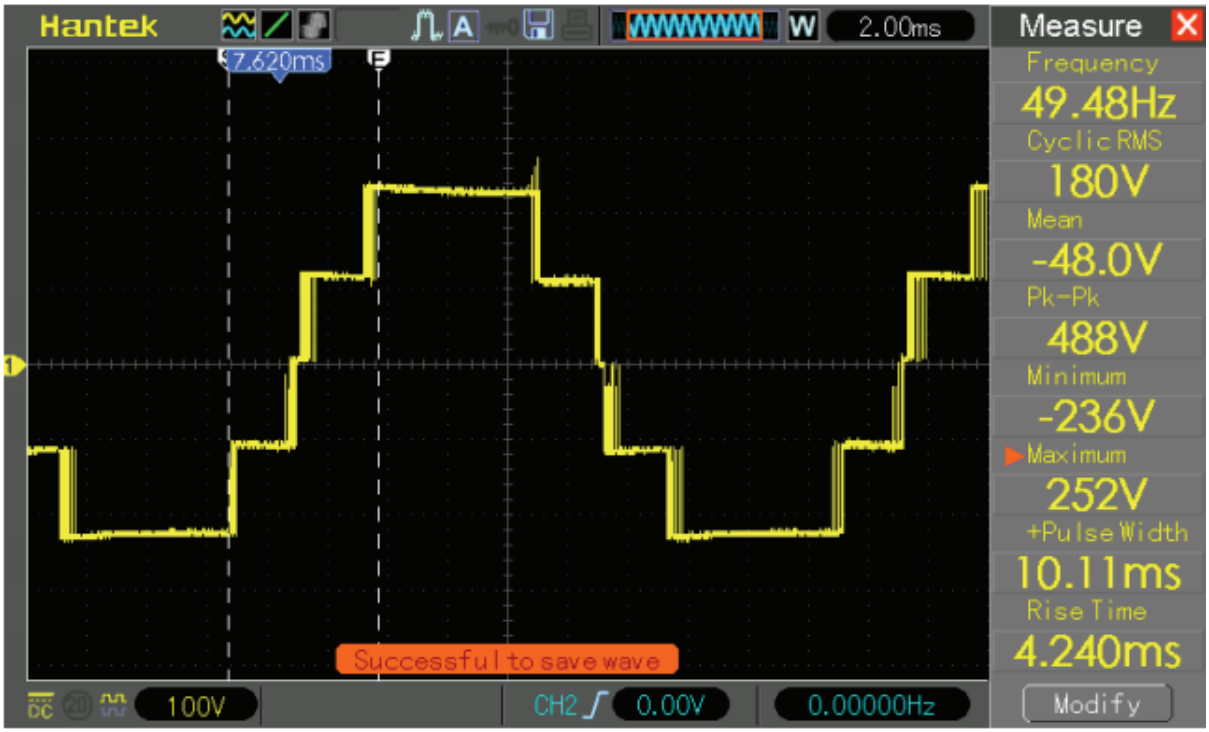

Figure 10. Voltage waveform. Five level generation with SPWM (Load 500W).

Figure 11. Current waveform. Five level generation with SPWM (Load 500W).

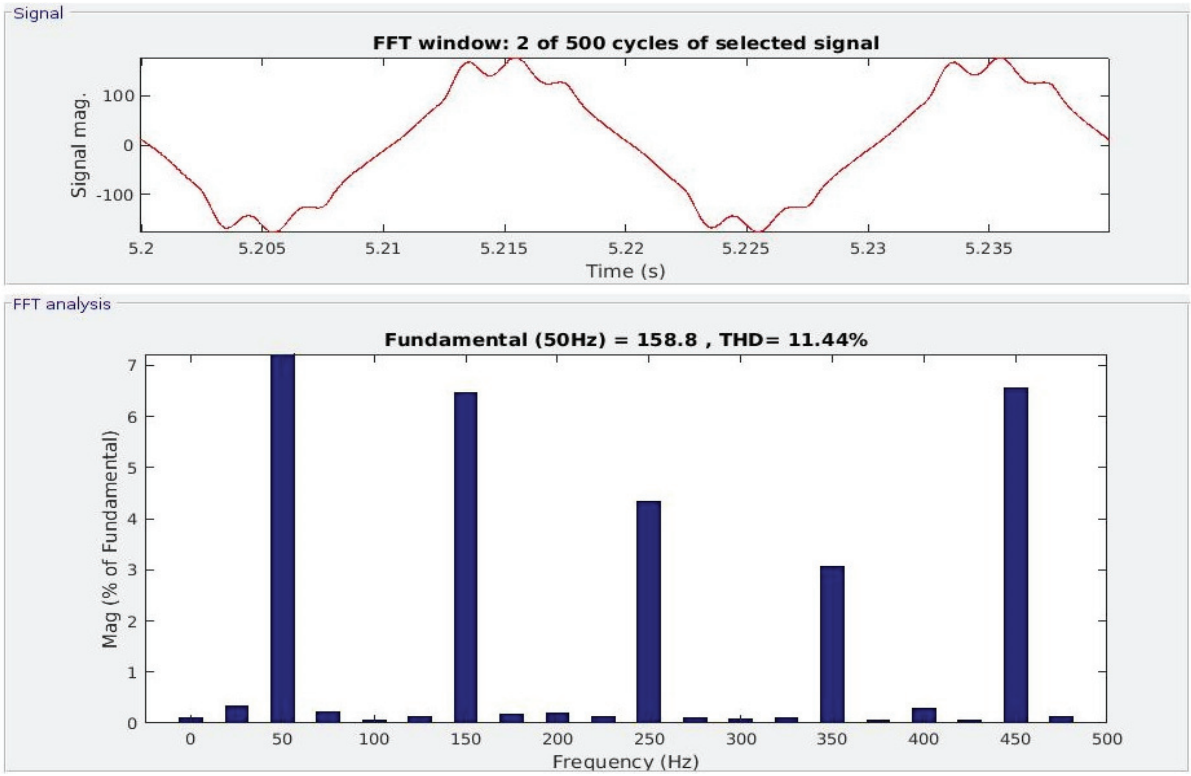

Figure 12. FFT PID Voltage THD Result

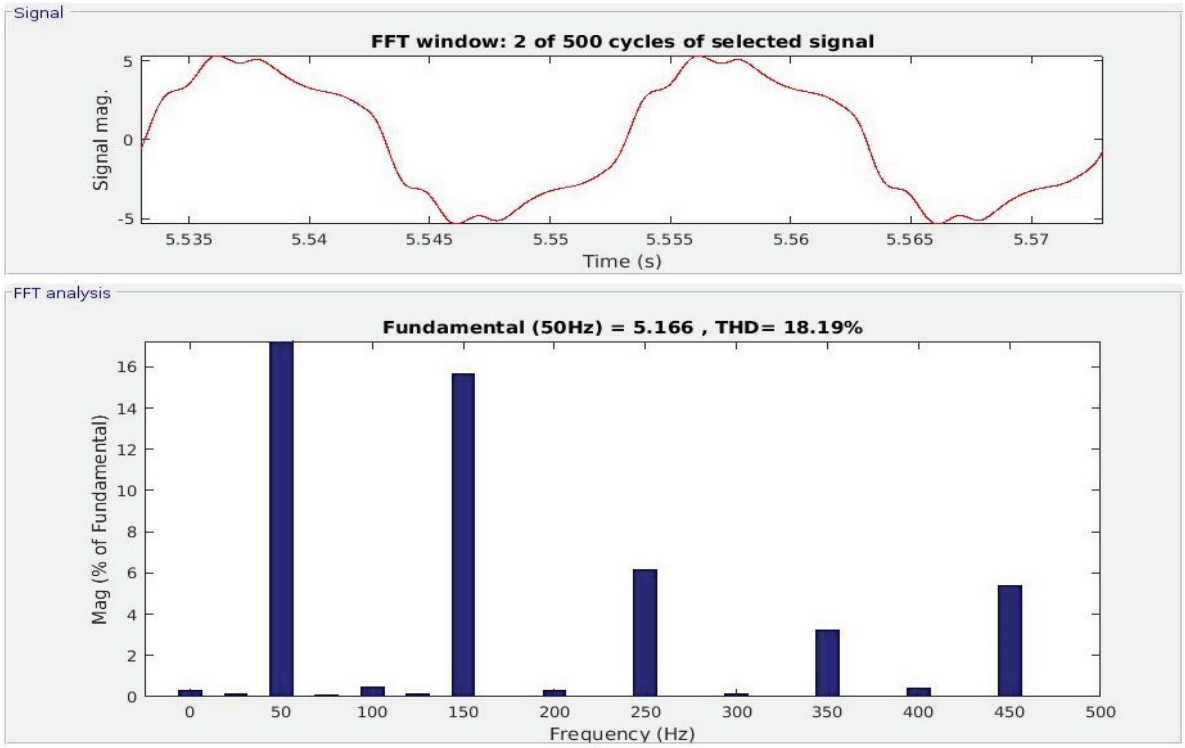

Figure 13. FFT PID Current THD Result

The experimental results clearly show that the proposed transformerless cascaded H-bridge multilevel inverter performs effectively for harmonic mitigation. The improvement in performance is mainly due to multilevel topology, SPWM technique, and PID control. The output waveform without SPWM, as shown in Fig. 4, has high distortion. The waveform contains sharp transitions and harmonic components. This is due to simple switching operation. Such waveform is not suitable for sensitive loads. With SPWM technique, as shown in Fig. 5, the waveform becomes smoother. The use of sinusoidal reference and carrier signals helps in proper switching. This reduces harmonic components. The five-level stepped waveform approaches sinusoidal shape. This improves power quality. The current waveform in Fig. 6 also shows improvement. The reduction in current distortion indicates better energy transfer. This reduces heating and losses in the system. It is important for efficient operation of loads such as induction motors. The effect of load variation is clearly observed from Fig. 7 to Fig. 9. At 200 W load (Fig. 7), waveform is more stable compared to lower load. At 300 W (Fig. 8) and 500 W (Fig. 9), the waveform becomes more balanced and smooth. This shows that inverter performs better at higher load conditions. The system reaches near rated operation, which improves output quality.

The current waveform at higher load, as shown in Fig. 10, is nearly sinusoidal. This confirms that inverter is capable of supplying stable current under heavy load. This is important for practical applications. The FFT analysis results shown in Fig. 11 and Fig. 12 provide quantitative validation. The reduction in THD values confirms effectiveness of SPWM and PID control. Lower THD indicates better power quality

and reduced harmonic losses. The PID controller plays an important role in improving system response. It continuously adjusts control signal based on error. This helps in maintaining desired output voltage and speed. The system becomes stable under changing load conditions. The use of ATMEGA 2560 controller provides a simple and cost-effective solution. It allows flexible programming and control. The switching signals are generated accurately. The use of opto-isolator and IR2110 driver ensures safe and efficient operation of switching devices. The transformerless configuration reduces size and cost of the system. It eliminates bulky transformers. This improves efficiency and makes the system suitable for compact applications.

The close matching between simulation and experimental results confirms validity of the design. It shows that theoretical analysis is correctly implemented in hardware. The system performs well for both resistive and R-L loads. This shows its versatility. It can be used in heating applications as well as motor drives. However, some practical issues must be considered. Switching losses in IGBT devices can increase at higher switching frequency. Proper cooling is required. Also, balancing of DC sources is important for stable operation.

4. Conclusion

The study presents a detailed investigation of a transformerless cascaded H-bridge multilevel inverter for harmonic mitigation. The proposed hardware implementation using MOSFET 541 and an ATMEG controller was successfully developed and tested for both heating and induction motor applications. Sinusoidal Pulse Width Modulation (SPWM) techniques derived from the conventional two-level inverter were applied to the multilevel inverter, and a PID control strategy was implemented through programming on the ATMEG controller using the Atmel simulation development board. Experimental results demonstrate that the proposed inverter significantly reduces harmonic distortion under different load conditions compared to conventional two-level inverters. Furthermore, the close agreement between hardware and simulation results validates the effectiveness and reliability of the implemented control strategy for harmonic mitigation in practical applications.

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