A Novel Modified P-Q Theory to Control UPQC under Power Quality Issues in Distribution System

J. Sandhya Rani,
PG Scholar, M. Tech (EPS), VNR Vignana Jyothi Institute of Engineering and Technology (Autonomous), Hyderabad,

Dr. Rashmi Kapoor
Asst. Professor, Department of Electrical and Electronics Engineering, VNR Vignana Jyothi Institute of Engineering and Technology (Autonomous), Hyderabad.

Abstract- **Power quality in the distribution system in recent times has become a noticeable issue due to the changing trends in electrical distribution system. The increasing usage of power electronic interfaces to convert power from one form to another and to control the speed of electrical motors and some of the non-linear loads are causing the attenuation in the current profile and there by injecting the harmonics in to the system. The other various power quality issues are also mentioned in this paper, like voltage Sags/Swells and unbalanced voltages. To address all the mentioned issues, in this paper a modified instantaneous p-q theory is proposed for controlling the series and shunt converters of Unified Power Quality Conditioner (UPQC). The UPQC is joined to the distribution system at Point of Common Coupling (PCC) and the mitigation of various power quality issues in the distribution system is done by the UPQC. The shunt converter not only compensates the harmonics in the current component but also does the some part of reactive power compensation. The series converter, by injecting voltages at PCC, performs the compensation during voltage Sags/Swells. The UPQC capability in solving the mentioned issues is analyzed by conducting the simulation tests in MATLAB/Simulink platform.**

Index Terms- **Distribution system, Power Quality, Sag/Swell, Non-Linear load, UPQC, PCC**

I. INTRODUCTION

At the end of the distribution systems i.e, on the utility side, due to the limited power and other loads influences, distortions of the voltage can occur which negatively influence the supplied load. There could be not only alterations of the rated value, but alterations of the sinusoidal waveform. On the other side, the loads themselves can be sources of distortions, especially when we consider the currents drawn from the source. The development of the power electronics increases the nonlinear loads. Unified Power-Quality Conditioner (UPQC) systems could be a solution in order to enhance the power quality [1, 3]. These types of systems are capable not only to enhance the power quality on the load side, but also on the source side, simultaneously with the reactive power compensation. Mainly, this type of systems consists of two active filters for which a common DC circuit is there. The series active filter is responsible for correction of the source voltage while the parallel (shunt) active filter locally supplies the harmonics of load current specific to the load, compensates the source side reactive power and controls the common DC voltage. Simultaneous filtering of grid voltage and load current has become a difficult task due to the actual tendency of standards imposed by the grid to maintain power quality. The enhanced quality of power supply on

the grid side has become a mandatory thing. This puts an immense pressure on grid to satisfy its industrial load. Appearance of frequent sags / swells over power system will result in malfunction of industrial processes. This makes the grid to stick to the objective of supplying reliable quality power to industrial customers [2]. Major portion of power quality issues that results from power system are voltage sags/ swell and current harmonics.

Use of Unified Power Quality Conditioner (UPQC) is one of the best options for compensation of voltage sag / swells and current harmonic filtering at the same time. Also UPQC can mitigate the unbalance that occurs because of different types of faults. In simple words the UPQC provides protection for critical or sensitive loads against voltage disturbances that arise in power system and compensates the critical load currents by providing a sinusoidal current to be drained into the power system.

The UPQC comprises of back to back connected two voltage source converters, one converter is joined in series with the line popularly known as Series Active Filter (SAPF) and the other is connected across the line commonly known as Shunt Active Filter (ShAPF). The SAPF performs the job of voltage restoration, flicker and voltage imbalance compensation whereas ShAPF compensates current harmonics. SAPF behaves like a controlled voltage source and ShAPF operates as controlled current source. The circuit configuration of distribution system with UPQC connected at PCC is shown in Fig.1.
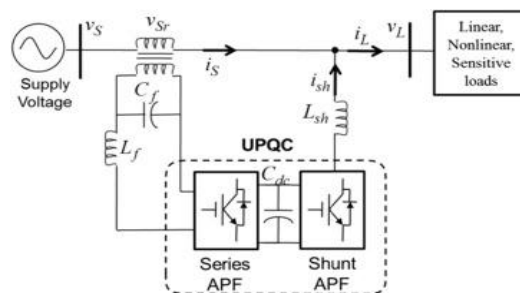

Fig.1 Configuration of distribution system and UPQC

The methods based on p-q and d-q theories that are used for calculating the reference signal in the earlier times were largely time domain based techniques. Apart from traditional d-q and p-q theories[5]-[7] there are other advanced control methods for generating the reference signal which use the adaptive filters such as adaptive notch filter(ANF), Adaptive Linear Element(ADALINE) etc[10]-[12]. But these methods need calculation for each phase currents and voltages which makes more complex when compared to p-q and d-q theories. However the conventional p-q theory is not able to generate accurate results in the case of voltage distortions or unbalanced conditions. This disadvantage can be overcome by using fundamental frequency positive sequence (FFPS) voltages for the calculation of reference current signal. For this purpose the modified p-q theory use the Generalized Cascaded Delay Signal Cancellation (GCDSC) technique.

II. SYSTEM DESCRIPTION

The distribution system shown in figure1 is connected to various types of loads through the line impedance. The loads are linear load, non-linear load and sensitive loads. The sensitive load in this case refers to RL load. A Single line to Ground fault is also placed in the system at a particular point of time to study the case of unbalance. The issues like harmonics, Sag/Swell conditions and unbalanced cases are as described below.

The increasing usage of power electronic converters and semiconductor devices, causes the power system to be subjected to harmonics especially the deterioration of current profile is insisting the concern towards power quality problem. A three phase diode bridge rectifier with R-L load across its output terminals is used as non-linear load in the system.

A three phase asynchronous machine i.e, induction motor is connected to the system. As we know Induction motor needs high starting torque so initially it draws the huge current from the source there by causing a dip in the voltage which is called as sag. The voltage comes to the normal state automatically once the motor achieves the rated speed but the sag in the source voltage is not the desired one so it must be either eliminated or reduced.

The power system is subjected to load changes often. The sudden trip or outage of the load may cause rise in the voltage which is called as swell.

A single Line to Ground fault is placed in the system to create unbalance in the source voltages and load voltages as well.

A. Unified Power Quality Conditioner

UPQC-Unified Power Quality Conditioner, a FACTS family device of series-shunt type. The circuitry of UPQC is also shown in the figure1. It is constructed as a combination of two voltage source converters i.e, series converter and shunt converter which share the common DC link(A capacitor connected in between the series and shunt converters)[3].

The series converter is used mainly for voltage compensation as it either injects the voltage in to the system or draws the voltage from the main system and shunt converter is used for load side compensation which either injects the current into or takes the current from, the main distribution system. The shunt converter also regulates the common DC-link voltage and also it acts as Active Power Filter which compensates the current harmonics. It balances the reactive power and improves the power quality of the distribution system. The detailed description of control strategies is presented in section III.

III. CONTROL OF UPQC

The controlling of UPQC is implemented based on modified instantaneous p-q theory and it is designed with four different blocks and they are the Generalized Cascaded Delay Signal Cancellation (GCDSC) block which is used to extract fundamental-frequency positive-sequence(FFPS) component, the load power calculation block, series VSC and shunt VSC control blocks. The detailed description of the above mentioned blocks is given as follows.

A. Generalized Cascaded Delay Signal Cancellation Block

Sampling and storing of αβ instantaneous voltage vector is used to construct the GCDSC technique. The current and delayed voltage vectors are joined together through a mathematical transformation. The proposed transformation will give a unity gain for the fundamental-frequency positive-sequence (FFPS) voltage vector component and for some selected components it is zero. The fundamental-frequency negative-sequence vector can be eliminated by cascaded transformation and also some selected positive-

sequence and negative-sequence harmonic vector components so that accurate FFPS voltage vector can be obtained.

As we mentioned above, for the extraction of FFPS signal component of voltage a delay signal cancellation (DSC) operator [10] is used and the equation for the same is given as below,

$$V_{h\alpha\text{-}\beta}(t) = \frac{1}{2}[V_{\alpha\text{-}\beta}(t) + e^{\frac{j2pi}{N}}V_{\alpha\text{-}\beta}\left(t - \frac{T}{N}\right)] \qquad (1)$$

In the above equation the voltage component vector values are presented in α-β frame, where vα−β(t) = vα + jvβ(t) is the voltage vector, vhα−β(t) = vhα(t) + jvhβ(t) is the FFPS component of voltage which is given in sequentially with different harmonics orders as in the equation h represents harmonic order and the value of h is, h = N ×k+1 (k = ±1,±2,±3...) in α−β domain, T is the fundamental period of voltage, delay factor is N. The DSC operator has a transfer function and its value is given in equation 2 as below,

$$G_N(j\omega) = \left| \cos(\frac{\omega T}{2N}\text{-}\frac{\pi}{N}) \right| \angle(\frac{\omega T}{2N}\text{-}\frac{\pi}{N}) \qquad (2)$$

In equation 2, 'N' is known as delay factor and it is used to block the harmonics of the particular order which is given as, h_b = N ×k − 1 (k = ±1,±2,±3...). Using equations 1 and 2, the DSC operator is mathematically modeled and that is depicted in Fig. 2(a). In the figure the delay is shown with the block z−M which is in discrete form where M represents the value of delay sample corresponding to a delay factor of N. As it is difficult to find specifically, the PCC voltage harmonic quantity, the possible solution is to connect five delay signal operator blocks in series with delay factors N = 2, 4, 8, 16, 32 [4]. This system of series connected blocks is known as GCDSC block which is shown in Fig. 2(b).

(a) Delay Signal Cancellation Block-N

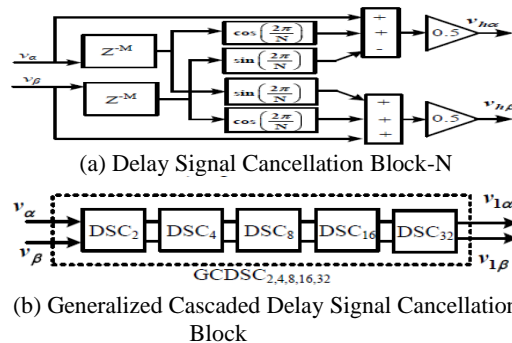(b) Generalized Cascaded Delay Signal Cancellation Block

Fig.2 Fundamental Frequency Positive Sequence Extraction using Generalized Cascaded Delay Signal operation

As we know, frequency adaptive system is quite effective, this can be done by using the GCDSC block as a pre-filtering mechanism, but it is more complex. The GDSC causes an attenuation in a signal of 0.065% and phase error is observed at a value of 3.43◦(2), where the given signal frequency is 59Hz, if the GDSC is designed for frequency of 60Hz. The grid fundamental frequency varies in a low range where the variation is in between 59.3 and 60.2 Hz in normal conditions, which causes insignificant change in the values of magnitude and phase error. As the changes are insignificant, there is not much necessity of making the system, frequency adaptive so that unnecessary complexity can be avoided.

The function of GCDSC is mainly to extract the FFPS component so it a only allows the same through it but still it is also able perform the operation of attenuating the lower order harmonic values. However, while these lower order harmonics are passing through GCDSC few of them comes out from it without alteration. Such harmonics are measured as h = 32 × k + 1, (k = ±1,±2..), (i.e 33rd positive sequence harmonic, 31st negative sequence harmonic etc.). Usually, the magnitude of such components is not considered. Though these lower order components are insignificant, they are sufficiently able to cause the error in the calculation of magnitude

and phase values. Because of this reason a band-pass filter (BPF) is also used to remove these high frequency signals from FFPS signal that is obtained from GCDSC.

B. Load Power Calculation Block

The load power calculation block is shown fig. 3 is used to calculate the fundamental active and reactive power values *PL* and *QL* respectively. The process is done using a power invariant Clarke transformation theory in which abc quantities are converted into α-β frame i.e, the load voltages (*vLa, vLb, vLc*) and load currents (*iLa, iLb, iLc*) are transformed into $\alpha - \beta$ domain load voltages (*vLα, vLβ*) and load currents (*iLα, iLβ*), and it also uses the required equations that are developed using p-q theory[5]-[9]. To get the values of fundamental active power *PL* and reactive power *QL,* the instantaneous active power *pL* and reactive power *qL* are given to a low-pass filter (LPF).

Fig.3 Block diagram of Power Block

C. Shunt VSC Control Structure

As it is shown in fig. 4, the shunt converter control strategy starts with transformation of abc voltage quantities into α-β domain quantities. The shunt converter is capable of solving current power quality issues on load side such as unbalanced loading, disturbed current and poor power factor can be mitigated by the shunt VSC. Apart from this, to maintain the DC-bus voltage at required reference value, it injects real power obtained from DC link into the grid. The reference value for the DC-bus voltage is obtained from general relation between RMS and DC offset value of the AC system. The sensed DC-bus voltage (*Vdc*) is passed through LPF and is compared with reference DC-bus voltage (*V*dc*). The error between *Vdc* and *V*dc* is given to proportional integral (PI)-controller to calculate the loss component (*Ploss*).

Fig.4 Shunt VSC Control Structure

Equation 3 gives the power (*Pref*) to be drawn from the grid which is mentioned below,

$$P_{ref} = P_L + P_{loss} \qquad (3)$$

The FFPS components of PCC voltages *vs1α, vs1β* obtained using GCDSC block are filtered using band pass filters to give *vsf1α, vsf1β*. The reference grid currents in $\alpha - \beta$ frame are calculated using *Pref* and *vsf1α, vsf1β* as,

$$i_\alpha^* = \frac{V_{sf1\alpha} * P_{ref}}{V_{sf1\alpha}^2 + V_{sf1\beta}^2} \qquad (4)$$

$$i_\beta^* = \frac{V_{sf1\beta} * P_{ref}}{V_{sf1\alpha}^2 + V_{sf1\beta}^2} \qquad (5)$$

The above reference current signals are then again converted back to abc domain and compared with measured grid currents (*isa, isb, isc*) in a hysteresis current controller to produce gating signals for the shunt VSC.

D. Control of Series VSC

The control block diagram of series VSC is shown in Fig5. The series VSC, not only protects the sensitive loads from PCC voltage sags/swells, but also compensates for a part of the load reactive power even under normal PCC voltage conditions. The relationship between power angle δ and reactive power shared by series VSC (*QSE*) under normal condition [10] is given in equation 6,

$$\delta = arcsin[\frac{Q_L - Q_{SH}}{P_L - P_{dc}}] \qquad (6)$$

where *QSH* is a standard preset parameter which is the amount of reactive power to be shared by the shunt VSC, *QL* is average load reactive power, *PL* is average load active power and *Pdc* is power of the DC bus. Under conditions of PCC voltage sag and swell, the expression is modified as below which is shown in equation 7,

$$\delta = arcsin[\frac{Q_L - Q_{SH}}{K(P_L - P_{dc})}] \qquad (7)$$

Fig.5 Series VSC Control Structure

where *K* is ratio between load reference voltage peak *VL* and PCC voltage peak *VS*. For the justification of (7). the magnitude of (*QL − QSH*) should be always lesser than (*PL −Pdc*). The power angle δ is less when *Pdc* is lesser and vice-versa, for same reactive power sharing by series VSC. The peak of PCC fundamental voltage (*VS*) and its phase(θ) are obtained by using *vsf1α, vsf1β* components .

The ratio between *VS* and *VL* gives factor *K*. By doing the mathematical operation of 'floor' on *K,* factor *Kd* is calculated. The value of *Kd* is 1 under sag condition and 0 under swell condition. The value of *Kd* is kept 0 under swell condition so that reactive power sharing is done only in sag and nominal conditions because the PCC current decreases under swell condition so a higher amount of voltage needs to be injected for same amount of reactive power compensation, though the series VSC can compensate load reactive power during voltage swell conditions. This requires higher voltage rating of series compensators. As the probability of occurrence of voltage swell is very much lesser as compared to that of voltage sags, it is finalized in the control algorithm to not to give importance to reactive power compensation during swell conditions and it only performs voltage swell compensation. There is a saturation block to keep lower limit of *QSE* to zero. Thus if the load reactive power is less than that of *QSH*, then the entire reactive power is shared by shunt VSC.

The power angle δ is calculated based on (7). Using power angle δ, phase information θ and load voltage reference peak *VL* , the three phase reference load voltages (*vLa, vLb, vLc*) are generated as follows,

$$v_{La}^* = V_L^* \cos(\theta + \delta) \qquad (8)$$

$$v_{Lb}^* = V_L^* \cos(\theta + \delta - \frac{2pi}{3}) \qquad (9)$$

$$v_{Lc}^* = V_L^* \cos(\theta + \delta + \frac{2pi}{3}) \qquad (10)$$

The switching pulses for series VSC are finally produced using a pulse width modulated (PWM) voltage controller which uses the reference load voltages.

IV. TEST SYSTEM SIMULATIONS

The test system i.e, distribution system with UPQC is depicted in Fig.6. The system values are: PCC line voltage: 415 V, 60 Hz; Nonlinear load: Bridge Rectifier with R-L: 10 Ω, 100mH; DC-bus Voltage: 700 V; DC-bus Capacitor: 15 mF; Interfacing Inductor of Shunt VSC: 2mH; Interfacing Inductor of Series VSC: 3mH; DC-bus PI Gains: Kp= 1000, Ki = 50; LPF cut-off frequency = 10Hz; BPF center frequency = 60Hz, Damping Ratio = 0.7.

To compensate the above mentioned issues which are causing the power quality degradation in the distribution system, at PCC UPQC is connected with necessary control mechanisms.

V. RESULTS

The Simulation results of various components of the distribution system under different conditions are presented as follows.
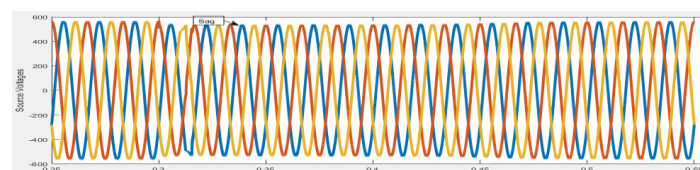
Fig. 6(a) Source Voltages
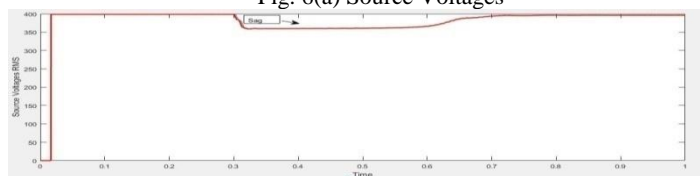
Fig.6(b) Source RMS Voltage

Fig.6(a)shows the source voltages under sag condition, initial peak voltage is 565.6V and when 10HP induction motor is connected at 0.3sec to 0.5secthe effect of sag has begun, and the instantaneous peak voltage is 537V. The percentage of dip in voltage is 7.6%. The same is depicted in the form of RMS value in Fig.6(b), the initial RMS is 400V and instantaneous RMS from 0.3sec to 0.5sec fell down to 380V.
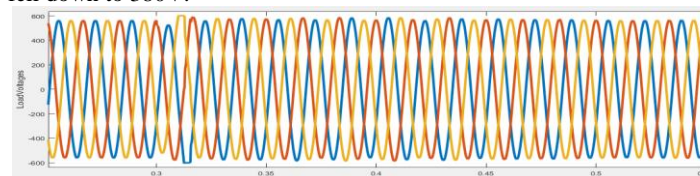
Fig.7(a) Load Voltages
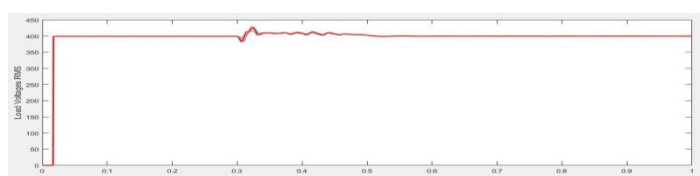
Fig.7(b) Load RMS Voltage

Fig.7(a) shows the load voltages under sag condition. The sag that occurred due to induction motor load has been compensated by connecting UPQC at PCC. The compensation starts from 0.31sec to 0.5sec, due to the transients the delay in UPQC response is 0.01sec and the percentage of compensation is 99.25% as the instantaneous peak voltage during sag is increased to 561.3V where the initial peak voltage is 565V. Fig.7(b) shows the load

RMS voltage under sag condition in which the voltage is increased to 397V from 380V during the sag period with a nominal RMS voltage of 400V.
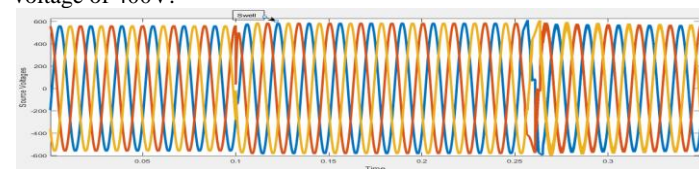
Fig.8(a) Source Voltages
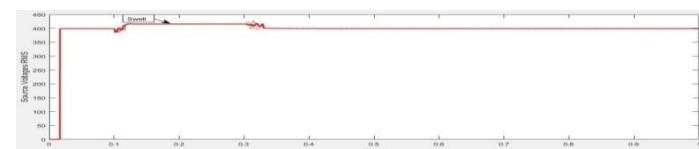
Fig.8(b) Source RMS Voltage

Fig.8(a) shows the source voltages under swell condition, initial peak voltage is 565.6V and when large Resistive load is disconnected at 0.1sec the effect of swell has begun, and the instantaneous voltage is 615V. The percentage of rise in voltage is 8.9%. The same is depicted in the form of RMS value in Fig.8(b), the source RMS is increased from 400V to 435V at 0.1 sec.
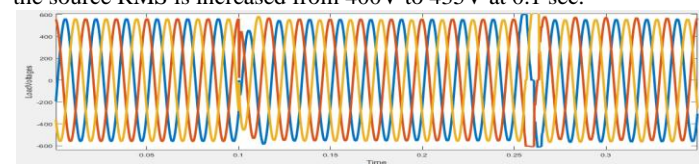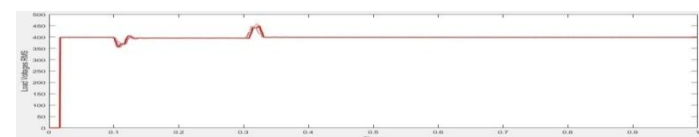

Fig.9(a) Load Voltages

Fig.9(b) Load RMS Voltage

Fig.9(a) shows the load voltages under swell condition. The swell that occurred due to switching off of largeresistive load has been compensated by connecting UPQC at PCC. The compensation starts at 0.11sec, due to the transients the delay in UPQC response is 0.01sec and the percentage of compensation is 99.5% as the instantaneous peak voltage during swell is decreased to 566V where the initial peak voltage is 565V. Fig.9(b) shows the load RMS voltage under swell condition in which the voltage is decreased to 398V from 435V during the swell period with a nominal RMS voltage of 400V.
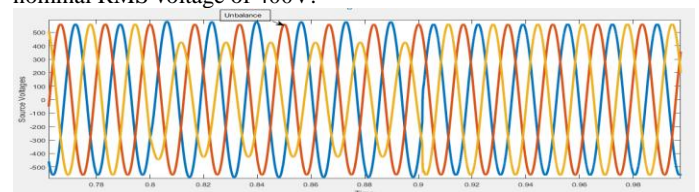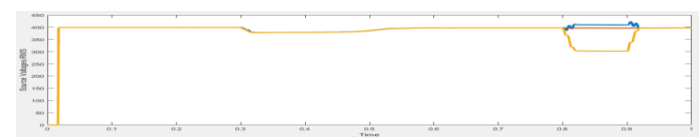

Fig.10(a) Source Voltages:

Fig.10(b) Source RMS Voltage

Fig.10(a) shows the source voltages under fault/unbalance condition, initial peak voltage is 565.6V and when a Single Line to ground fault is inserted at 0.8sec the effect of unbalance has begun,

and the instantaneous variation in three phase peak voltages is ranges from 537V to 594V. The percentage of variation is ranging from -4.9% to 4.9%. The same is depicted in the form of RMS value in Fig.10(b), the initial RMS is 400V and instantaneous variation in RMS from 0.8sec to 0.9sec is ranges from 380V to 420V.
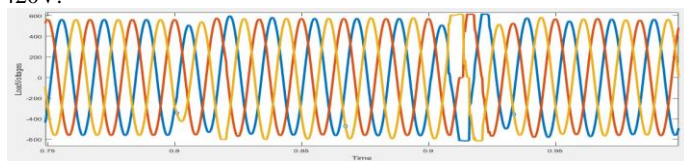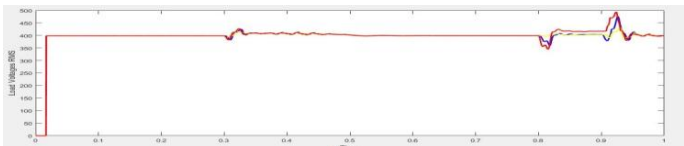

Fig.11(a) Load Voltages

Fig.11(b) Load RMS Voltage

Fig.11(a) shows the load voltages under fault/unbalance condition. The unbalance that occurred due to L-G fault has been compensated by connecting UPQC at PCC. The compensation starts from 0.81sec due to the transients the delay in UPQC response is 0.01sec and the percentage of compensation is 95% as the instantaneous peak voltages during fault, ranges from 558V-574V where the initial peak voltage is 565V. Fig.9(b) shows the load RMS voltage under fault/unbalance condition in which the voltage variation is minimized in the range of 395-406V during the fault period with a nominal RMS voltage of 400V.
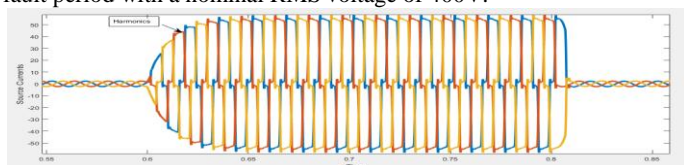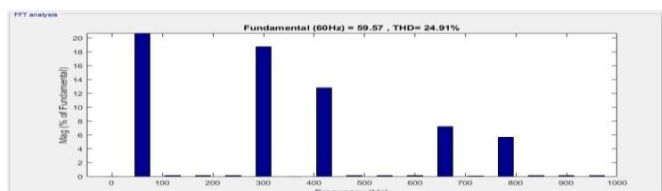

Fig.12(a) Source Currents

Fig.12(b) THD Spectrum of Source Currents

Fig.12(a) shows the source currents which involve harmonics from 0.6sec to 0.8sec due to the nonlinear load that has been connected at 0.6sec and removed at 0.8sec.Fig12(b) shows the THD spectrum of source currents from FFT analysis and the percentage of Total Harmonic Distortion is 24.92% which is measured at 0.75sec for 1 cycle.
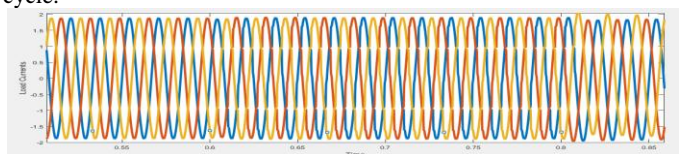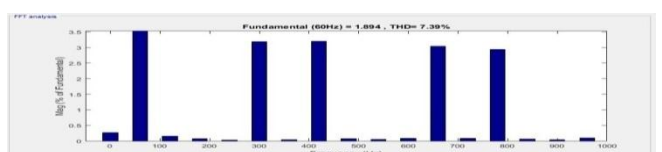

Fig.13(a) Load Currents

Fig.13(b) THD Spectrum of Load Currents

Fig.13(a) shows the load currents, in which the harmonics that are generated due to nonlinear load are reduced to a permissible level by the active power filter capability of UPQC. Fig13(b) shows the THD spectrum of load currents from FFT analysis and the percentage of Total Harmonic Distortion is 7.38% which is measured at 0.75sec for 1 cycle. The percentage of compensation by UPQC is 17.6%.

VI. CONCLUSION

This paper presented the detailed analysis of power quality problems in the distribution system and their mitigation. The Unified Power Quality Conditioner with proposed controller has compensated Sag/Swell, unbalance due to faults and also reduced harmonics thereby improved the current profile. The UPQC is having a response time of mere 0.01second. The performance of proposed system can be analyzed from fallowing table.

Table for Simulation Results Comparison

Nominal RMS: 400V

	Source Voltage-RMS (volts)	Load Voltage-RMS(volts)	%Compensation
Sag	380	397	99.25
Swell	435	398	99.5
Fault/ Unbalance	380-420	395-406	95

	Source Currents	Load Currents	%Compensation
THD	24.92%	7.38%	17.6

THD calculation is done at 0.75sec for 1 cycle

A. Future Scope

1. The UPQC applications can be further extended to various fields like industries, electrical drives etc,
2. The control strategies can be modified to robust methods.
3. Any Renewable energy source can be connected across the DC bus to make UPQC power supplier to the main distribution system

REFERENCES

[1] SachinDevassy and BhimSingh "Modified p-q Theory Based Control of Solar PVIntegrated UPQC-S", IEEE Trans. Industry Applications,2016.
[2] H. Rudnick, J. Dixon and L. Moran, Delivering clean and pure power,IEEE Power and Energy Magazine, vol. 1, no. 5, pp. 32- 40, Sep-Oct2003.
[3] H. Fujita and H. AkagiThe Unified Power Quality Conditioner: TheIntegration of Series- and shunt-active filters, IEEE Trans. PowerElectronics, Vol. 13, No. 2, pp. 315-322, 1998.
[4] Y. F. Wang and Y. W. Li, "Three-phase cascaded delayed signalcancellation pll for fast selective harmonic detection," *IEEE Trans. Ind.Electron.*, vol. 60, no. 4, pp. 1452–1463, April 2013.

[5] H. Akagi, E. H. Watanabe, and M. Aredes, "Instantaneous Power Theoryand Applications to Power Conditioning". Hoboken, NJ: Wiley-IEEEPress, Apr. 2007.

[6] H. Akagi, E. Watanabe, M. Aredes, *Instantaneous Power Theory andApplications to Power Conditioning*. New Jersey: Wiley, 2007.

[7] P. Kanjiya, B. Singh, A. Chandra, and K. Al-Haddad, "'SRF TheoryRevisited' to control self-supported dynamic voltage restorer (dvr) forunbalanced and nonlinear loads," *IEEE Trans. Ind. Appl.*, vol. 49, no. 5,pp. 2330–2340, Sept 2013.

[8] R. S. Herrera and P. Salmeron, "Present point of view about theinstantaneous reactive power theory," *IET Power Electronics*, vol. 2,no. 5, pp. 484–495, Sept 2009.

[9] M. Popescu, A. Bitoleanu, and V. Suru, "A dsp-based implementationof the p-q theory in active power filtering under nonideal voltageconditions," *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2,pp.880–889, May 2013.

[10] R. R. Pereira, C. H. da Silva, L. E. B. da Silva, G. Lambert-Torres, andJ. O. P. Pinto, "New strategies for application of adaptive filters in activepower filters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1136–1141,May 2011.

[11] S. Arya and B. Singh, "Performance of DSTATCOM using leaky LMScontrol algorithm," *IEEE Journal of Emerging and Selected Topics inPower Electronics*, vol. 1, no. 2, pp. 104–113, June 2013.

[12] B. Singh, S. R. Arya, A. Chandra, and K. Al-Haddad, "Implementationof adaptive filter in distribution static compensator," *IEEE Trans. Ind.Appl.*, vol. 50, no. 5, pp. 3026–3036, Sept 2014.

[13] S. Golestan, F. D. Freijedo, A. Vidal, A. G. Yepes, J. M. Guerrero, andJ. Doval-Gandoy, "An efficient implementation of generalized delayedsignal cancellation PLL," *IEEE Trans. Power Electron.*, vol. 31, no. 2,pp. 1085–1094, Feb 2016.