International Journal of Engineering and Manufacturing Science.
ISSN 2249-3115 Volume 7, Number 2 (2017), pp. 383-391

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Novel Fault Resistant D-Latch for Low Power VLSI Design

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Abstract

The novel digital VLSI circuit applications are increasing exponentially. Recent trends in the design of such circuits are to decrease the node capacitances and power supply requirements. Because of these requirements, huge susceptibility to transient faults increases in the nano-range digital CMOS designs. In this paper, we have constructed a new robust fault resistant D-latch for low power applications. D-latch has been designed with the combination of 1P-2N and 2P-1N three-transistor structures. In this design, if any transient fault affects one of the structure then it is corrected by the other structure. The novel circuit design protects store data information from transient faults which have appeared at the input node from the preceding circuits. An internal dual-feedback structure is used in this design. The proposed novel latch reduces average power consumption and reduces the Power Delay Product (PDP) as compared with the existing latch designs.

Keywords: - D-latch; Lower power consumption; Lower propagation delay; Power delay product; Transient faults.

1. INTRODUCTION

At present, in digital VLSI designs, the fast development in the CMOS technology marked more chances to fail current circuit designs. As long as the reduction in circuit node capacitances, less power supply requirements, reduction in charge and uppermost clock frequency increase circuit vulnerability to the glitches caused by radiation induced transient faults [1]. The transient fault arising in the latch are called soft errors. The soft error rate is prominently in nanometer CMOS designs [2]. As explained in the reference [3-4], mostly soft errors occurred in the memory portion of

the sequential circuits. [5-6]. As a result of this fact, researchers deal with troubles to come up with advanced approaches for flip flops and latch devices. Generally, redundancy used to protect flip-flops, latches and also combinational circuits. Redundant circuits provide the highest protection, but these circuits acquire large area, power and delay. Hardened circuit devices with increased stored charge are implied to scale down the soft errors in digital devices but at higher cost [7].

A lot of error tolerant approaches have been recommended for soft errors, which appear in digital logic circuits. To prevent memory components from transient faults, the parameters speed, area and power plays significant role. Consequently, for general purpose applications, data security from transient faults is very important. The soft errors by virtue of the transient faults, effects sampling element, therefore, transient fault tolerant latches and memory designs are recommended in [3, 7 and 8]. Few approaches modified the configuration of latches to make immune to soft errors [9-11]. Another approaches have modified, stored node capacitance and the width of the transistor in the device [12-13]. A few approaches adopt C-elements for transient fault tolerant circuits, all this type of existing methods can be found in [9, 10, 12, and 13]. The C-element has the ability to penetrate any type of change in the input node that is if any of the two inputs of the C-element are not equal, then the output will be in its past state; this is the very different property of the C-element.

In this paper, the existing designs are discussed in section 2. The proposed novel design is discussed in section 3. The simulation results and analysis are discussed in section 4 and conclusions are given in section 5.

2 EXISTING DESIGNS

M. Fazeli et al. [14], demonstrated a redundant, fault tolerant latch which modeled corresponding storage path and utilized C-elements to secure the output from the soft errors. Therefore, soft errors never disturb the output node. Whenever, a transient fault error arises in one of the nodes, the other internal output node goes into the high impedance state and therefore the preserved value of the output node will be saved. The designed latches in [14, 15], are not protected from transient faults propagated by an input terminal, even though the flip-flops and latches have to preserve combinational circuit against transient fault through the exclusion of glitches from their outputs. The authors [15] have presented, a low power fully protected CMOS latch design and utilized C-elements to secure the output from the soft errors, which represents a higher protection from transient faults with low power consumption for a tolerable amount of delay and transistor counts. The presented latch avoids propagating transient pulses which appeared in the input terminal of the circuit shown in fig. 1.

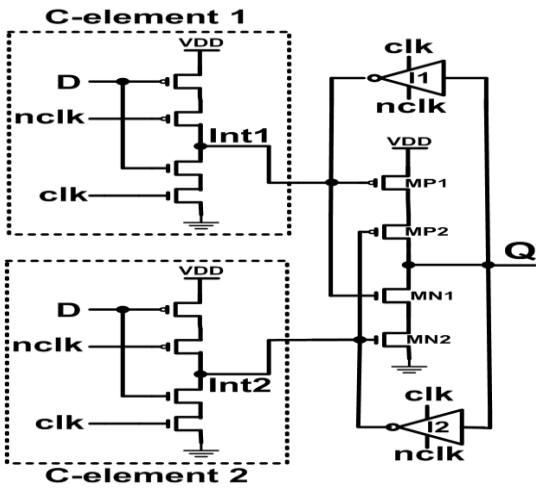


Figure 1: Protected CMOS latch [15].

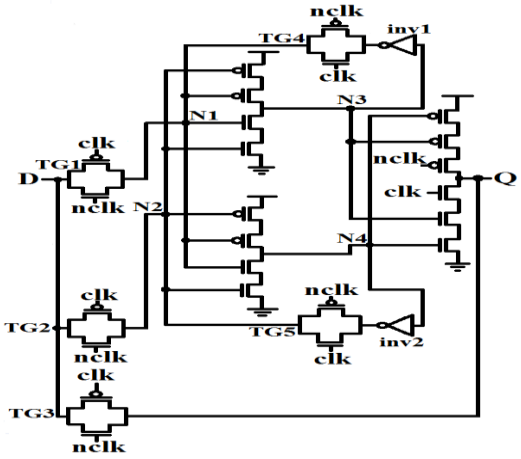


Figure 2: High Performance SEU tolerant latch [16].

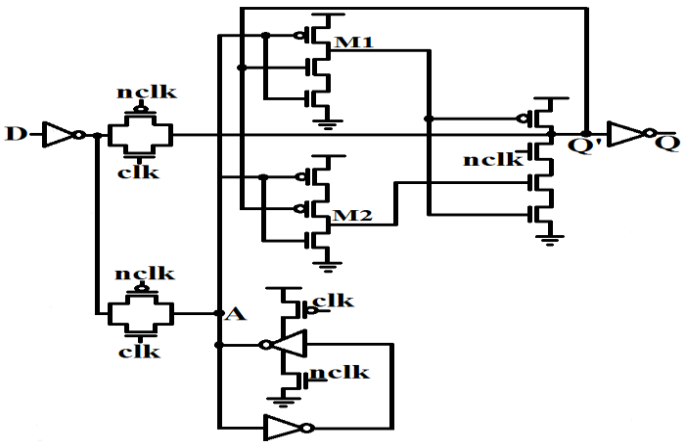
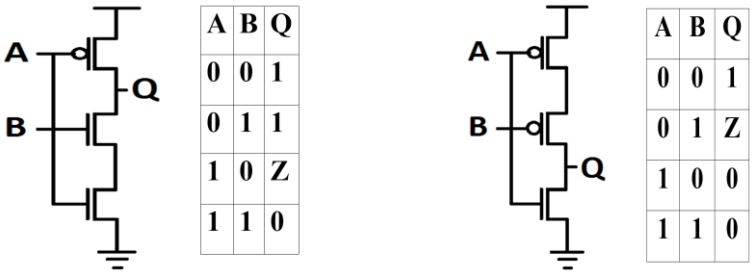


Figure 3: Soft error resistant latch construction [17].

The high performance SEU tolerant (HPST_L) latch [16] is symmetric and dual interlocked, as shown in fig. 2. This latch design can enhance robustness to reduce soft errors by using the C-element circuit. The high performance SEU tolerant latch consists of three C-element circuits that may make the known high impedance issue. To reduce single event upsets, the high performance SEU tolerant latch uses redundant feedback lines and C-element circuit. By using the clock gating at the output node, the high performance SEU tolerant latch decreases power consumption. It gains a tradeoff between power, reliability, area and performance [16]. The 3-transistor structures, 1P-2N and its opposite design 2P-1N, present an acceptable soft error rate performance in comparison to the other soft error tolerant latches [17]. The

soft error resistant latch construction (D1-V1_L) is shown in fig. 3. The 1P-2N and its opposite design 2P-1N structures carry a more adjustable trade-off between soft error rate, power dissipation, area and delay [17]. A lot of error tolerant approaches have been recommended for soft errors. The major parameters the speed, area and power consumption in latches and flip flops are very significant in the study of transient fault analysis. The schematic and the truth table of the 1P-2N and 2P-1N three-transistor structures are shown in fig. 4 [17]. In the 1P-2N and 2P-1N three-transistor structures, when the inputs are not equal then the output may not go to the high impedance state. These structures have three transistors.



A	B	Q
0	0	1
0	1	1
1	0	Z
1	1	0

A	B	Q
0	0	1
0	1	Z
1	0	0
1	1	0

(a) (b)

Figure 4: Structures and their truth tables (a) 1P-2N (b) 2P-1N [17].

3 PROPOSED NOVEL DESIGN

Today, the main motive of the researchers is to achieve small area, low power and high speed in the field of VLSI applications. Therefore, many more approaches have been considered by the researchers in VLSI designing to achieve these goal. The proposed advanced latch circuit model is shown in fig. 5.

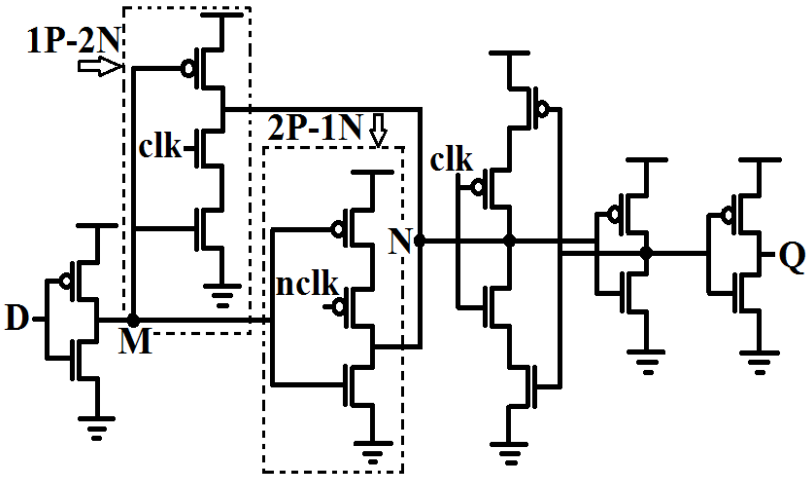


Figure-5: Proposed latch design.

The proposed design consumes less power and it takes care of the output from transient faults which appeared at the input of the circuit. The presented design is different from the design [17]. In the novel design, the dual feedback path is used but in [17], it is not used. The C-element circuit is used in [17] but in novel design, it is not used. The working of this design is as follows. The fault either filter or propagate to the output stage. If fault propagates to the output stage than it is filtered out through the feedback path. Assume that the initial state of nodes M and N to be M=0, N=1, output Q=1, and clk=0. At the node M, if any fault occurs from the preceding combinational circuit, the state of the node M will change from 0 to 1 and becomes M=1. Now M=1 and clk=0, the 1P-2N structure goes to the high impedance state, therefore, node N in its previous state that is N=1 and output Q=1. Consequently, there is no change in the output state.

Now the state of nodes M and N to be M=1, N=0, output Q=0, and clk=0. If any fault occurs at the node M then its value becomes M=0. For the 2P-1N structure, M=0 and clk=1 therefore, the 2P-1N structure goes to the high impedance state and node N in its previous state that is N=0 therefore, Q=0. Repeatedly there is no change in the output state. If any fault propagates to the output Q than it is filtered out through the feedback path. If any transient fault affecting one of the structure then it is corrected by the other one structure and get back to the original state. When clk=0, that is the latch mode, both the 1P-2N and 2P-1N structures are biased by the data input D and clocks are off and the output is retained by the feedback paths. The faulty input is omitted without any penalty in time, area and power consumption. If any error exists at the node N, then it cannot upset the output state. Consequently, the proposed novel latch is completely transient fault resistant and has high speed and high efficiency.

4 SIMULATION RESULTS AND ANALYSIS

The performance evaluation of the proposed novel latch is performed through the SPICE simulator and simulated in a Predictive Technology Model (PTM) 45 nm CMOS technology [18] with a power supply of 1V. Existing latches, which are discussed in the section 2, are also evaluated. The channel lengths of all of the transistors are fixed to 45 nm. The channel widths of the PMOS transistors are fixed to 630 nm and the channel widths of the NMOS transistors are fixed to 210 nm. The clock frequency is fixed at 500 MHz for the simulation results. For comparison with the existing models as discussed in section 2, we have set the above parameter values. The performance evaluation results are presented in table I. We note that the proposed novel circuit has the lowest power consumption as compared to other existing latches. Absolutely, the proposed novel design provides a safety measure by consuming lowest power. In the proposed novel latch, the delay is reduced; therefore, the speed of the proposed circuit is high.

Table-1: Result analysis of different D-latch designs.

Latch designs	Design in [14]	Design in [15]	Design in [16]	Design in [17]	Proposed latch
$P_{avg.cons.}$ (µW)	4.03	2.24	2.08	5.02	2.06
t_p (ps)	65.07	42.63	40.01	62.32	38.10
PDP (fJ)	0.262	0.095	0.083	0.299	0.078
No. of transistors	24	16	28	24	16

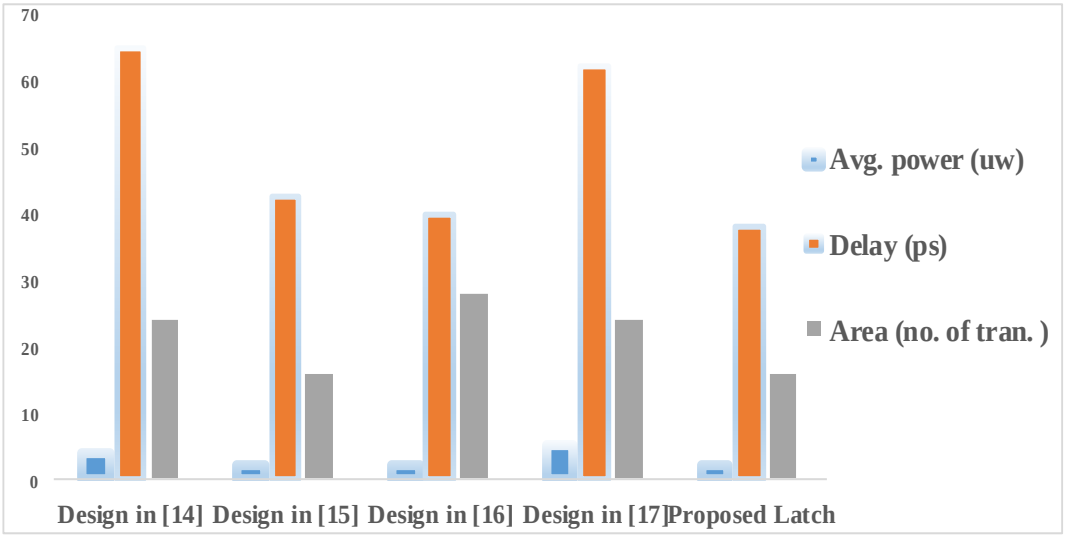


Figure-6: Power and delay comparison in different designs

The proposed design has the high performance with small area and number of transistors are less than the existing latches [14, 16, and 17]. Power Delay Product (PDP) is an essential parameter in digital designs. The delay, power and power delay product comparisons are given in table 1. The proposed novel latch has the lowest power delay product as compared to other existing fault tolerant latches. Consequently, the proposed novel latch has high efficiency in comparisons with other existing fault tolerant latches. The average Power consumption, propagation delay and area analysis for different transient fault resistant latches is shown in fig. 6, which shows that the proposed novel circuit design has the lowest power, smallest area and lower propagation delay in comparison with other existing fault resistant latches.

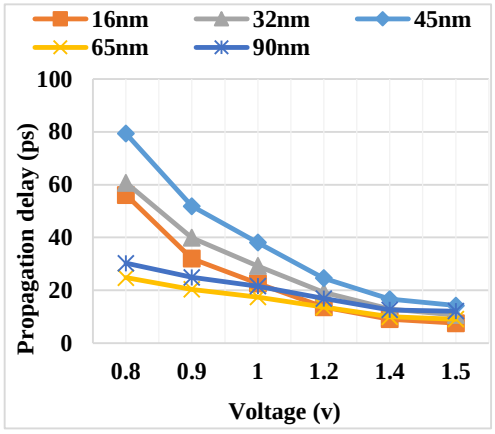


Figure-7: Delay analysis of proposed design at different supply voltage

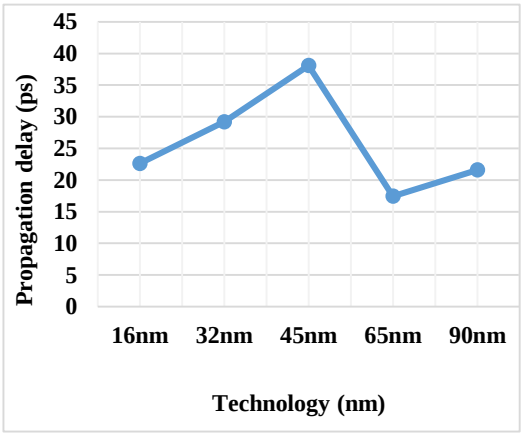


Figure-8: Delay analysis of proposed design at different technologies

The propagation delay of the proposed novel latch, in different technologies at the different supply voltages (from 0.8V to 1.5V), indicated in fig. 7. In all considered technologies, the delay decreases with the increase in the power supply voltage. The delay analysis plot of the novel latch, at different technologies, is plotted in fig. 8 that indicates the delay varies with the technology variations. The propagation delay of the proposed novel latch at different temperature values with different technologies is shown in fig. 9, which shows delay increases with the increase in the temperature in almost all discussed technologies. We also perform and analyze delay with frequency variations with different technologies as shown in fig. 10. The delay is found almost constant with change in frequency but varies with technologies.

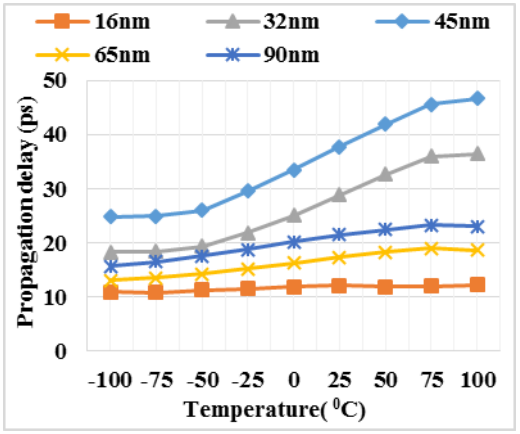


Figure-9: Delay analysis of proposed design at different temperatures.

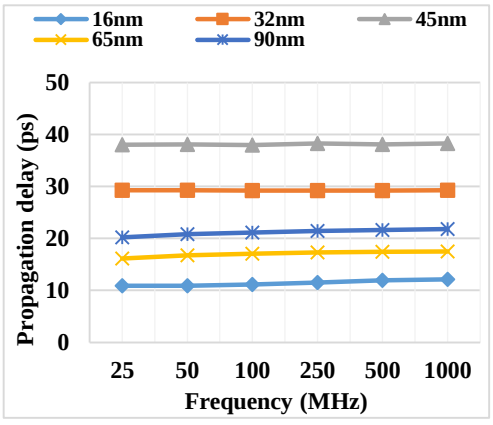


Figure-10: Delay analysis of proposed design at different frequencies.

CONCLUSION

This work presents a modified transient fault resistant D-latch for low power applications with 3-transistor 1P-2N and 2P-1N circuit models. The performance evaluation indicates that the proposed novel latch design provides protection from the transient faults with a reduction in average power consumption and the proposed design can save hardware resources as compared to the existing latches. The proposed design gives the little similar results as compared to [15] but consumes less power and provides better PDP. The novel design has the less number of transistors as compared to [16] and occupies small area. The proposed design has the low average power consumption, low delay and low PDP as compared to existing designs [14 and 17]. The presented design has lower delay and lower PDP as compared to existing latch designs.

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