

## Stitch-less Double Patterning Technology for Reduced Wire Length Three-layer Routing Solution

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### Abstract

Here we proposed lithography based layer decomposition for reduced wire length three-layer routing solution using Double Patterning Technology (DPT). First we proposed a routing algorithm of three-layer (HVH) restricted dogleg routing solution to minimize the wire length of the chip to be designed. Next we designed a layer decomposition algorithm of the obtained routing solution using DPT to increase the quality of printability on wafer. Finally, we showed that the proposed DPT based layer decomposition is stitch-less and it reduces overlay errors and line-end effects. This is the most acceptable solution using current lithography process for 32-nm node and beyond.

**Keywords:** Dogleg routing; double patterning technology; Optical lithography process; VLSI; Wire length minimization.

### INTRODUCTION

In the current scenario the chip size is go on decreasing whereas suitable lithography process is not developed so far. The extreme ultra violet (EUV) lithography process is not yet come into the market. So, double patterning technology (DPT) is the most acceptable solution using current lithography process for node size 32 nm and beyond [2,3,5,11]. In optical lithography process using the light of 193 nm wavelength particular patterns of the mask is printed on the photoresist wafer [1].

The quality of printability on tiny wafer decreases for dense patterns. So, to improve it, technology of double, triple and multi patterning comes into the picture [2,3,5,6,11]. In DPT patterns present on one layer is decomposed into two layers and using two step lithography process patterns are printed on tiny wafer one after another.

The problem of wire length minimization of three-layer (HVH) restricted dogleg routing and the problem of single layer double patterning is NP-hard [7,11]. Hence, heuristic algorithm to get the solution of these problems is highly acceptable. Here we proposed lithography based routing algorithm for three-layer (HVH) restricted dogleg reduced wire length routing solution.

On a chip, the space between different circuit blocks is the routing region or channel [7-10]. The terminals or pins are placed on the periphery of these blocks and these terminals are fixed for a particular chip. A set of terminals which will be connected together is called a net. We consider three-layer (HVH) Manhattan routing model where vertical layer (V) placed between two horizontal layers (H) and vertical and horizontal wire segments for interconnecting nets are to be placed in respective layers [7,10].

If net  $n_i$  is placed in track  $X_i$ , (for  $i = 1, 2, \dots, n$ ), the total number of tracks required to route the nets is  $TN$ , the total horizontal wire needed to route all the nets is  $\mathfrak{S}_H$  and  $s_i$  being the set of nets assigned to track  $X_i$  then the total wire length required for routing is as follows:

$$\sum_{1 \leq j \leq TN} \left[ \sum_{\forall i \in S_j} [X_i T_i + (TN - X_i + 1) B T_i] \right] + \mathfrak{S}_H$$

As the terminal positions of nets are fixed so, the total horizontal wire length  $\mathfrak{S}_H$  is fixed in a chip. Hence, reducing the vertical wire length of nets present on the chip is the only solution to reduce the wire length of the chip i.e., our first objective is to minimize the following expression.

$$\sum_{1 \leq j \leq TN} \left[ \sum_{\forall i \in S_j} [X_i T_i + (TN - X_i + 1) B T_i] \right]$$

DPT is cost effective compare to triple and multi patterning technology. The two main challenges of DPT is layout decomposition and stitch minimization. Somewhere adding some stitches it is manageable to decompose the patterns of single layer into two layers of patterns but, it increases overlay error which is caused by the mismatch between the first and second patterning. None of existing research work in the literature focuses on DPT without any stitch. This is the prime motivation to address the said problems.

### THREE-LAYER RESTRICTED DOGLEG ROUTING ALGORITHM:

Here we formulate the problem which reduces the total vertical wire length of three-layer (HVH) restricted dogleg routing solution. In restricted dogleg, horizontal wire segment of a multi-terminal net is splitted at columns where the terminals present and form subnets. Two nets  $n_i$  and  $n_j$  are horizontally constraint if they are overlap at least at one column. Subnets of a net are not horizontally constraint to each other that means they can be placed in one track during routing. Two nets  $n_i$  and  $n_j$  are vertically constraint if one terminal of each net placed at the opposite sides of one column. So,

they must not place in one track. Horizontal and vertical constraints are represented by *horizontal constraint graph (HNCG)* and *vertical constraint graph (VCG)*, respectively [7-10].

Now it is easier to handle subnets instead of nets for reducing the total vertical wire length as these are comparatively small in size. Doglegging removes the cyclic vertical constraints present in the channel. As we have two horizontal layers, so we may assign two sets of subnets on two different horizontal layers. Hence, it again reduces the total vertical wire length.

We construct *HNCG* and *VCG* by taking subnets as vertices. Now considering set of source (sink) vertices  $S$  of *VCG* and we find maximum weighted clique [4]  $C$  from induced subgraph of *HNCG* as algorithm designed in [8]. Then we assign its corresponding subnets into the current topmost (bottommost) track of the first horizontal layer. If  $S=C$ , then nothing to be remained for assignment to the same track of the second horizontal layer. If  $S-C$  is not null, then compute another maximum weighted clique among the vertices of  $S-C$  from the induced sub graph of *HNCG*. Then we place its corresponding intervals on the same track of the second horizontal layer. We continue this process unless and until all the subnets are assigned to the tracks.

## DOUBLE PATTERNING TECHNOLOGY BASED LAYER DECOMPOSITION

During lithography process the patterns of two horizontal layers (H) and one vertical layer (V) are to be printed on the wafer using the light of 193 nm wavelength. As the patterns of single layer is very dense to print in a single lithography process on the one layer of tiny wafer (node of 32 nm or less) so, single layer decomposition using DPT usually give the solution of the problem. Here we shall discuss about single layer (say, the first horizontal layer) decomposition algorithm of three-layer (HVH) routing solution.

We decompose the patterns (i.e. horizontal wire segment) present in the horizontal layer into two layers of pattern in such a way that patterns present in each odd track of the first horizontal layer of three-layer (HVH) routing solution are to be considered for the first patterning and patterns in the even track of the first horizontal layer of three-layer (HVH) routing solution are to be considered for the second patterning. As all the patterns present in two decomposed layers are rectangular in shaped so, decomposed layers do not contain any stitch. Hence, the layer decomposition using DPT for reduced wire length three-layer restricted dogleg routing solution is stitch-less. In similar way we can easily decompose the patterns present in the vertical layer and patterns present in the second horizontal layer of three-layer (HVH) routing solution into two layers of stitch-less patterns for each case.

As this method supports DPT without any stitch, hence it solves the problem of overlay errors which is mainly caused by the mismatch between the first and the second patterning. Another aspect of this method is it easily reduces line-end effect using optical proximity correction (OPC) [1].

## EXPERIMENTAL RESULTS

Here, we showed the experimental results obtained for three-layer restricted dogleg routing solution. We have implemented these algorithms using Dev C++ 4.9.9.1. We compare three-layer routing solution for benchmark channel instances [7] with the existing work in this model [7,10,12]. It is seen that the wire length reduces drastically for all the instances using the designed algorithm discussed in this paper. After obtaining reduced three-layer routing solution we have decomposed the patterns of each layer into two layers of patterns using stitch-less layer decomposing algorithm of DPT discussed earlier. Now this is ready for lithography process using node size 32 nm and beyond. We have showed the experimental results in Table 1.

**Table 1:** Experimental results computed for different channel instances available in [7], where A: Channel instance [7], B: Total vertical wire length required in computing the routing solutions using *TAH* for area minimization [7], C: Total vertical wire length required in computing the routing solutions using *TAH* for wire length minimization [7], D: Total vertical wire length required in computing routing solutions using algorithm developed by Yoeli [12], E: Total vertical wire length required in computing routing solutions using algorithm developed by Saha Sau *et al.* [10], F: Total vertical wire length required in computing the routing solutions starting from *TAH* for area minimization [7], G: Total vertical wire length required using proposed algorithm.

(A) Channel Instance	(B) VWL using TAH for area min [7]	(C) VWL using TAH for wl min [7]	(D) VWL using algo by Yoeli [12]	(E) VWL using algo by Saha Sau <i>et al</i> [10]	(F) VWL starting from TAH for area min [7]	(G) VWL using proposed algorithm
<i>Ex 1</i>	167	167	-	154	156	105
<i>Ex 2</i>	299	260	-	223	275	160
<i>Ex 3a</i>	365	355	306	310	338	263
<i>Ex 3b</i>	500	498	432	446	474	380
<i>Ex 3c</i>	594	577	329	520	557	303
<i>Ex 4b</i>	1105	1153	616	909	1017	521
<i>Ex 5</i>	857	786	601	557	728	387
<i>DDE</i>	3105	3077	1376	2988	3041	1245
<i>r1</i>	915	833	-	645	872	566
<i>r2</i>	637	558	-	537	549	476
<i>r3</i>	796	769	-	753	768	676
<i>r4</i>	982	948	-	825	927	556
<i>Ex 3b.1</i>	620	664	-	554	605	484
<i>Ex 3c.1</i>	604	577	-	432	552	369

## CONCLUSIONS

In this paper we have minimized the wire length of three-layer (HVH) restricted dogleg routing solution. The proposed algorithm reduces wire length compare to existing solutions using algorithms developed in literature. Then we have obtained stitch-less patterns using proposed layer decomposition algorithm of DPT which is most suitable for current lithography process. We have discussed the method of reducing line-end effect. We again conclude that similar stitch-less decomposition process is also applicable for reducing the wire length of reserved multi-layer Manhattan routing solution.

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