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The Pair-wise Bus-Invert Coding for Low-Power Bus Design

Myungchul Yoon

Department of Electronics Engineering, Dankook University, Cheonan, Korea
E-mail: myoon@dankook.ac.kr

Abstract.
A new bus-invert coding circuit called Pair-wise Bus-Invert Coding (PWBIC) is presented. PWBIC partitions a bus into a set of two-bit sub-buses, and applies the bus-invert algorithm to each sub-bus. One of two bus-lines in PWBIC is made to have quaternary states, so that a bit of coding information can be transmitted simultaneously with a data-bit. A transmitter circuit and a receiver circuit for the four-valued bus-line are presented. The performance of PWBIC is verified by simulations. According to the simulation results, PWBIC can reduce the number of bus transitions by about 49%. This performance is almost the same as that of the ideal BIC circuit, and it is double of that of the ordinary BIC circuit.

Keywords: Bus-Invert Coding, Low-Power Bus, Low-Power VLSI design, Reduced-Swing Bus.

Introduction

Power saving is one of the major concerns in mobile devices so that the interest in low power design has increased for the latest VLSI chip design. As the feature size decreases, the power consumed by individual circuits decreases, but the power dissipated in buses increases because more number of modules are attached to the buses. Therefore, the design of low-power bus is essential for low power VLSI design.

Bus-Invert Coding (BIC) [1] is a well-known general-purpose coding that decreases bus-power by reducing the number of bus-activations. The algorithm of BIC is simple; if sending a datum activates more than half of the bus-lines, its complement is transmitted to reduce the number of transitions. Because of its simplicity and usability, many enhanced BIC algorithms [2]-[9] have been developed. However, its performance and usability are limited by the method of sending coding information. To decode received data, the inversion state of the data, called *inv*-bit should be sent to receiver. Almost all of BI derivative algorithms [1]-[7] use an auxiliary line, called invert-line, to transmit an *inv*-bit. However, the invert-line has two major drawbacks. The first is the increase of bus-width due to the added line. The second is the performance degradation due to its transitions.

Some bus-activations are required to send the *inv*. These activations are the overhead of BI coding that should be paid to reduce the total number of transitions of the bus-lines. However, this overhead transition (OT) is the major factor degrading the performance of BI circuits. It is known that the invert-line generates many OTs so that it significantly degrades the performance of BI.

According to a theoretical performance analysis [9][10], the performance of BIC decreases with the increase of bus-width, therefore, a bus with large bus-width needs to be partitioned into several sub-buses with small bus-width. If no OT occurs, the maximum performance can be obtained when BIC is applied for the buses partitioned into 2-bit sub-buses. With a bus partitioned by 2-bit sub-buses, the theoretical analysis predicts that an ideal BIC implementation which generates no OTs can reduce bus transitions by 50% for independent data [9][10]. Under the same conditions, an ordinary BIC with invert-lines can reduce transitions of bus-lines by 50%, as well, but the invert-lines generate OTs by 25%. As a result, the net reduced transitions are only 25% which is just a half of the maximum achievable performance.

An implementation without invert-line is suggested in NIL-BIC (No-Invert-Line BIC) [8]. It sends the *inv* through the bus by using a special bus-driver called flip-driver. By employing Selectively Activated Flip Driver (SAFD) scheme, NIL-BIC suppresses the generation of OTs so that it can reduce bus transitions by 35%. However, the maximum achievable performance of NIL-BIC is limited to 35% due to a property of flip-driver [9].

A new BI implementation scheme without invert-lines, called Pair-wise Bus-Invert Coding (PWBIC) is presented in this paper. PWBIC transmits *inv*-bit by a special bus-line which can have quaternary states. A bus-driver circuit and corresponding decoder circuit for the four-valued bus-line are presented. With the quaternary transferable bus-line, PWBIC aims to minimize the influence of OT on bus-power dissipation so that its performance reaches as close as that of the ideal BIC.

Pair-wise Bus-Invert Coding

Since the performance of BIC is maximum for a 2-bit bus when no OT is generated, PWBIC focuses on the design of BIC circuits for 2-bit bus system with minimum influence of OTs. The structure of PWBIC is shown in Fig. 1. The basic block of PWBIC is a pair-bit bus-invert coding (PBBIC) circuit. A PBBIC consists of a pair of bus-lines, a two-bit BIC transmitter and receiver as in Fig. 1-(a). The Pair-wise BIC (PWBIC) for a bus with even buswidth ($2k$) is composed of k PBBICs. As described in Fig. 1-(b), 2k-bit of a datum is distributed to k-PBBICs by 2-bit per PBBIC, and each PBBIC transmits a pair of bits independently. For odd-line buses, one bus-line is omitted in coding.

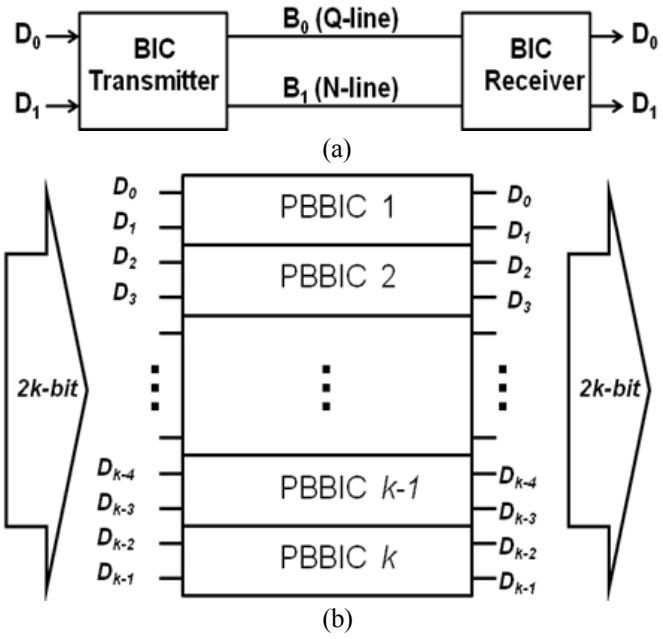

Figure 1: The structure of PWBIC (a) The structure of a pair-bit BIC (PBBIC) transmission bus (b) Configuration of PWBIC for 2*k*-bit bus.

To avoid bus-width increase, the coding information, *inv*-bit, is sent through one of the bus-lines instead of using an additional line. To send *inv* with a data-bit, one of the lines in PBBIC is made distinctive to have four possible states. The two bus-lines of a PBBIC are not identical. One of the two lines, named N-line, is a normal bus-line that carries one data bit. The other line, named Q-line, can have quaternary states so that it can carry two bits, one data bit and one bit of coding information (*inv*), simultaneously.

As in Fig. 2, the Q-line can have four possible states: 0, 1, I_0 (inverted 0), and I_1 (inverted 1). The Q-line is at 0 or 1 state when *inv*=0, but it moves inward slightly when *inv*=1. The voltage gaps between 1 and I_1 (Δ_H), and between 0 and I_0 (Δ_L) could be different, but equal size is preferable in general. The magnitude of Δ is closely related to the power dissipation of OT, so that it affects the performance of PWBIC greatly. The smaller Δ is, the better performance is achieved.

For performance enhancement, it needs to separate overhead transitions (OTs) from bus-transitions, and find a way to minimize the effect of OTs. For convenience, let us define the bus-transition as the transitions of bus-lines required to transmit data, and the OT as the transitions required to transmit coding information. Since the *inv* is transmitted through Q-line, all transitions of N-line are bus-transitions.

Among the transitions of Q-line, OTs can be distinguished from bus-transitions by comparing the waveforms of bus-lines between PBBIC and the ideal BIC. The transmission algorithm of PBBIC is simple. A pair of bits are transmitted in the inverted form only when both of the bits are different from the current value of bus-lines. In the comparison, the 1 and I_1 of PBBIC are considered as 1. Similarly, 0 and I_0 are considered as 0. Under the same transmission algorithm of PBBIC, the transitions of PBBIC and the ideal BIC are compared.

Because no OT exists in the ideal BIC, all transitions of the ideal BIC are bus-transitions. A transition of PBBIC is classified as a bus-transition if it is possible to find the matching transition in the transitions of the ideal BIC. If a transition cannot find the matching transition, it is classified as OT. However, the transition patterns of Q-line are more complicated than those of a normal bus-line, because the Q-line can transfer among four possible states. By observing the transitions of Q-line under the algorithm of PWBIC, some transition patterns of Q-line are observed. Even though Q-line can transit to any of four states, some transitions such as in Fig. 2-(b) never happen due to the transition rule of BI algorithm. In addition, the transitions of Q-line could be classified into three patterns as in Fig. 2-(c): direct transition (DT), via-transition (VT), and round transition (RT). A DT is a single transition between 0 and 1. A rising DT is a transition from 0 to 1, and a falling DT is a transition from 1 to 0. Both VT and RT are composed of two transitions involving one of I-states. A rising VT is a combination of two transitions, the first is from 0 to I_0, and the second is from I_0 to 1. It may stay I_0 for a while but it does not matter in the classification. A falling VT is a combination of an 1-to-I_1 transition and a following I_1-to-0 transition. A RT-0 is a combination of two transitions, the first is from 0 to I_0, and the second is transition from I_0 to 0. A RT-1 is a combination of an 1-to-I_1 transition and a following I_1-to-1 transition.

All DTs and VTs are included in bus-transitions but all RTs are considered as OTs. Comparing the transitions of Q-line and the counterparts of the ideal BIC, it is possible for every DT to find its matching transition, but it is impossible for RTs. Although it is not clear for VT to find its matching transition, it is possible in the sense of bus-power. From all transitions of the ideal BIC, let us remove the transitions matching to DTs of PBBIC, then there are some transitions left, which are related to VTs.

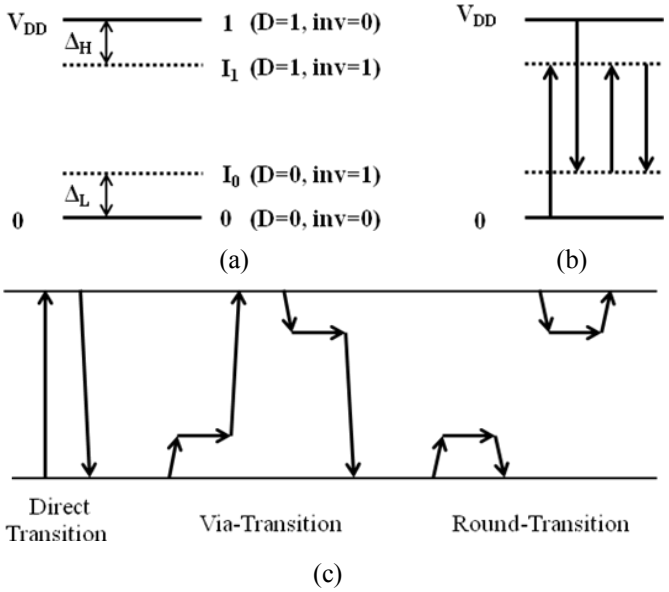

Figure 2: Transitions of Q-line (a) Four logic states of Q-line (b) Never happening transitions (c) Classification of transition patterns

For example, the transition-X of the ideal BIC in Fig. 3 can be matched to the VT-(*a*+*b*). Similarly, transition-Y can be matched

to the VT-(*c*+*d*). In this way, every VT of PBBIC can find a matching transition in the ideal BIC so that VTs are included in bus-transition. The bus-power dissipated for a VT is the same as that for a DT. For example, the bus-power dissipated for a rising DT is expressed by

$$P_{DT\uparrow} = \int_0^{V_{DD}} C_Q V dV = \frac{1}{2} C_Q V_{DD}^2 \quad (1)$$

where C_Q is the capacitance of Q-line. The dissipated bus-power for a rising VT such as (*a*+*b*) in Fig. 3 is

$$P_{VT\uparrow} = P_a + P_b = \int_0^{\Delta_L} C_Q V dV + \int_{\Delta_L}^{V_{DD}} C_Q V dV$$

$$= \int_0^{V_{DD}} C_Q V dV \quad (2)$$

This result is the same as Eq. 1. In the point of power dissipation, therefore, a VT can be matched to a DT. Note that the dynamic power for a VT is independent of the magnitude of Δ. Hence, the bus-power required to send data is independent of the voltage level of I_0 and I_1 state.

While the power-dissipation for bus-transitions is independent of the value of Δ, the power dissipated for OTs is dependent on it. The power dissipated for a RT-1 (*e*+*f*) in Fig. 3 is

$$P_{RT-1} = P_e + P_f = \frac{1}{2} C_Q \Delta_H^2 + \frac{1}{2} C_Q \Delta_H^2 = C_Q \Delta_H^2 \quad (3)$$

Likewise

$$P_{RT-0} = C_Q \Delta_L^2 \quad (4)$$

Comparing Eq. 3 and Eq. 4 to Eq. 1

$$P_{RT-1} = 2\left(\frac{\Delta_H}{V_{DD}}\right)^2 P_{DT} \quad (5)$$

$$P_{RT-0} = 2\left(\frac{\Delta_L}{V_{DD}}\right)^2 P_{DT} \quad (6)$$

Eq. 5 and Eq. 6 show that the power for OT is greatly affected by the magnitude of Δ.

Let denote P_T as the total power to transmit data, N_X as the total number of transitions of type X, and P_X is the power dissipation per transition of type X. If $\Delta_H = \Delta_L$, the total bus-power dissipation for PWBIC can be expressed by

$$P_T = N_{DT} P_{DT} + N_{VT} P_{VT} + N_{RT} P_{RT}$$

$$= \left[N_{DT} + N_{VT} + 2N_{RT} \left(\frac{\Delta}{V_{DD}}\right)^2 \right] P_{DT}$$

$$= N_{eff} P_{DT} \quad (7)$$

where N_{eff} is the effective number of total transitions. The total bus-power by OTs is given by

$$P_{OT} = 2N_{RT} \left(\frac{\Delta}{V_{DD}}\right)^2 P_{DT} \quad (8)$$

Eq. 7 implies that the performance of PWBIC is enhanced by reducing N_{eff}, and it can be achieved either by decreasing the number of RT or by making Δ as small as possible.

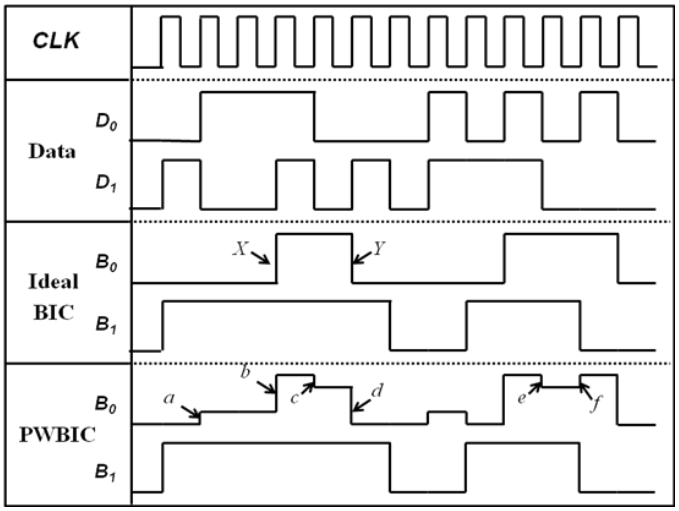

Figure 3: Comparison of bus-line waveforms between the ideal BIC circuit and PWBIC

Implementation of PWBIC

As shown in Fig. 1, a PWBIC is an array of PBBICs which operate independently. Therefore, the design of two-bit transmitter and receiver circuits for the PBBIC is all that is needed for PWBIC.

Transmitter Circuits of PBBIC

The transmitter circuits developed for PBBIC is depicted in Fig. 4. Fig. 4-(a) shows the encoder circuit of PBBIC. It has a 3-bit register (D flip-flops), and the entries of the register are named R_0, R_1, and R_{inv}. R_0 and R_1 store the values to be transmitted through the bus-lines B_0 and B_1 (let B_0 be Q-line, and B_1 be N-line). R_{inv} is used to store the values of *inv*. The register ensures the stability of inputs for the bus- driver circuit.

Because only a pair of bits exist in PBBIC, the decision logic is simple: inverted transmission occurs only when both of the two data bits (D_0 and D_1) are different from the current values of bus-lines (R_0 and R_1), i.e., the logic function for *inv* is

$$inv = (D_0 \oplus R_0) \cdot (D_1 \oplus R_1) \quad (9)$$

where ⊕ is the exclusive-OR operation.

The bus-driver circuit is depicted in Fig. 4-(b). The N-line is driven by a normal buffer, and the Q-line is, when *inv*=0, also driven by a normal buffer. When *inv*=1, the *I*-state generator circuit is activated and the Q-line goes to one of *I*-states. The V_{ref-H} and V_{ref-L} in the *I*-state generator circuit are set to the following values.

$$V_{ref-H} = V_{DD} - |V_{TP}| - \Delta$$
$$V_{ref-L} = V_{TN} + \Delta \quad (10)$$

where V_{TN} and V_{TP} are the threshold voltage of NMOS and PMOS transistors. As described in the Eq. 7, the smaller Δ results in the better performances. However, it affects other circuit characteristics so that a reasonable choice is a value in the range of $V_T/2 \le \Delta < V_T$.

The operation of *I*-state generator circuit is simple; it charges or discharges Q-line up to Δ. Note that, when *inv*=1, the data bit of

Q-line is not changed. Therefore, the Q-line transfers either from 1 to I_1 or from 0 to I_0. For example, if the previous state of Q-line is 1, R_0 is 1 so that the discharge path (the PMOS network) is opened, and the voltage of Q-line drops. When the voltage of Q-line reaches V_{DD} - Δ, the discharge path is closed by the PMOS gated by $V_{ref\text{-}H}$. From this point, the Q-line stays at a pseudo-floating state, i.e., both of the charging and discharging path are blocked. This property is used in the decoder circuit. Similarly, Q-line is charged up to Δ by the NMOS network if R_0 is 0, and stays at the pseudo-floating state.

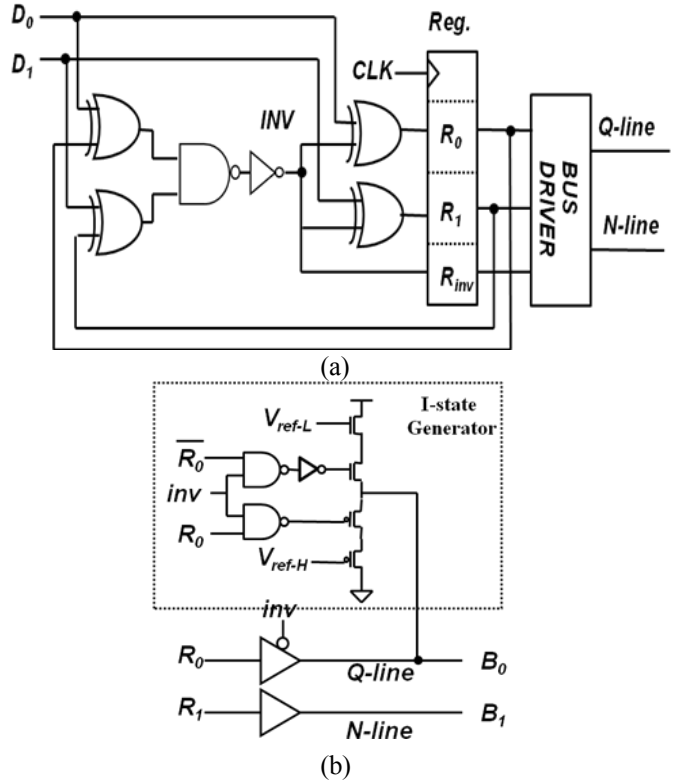

Figure 4: Transmitter circuits of PWBIC (a) Encoder circuit (b) Bus driver.circuit.

Receiver Circuits of PBBIC

Fig. 5 shows the receiver circuit for PBBIC. The decoder also has a 3-bit register. R_0, R_1, and R_{inv} are used to store the receive value of B_0, B_1, and *inv*, respectively. An inversion detector circuits is shown in Fig. 5-(b). The upper part of the circuit is I_0-detector which differentiates I_0 from 0 state, while the lower part is I_1-detector which differentiates I_1 from 1 state. If either I_0 or I_1 is detected, the *inv* becomes 1.

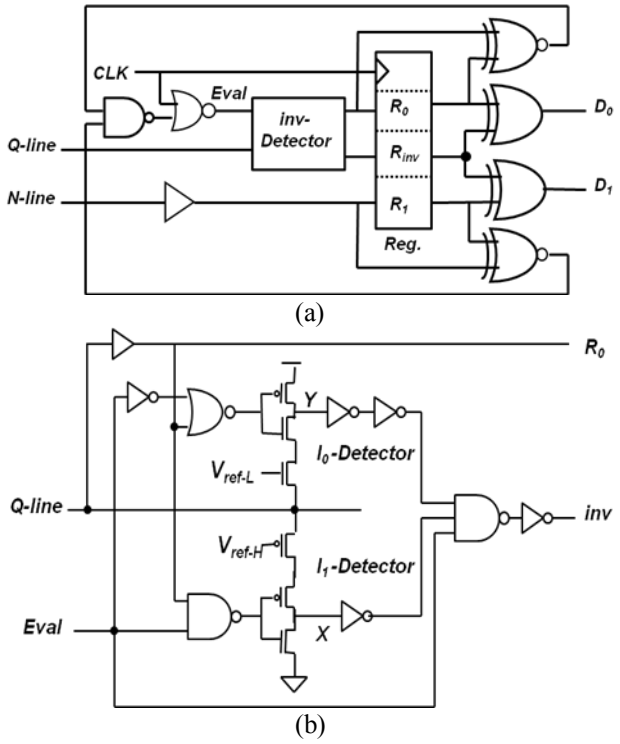

Figure 5: Receiver circuits of PWBIC (a) Decoder circuit (b) Inversion detector circuit.

The inversion detector circuit is activated only when the arrived bits, B_0 and B_1, are the same as the values stored in R_0 and R_1. If either one is different, *inv*=0. If activated, either I_0-detector or I_1-detector is activated by R_0. If R_0=1, I_1-detector is activated and operates as follows.

Before the detector circuit is activated, the node-*X* is preset to 0. The path from node-*X* to ground is closed as soon as it is activated, then the node-*X* either charged to V_{DD} or stay at the ground depending on the state of the Q-line. The difference between I_1 and 1 is that Q-line is floating in I_1 state while it is connected to V_{DD} in 1 state. When Q-line is in 1 state, it is connected to V_{DD} and the PMOS gated by $V_{ref\text{-}H}$ is in saturation region so that the node-*X* is charged to V_{DD}, and triggers the following inverter. When Q-line is in I_1, however, the Q-line is in the floating state and the PMOS is in cut-off region so that node-*X* is left uncharged. Therefore, the following inverter is not triggered which results in the different output from the output when Q-line is in 1 state. By this way, the I_1-detector distinguishes I_1 from 1.

Similarly, the node-*Y* is pre-charged to V_{DD} before the I_0-detector is activated. When activated, the node-*Y* either discharges to ground or stays at V_{DD} depending on the state of Q-line. Hence, it can distinguish I_0 from 0.

Experiments

The operation of transmitter and receiver circuits is verified by SPICE simulation. Fig. 6 shows the simulation result of the Q-line driver (I-state generator) circuit. The simulation is performed by HSPICE with IBM's "1.2V-0.13μm 8RF-LM" model parameters [11]. The threshold voltage of MOS transistor is V_{TN} = -V_{TP} = 0.3V. The outputs of reference voltage generators

are $V_{ref\text{-}H}$ = 0.7V and $V_{ref\text{-}L}$ = 0.5V. According to the Fig. 6, $\Delta \approx$ 0.2V, so that $(\Delta/V_{DD}) = 1/6$.

The performance of PWBIC is estimated by measuring the number of bus-transitions and that of OTs through simulations. For the application to multimedia VLSI chips, some audio and video files are used in the simulations. The experiments are carried out with 9 different files. Three of them are random binary files generated by a random number generator. The other three are music files of the MP3 format: "Gangnam Style (Psy)", "Let It Go (Idina Menzel)", and "Young Girls (Bruno Mars)". The other three are movie trailers of the MP4 format: "Frankenstein", "Frozen", and "Robocop".

The simulations count the number of transitions of bus-lines during the transfer of each file through 16-bit, 32-bit, 64-bit and 128-bit buses. The performance of PWBIC is compared to that of the ordinary BIC which uses invert-lines. The ordinary BIC is partitioned into 2-bit sub-buses like PWBIC. For both of the BIC schemes, the number of bus-transitions (N_B) and the number of overhead transitions (N_{OT}) are measured through simulations. For PWBIC, the number of rising VT, falling VT, RT-0, and RT-1 are counted separately, and then N_B, N_{OT} are calculated by the numbers. The effective total number of transitions (N_{eff}) is calculated by

$$N_{eff} = N_B + N_{OT} \text{ (for ordinary BIC)}$$

$$N_{eff} = N_B + 2N_{RT}(\Delta/V_{DD})^2 \text{ (for PWBIC)}$$

The effective number of OTs for PWBIC is

$$N_{OTe} = 2N_{RT}(\Delta/V_{DD})^2 \quad (11)$$

The simulations results are shown in Table 1. The averaged values are used to simplify the table; the values in the columns of the bin, mp3, and mp4 represent the average of the three files of the same format for random binary, mp3, and mp4, respectively. For convenience, all numbers are normalized by N_{RAW} which is the total number of bus transitions without applying any BI algorithm. The normalized value of N_X is denoted by n_X. $(=N_X/N_{RAW})$. According to the simulation result in Fig. 6, (Δ/V_{DD}) = 1/6 is used in the calculation of n_{OTe} and n_{eff} for PWBIC. The reduction ratio R $(=1\text{-}n_{eff})$ represents what percent of N_{RAW} is reduced by the applied BIC scheme, so that it can be used as the performance of the scheme.

As we can see in Table 1, there is no significant performance difference among the three data formats. The ordinary BIC can reduce bus transitions by 25% at the expense of a 50% increase of bus width. The reduction ratio of PWBIC is about 49%, which is almost double the reduction ratio of the ordinary BIC. And it is very close to that of the ideal BIC.

Table 1: Experimental results (unit: %)

Bus Width (bit)			16			32			64			128		
File Format			.bin	.mp3	.mp4	.bin	.mp3	.mp4	.bin	.mp3	.mp4	.bin	.mp3	.mp4
Ordinary BIC		n_B	49.92	50.22	50.02	50.40	50.43	50.02	49.99	50.39	50.01	49.70	50.41	50.00
		n_{OT}	25.04	24.89	24.99	24.80	24.78	24.99	25.01	24.81	24.99	25.15	24.80	25.00
		n_{eff}	74.96	75.11	75.01	75.20	75.21	75.01	75.00	75.20	75.00	74.85	75.21	75.00
		R	25.04	24.89	24.99	24.80	24.79	24.99	25.00	24.80	25.00	25.15	24.79	25.00
PWBIC	BT	DT	43.76	44.07	43.78	44.23	44.27	43.78	43.82	44.20	43.76	43.46	44.19	43.75
		VT ↑	3.07	2.91	3.12	3.11	2.93	3.12	3.10	2.97	3.12	3.25	2.98	3.12
		VT ↓	3.10	3.23	3.12	3.08	3.23	3.12	3.09	3.23	3.12	3.10	3.24	3.12
		n_B	49.92	50.22	50.02	50.42	50.43	50.02	50.01	50.39	50.01	49.81	50.40	50.00
	OT	RT-0	6.30	6.49	6.25	6.32	6.47	6.25	6.26	6.49	6.25	6.37	6.44	6.25
		RT-1	6.32	5.98	6.24	6.16	5.94	6.24	6.21	5.91	6.25	6.13	5.95	6.25
		n_{RT}	12.62	12.46	12.50	12.49	12.41	12.49	12.47	12.40	12.50	12.50	12.39	12.50
		n_{OTe}	0.70	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69	0.69
		n_{eff}	50.62	50.91	50.71	51.12	51.12	50.72	50.70	51.08	50.70	50.50	51.09	50.69
		R	49.38	49.09	49.29	48.88	48.88	49.28	49.30	48.92	49.30	49.50	48.91	49.31

The discrepancy of the reduction ratio comes from the difference of n_{OT}. Note that, n_B of PWBIC and that of the ordinary BIC are almost the same. Both schemes reduce bus-transitions by 50%. However, the n_{OT} of the ordinary BIC is about 25% which is about half the number of the reduced transitions. Therefore, in the ordinary BIC, about 50% of the performance is lost by the transitions of the invert-lines. However, the effective number of OTs for PWBIC, n_{OTe}, is only 0.7%. The big difference of n_{OTe} results in such a big performance difference between PWBIC and

the BIC with invert-lines. As expected from Eq. 11, the small value of (Δ/V_{DD}) plays a great role in reducing n_{OTe}.
Theoretically, the maximum reduction ratio achievable by the BI algorithm is 50%. The reduction ratio of PWBIC is about 49%, which is only 1% smaller than the theoretical maximum reduction ratio. This shows that PWBIC effectively reduces the influence of OTs on bus power dissipation.

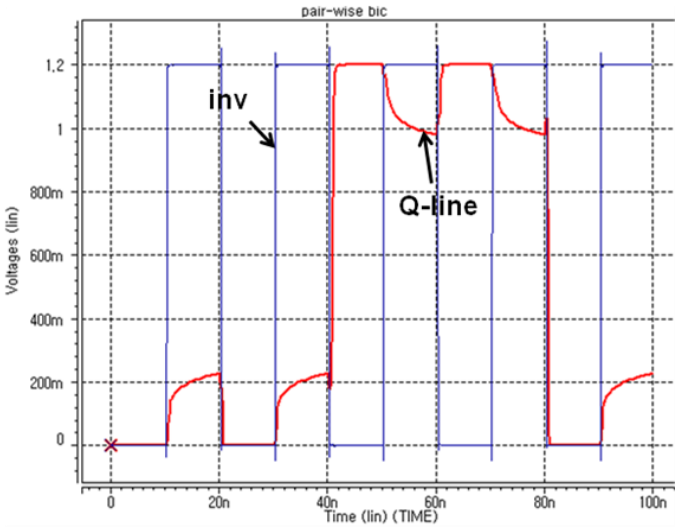

Figure 6: A waveform of the Q-line by simulation.

Conclusion

A new bus-invert coding circuit called PWBIC (Pair-wise Bus-Invert Coding) is presented in this paper. PWBIC intends to remove the problems of the invert-line and to achieve the performance that is close to the theoretical maximum performance of the BI algorithm. PWBIC sends the coding information through bus-lines instead of using invert-lines. To achieve the maximum performance, PWBIC focuses on the design optimization of 2-bit bus BIC circuit, since the performance of BI algorithm is maximum when it is applied to a 2-bit bus. For a bus with a larger bus-width, the bus is partitioned into a set of 2-bit sub-buses, and PWBIC is applied independently to every sub-bus. To send an *inv*-bit through a bus-line, one of two bus-lines is designed to have four logic states: 0, 1, I_0 and I_1. The encoder and the decoder circuits for the line with four logic states are presented.
The performance of PWBIC is verified by simulations. The simulation results show that the magnitude of Δ, the voltage difference between 1 and I_1 state, is very important in reducing the effective number of OTs. For the transmission of independent data, PWBIC can reduce bus-transitions by 49% when $(\Delta/V_{DD})=1/6$. This reduction ratio is about double that of the ordinary BIC using invert-lines. Furthermore, it is almost the same as the reduction ratio of the ideal BIC.

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