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2-D Analytical Modeling and Simulation of Dual Material Surrounding Gate Tunnel Field Effect Transistor with halo doping

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Abstract
In the nano regime, many non-classical MOSFETs have been proposed as device structures to meet with high packing density and increased performance. But TFETs are out beating due to its sub-60mV/dec sub threshold swing and low leakage current. A novel design of TFET namely Halo Dual Material Surrounding Gate Tunnel Field Effect Transistor (H-DMSGTFET) is proposed and analyzed in this paper with extensive analytical modeling and simulation approaches. The depletion region gets decreased with halo pocket implantation in the proposed model and shows improved ON current. Short channel effects are greatly deteriorated. Analytical modeling of the surface potential, lateral electric field, vertical electric field and drain current is developed for the new halo doped device using parabolic approximation method and its validity is assured by comparing it with Sentaurus TCAD simulation results, in which a good agreement is observed.

Keywords— TFET, Tunneling, Halo doping, Short channel effects, Dual material Surrounding gate.

I. INTRODUCTION

Due to downscaling of semiconductor devices, short channel effects and high leakage current become the bottle neck to circuit designers. Alternate novel designs to overcome this issue have been investigated. TFETs are promising devices for low power logic design due to low subthreshold swing (SS) and high Ion/Ioff ratio, thus out beating the MOSFET's physical limitation. TFET architecture attracts researcher's interest in the recent years and there have been many simulation reports on TFET [1-7]. However, for exact evaluation and study of electrical characteristics of TFET analytical modeling study is very crucial. But there are only few works on analytical solutions to model TFET and these include single gate structure [8], dual material gate structure [9], dual material double gate structure [10]. Rakhi Narang et al reported on drain current model of GAA p-n-p-n TFET [11]. M. G. Bardon et al reported a pseudo two dimensional modeling of double gate TFET [12]. Short channel effects such as threshold voltage roll off, DIBL can still be suppressed by increasing the channel doping through halo or pocket implants and few works on halo doped MOSFETS have been reported [13-15]. In the present work, a novel design of TFET namely Halo Dual Material Surrounding Gate Tunnel Field Effect Transistor (H-DMSGTFET) is proposed and analyzed for the first time. The attractive features of TFET and dual material surrounding gate with halo doping, are combined to form this novel structure. Surrounding gate structure proves the best among the various other structures with its fascinating features like high packing density, good gate electrostatic control over the channel potential profile resulting in improved sub-threshold characteristics and excellent immunity against undesired short channel effects. A heavily doped n + pocket implantation at the source end of the channel is expected to reduce the depletion width of the tunneling junction resulting in a considerable increase in the tunneling current. Also, the variation in the gate material work function leads to a step up potential profile near the interface of the two metals. When the drain voltage exceeds the drain saturation voltage, the excess voltage is absorbed by the gate metal M2, thus screening the drain field from penetrating into the channel. This step potential is thus responsible for lower leakage current and reduced DIBL effects.

II. MODEL FORMULATION

The cross sectional view of the Halo Dual Material Surrounding Gate TFET is shown in Fig.1. The Dual Material Surrounding Gate TFET consists of two gate material of different work functions. In this DMSG structure, halo doping is introduced for the first time to form a novel device structure called Halo Dual Material Surrounding Gate (H-DMSGTFET). The source and drain is made up of highly doped p-type and n-type regions respectively. The intrinsic channel region is made up of a moderately doped n-type material. The total length L is divided into L1, L2 and L3. L1 is the length of the halo doped region at the source end, under gate metal M1 with doping concentration N_h. L2 and L3-L2 are the lengths of gate metals M1 and M2 with varying work functions chosen between 4 – 4.8 eV. The other regions are doped with doping concentration N_c and in order to increase the carrier mobility, halo doping concentration should be greater than intrinsic channel concentration ($N_h > N_c$). With the halo doped dual material

gate structure, the model is divided into three regions namely region1 under halo implant inserted in gate metal M1, region2 under gate metal M1 and region3 under gate metal M2. The analytical modeling is done by considering different equations for three regions.

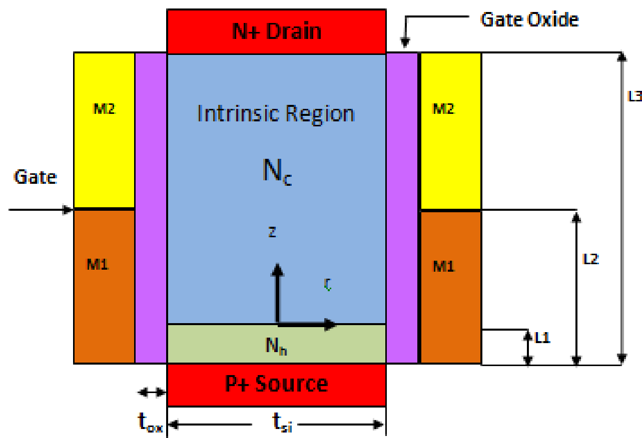

Fig.1. Schematic Cross Section of Halo doped Surrounding Gate Dual Material Tunnel FET (H-DMSGTFET)

III. BOUNDARY CONDITIONS

According to the cylindrical symmetry of the device structure, the coordinate system consists of radial direction r, vertical direction z and an angular component θ in the plane of the radial direction. The potential and electric field have no variations with respect to the angle θ along the radial direction, due to the symmetry of the device structure. Hence, a two-dimensional analysis is sufficient for the modeling of the proposed structure. The surface potential and electric field distribution can be derived by solving the Poisson's equation in the silicon pillar. The influence of the charge carriers and fixed oxide charges on the electrostatics of the channel is neglected. The potential profile is assumed to be parabolic along the radial direction, and the 2-D Poisson's equation for the potential distribution in cylindrical co-ordinates [16] is given by,

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial\phi_j(r,z)}{\partial r}\right)+\frac{\partial^2\phi_j(r,z)}{\partial^2 z}=\frac{qN_j}{\varepsilon_{si}}$$

$$L_{j-1}\le z<L_j, 0\le r<t_{si}/2, j=1,2,3 \quad (1)$$

where ε_{Si} is the dielectric constant of silicon pillar, $N_1 = N_h$, $N_2 = N_c$, $N_3 = N_c$, $L_0 = 0$, $L_1 = L_h$, $L_2 = L-L_h$, $L_3 = L$, $\phi_j(r,z)$ is the potential distribution.

The potential profile in the vertical direction can be approximated by a simple parabolic function given by

$$\phi_j(r,z)=c_{j0}(z)+c_{j1}(z)r+c_{j2}(z)r^2 \quad (2)$$

$$(L_{j-1}\le z<L_j, 0\le r<t_{si}/2, j=1,2,3)$$

where the arbitrary coefficients $c_{j0}(z)$, $c_{j1}(z)$ and $c_{j2}(z)$ are functions of z only. The Poisson's equation is solved separately for three regions by using the boundary conditions stated below.

(i) The electric field at the center of the silicon pillar is zero

$$\left.\frac{\partial\phi_j(r,z)}{\partial r}\right|_{r=0}=0=C_{j1}(z) \quad (3)$$

(ii) The channel surface potential is

$$\phi_{Sj}(z)=\phi(t_{si}/2,z)=C_{j0}(z)+C_{j2}(z)t_{si}^2/4 \quad (4)$$

(iii) The electric flux at the S_i/S_iO_2 interface is continuous, so we have:

$$\left.\frac{\partial\phi_j(r,z)}{\partial z}\right|_{r=\frac{t_{si}}{2}}=\frac{C_f}{\varepsilon_{si}}\left(\psi_G-\phi_{Sj}(z)\right)=C_{j2}(z)t_{si} \quad (5)$$

where $C_f = 2\varepsilon_{ox} / [t_{si}\ln(1+(2t_{ox}/t_{si}))]$,

$\psi_G=V_{GS}-\varphi_m+\chi+E_g/2$

ε_{ox} is the dielectric constant of the gate oxide, t_{ox} is the thickness of the gate oxide, V_{gs} is the gate to source voltage.

A. *Surface Potential*

The differential equations for potential distribution are obtained by substituting the boundary conditions (3) – (5) in Eq. (2)

$$\frac{d^2\phi_{Sj}(z)}{dz^2}-\lambda^2\phi_{Sj}(z)=\beta_j,\quad j=1,2,3 \quad (6)$$

where $\lambda=\sqrt{4C_f/(\varepsilon_{si}t_{si})}$ and $\beta_j=qN_j/\varepsilon_{si}-\lambda^2\psi_G$

Equation (6) represents the second order differential equation with constant coefficients, and the general solution for surface potential is

$$\phi_{Sj}(z)=A_je^{-\lambda z}+B_je^{\lambda z}-\frac{\beta_j}{\lambda^2}$$

$$(L_{j-1}\le z<L_j, j=1,2,3) \quad (7)$$

The coefficients A_j and B_j can be determined using the following boundary conditions.

(i) The potential at the source end is:

$$\phi_{S1}(t_{si}/2,0)=\phi_{S1}(0)=V_{bis} \quad (8)$$

where V_{bis} is the built in potential at the source side, N_A is the acceptor concentration at the source side, K is Boltzman constant and T is temperature.

(ii) The potential at the drain end is:

$$\phi_{S3}(t_{si}/2,L_3)=\phi_{S3}(L_3)=V_{bid}+V_{ds} \quad (9)$$

where V_{bid} is the built in potential at the drain side, N_D is the donor concentration at the drain side, V_{ds} is the applied drain to source bias.

(iii) The surface potential and electric flux at the interfaces between regions 1, 2 and 3 are continuous

$$\phi_j(t_{si}/2,L_j)=\phi_{j+1}(t_{si}/2,L_j) \quad (10)$$

$$\left.\frac{\partial \phi_j({}^{t_{si}}\!/_2, z)}{\partial z}\right|_{z=L_j} = \left.\frac{\partial \phi_{j+1}({}^{t_{si}}\!/_2, z)}{\partial z}\right|_{z=L_j} \tag{11}$$

By using equations (8)-(11) and substituting L_3 with L, constants A_j and B_j can be obtained as

$$B_1 = \frac{V_{bid} + V_{ds} + \gamma_2\omega_2 + \frac{\beta_3}{\lambda^2} + \gamma_1\omega_1 - \frac{\beta_1}{\lambda^2} e^{-\lambda L} - V_{bis}e^{-\lambda L}}{2\sinh(\lambda L)} \tag{12a}$$

$$A_2 = V_{bis} + \frac{\beta_1}{\lambda^2} - B_1 - \frac{\gamma_1 e^{\lambda L_1}}{2} \tag{12b}$$

$$A_1 = V_{bis} + \frac{\beta_1}{\lambda^2} - B_1 \tag{12c}$$

$$A_3 = V_{bis} + \frac{\beta_1}{\lambda^2} - B_1 - \frac{\gamma_2 e^{\lambda L_2}}{2} - \frac{\gamma_2 e^{\lambda L_2}}{2} \tag{12d}$$

$$B_2 = B_1 - \frac{\gamma_1 e^{-\lambda L_1}}{2} \tag{12e}$$

$$B_3 = B_2 - \frac{\gamma_2 e^{-\lambda L_2}}{2} \tag{12f}$$

where,

$$\gamma_1 = \frac{\beta_1 - \beta_2}{\lambda^2} \qquad \gamma_2 = \frac{\beta_2 - \beta_3}{\lambda^2}$$

$$\omega_1 = \cosh(\lambda(L - L_1)) \quad \omega_2 = \cosh(\lambda(L - L_2))$$

B. *Electric Field*

The electric field pattern along the channel determines the electron transport velocity through the channel. By differentiating the surface potential obtained (7), we get the electric field distribution along the channel length. The lateral electric field is obtained as

$$E_{zj} = \frac{\partial \phi_{Sj}(r,z)}{\partial z} = -\lambda A_j e^{-\lambda Z} + \lambda B_j e^{\lambda Z} \quad ; j = 1, 2, 3 \tag{13}$$

The vertical electric field E_r is given as

$$E_r = \frac{\partial \phi_s(r,z)}{\partial r} = 2C_{j2}(z)r \tag{14}$$

C. *Drain Current*

The drain current I_{ds} is based on the band to band tunneling of electrons and is obtained by the integration of the band to band generation rate G_{btbt} over the volume of the device [17].

$$I_{ds} = q\int G_{btbt} dV \tag{15}$$

The tunneling generation rate is first calculated using both the lateral and vertical electric field distribution and tunneling current is then obtained by integrating the generation rate G_{btbt} over the volume of the TFET structure.

IV. RESULTS AND DISCUSSIONS

With the results of analytical modeling, the performance of H-DMSGTFET is analyzed in terms of surface potential, lateral electric field, vertical electric field distribution, drain current. The accuracy of the analytical model is compared with the two-dimensional device simulation using the commercial technology computer aided design (TCAD Sentaurus) simulator [18]. Calculated surface potential, lateral electric field, and vertical electric field and drain current are excellently matching with the simulated results.

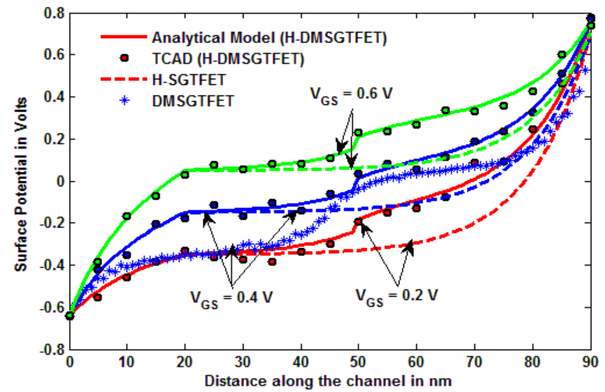

Fig.2.Surface potential along the channel for different gate to source bias voltage with V_{DS} = 0.6 V.

Also, the simulation results of H-DMSGTFET are compared with the performance of Halo Surrounding Gate TFET(H-SGTFET) and Dual Material Surrounding Gate TFET(DMSGTFET) and the investigated H-DMSGTFET exhibits improved electrical characteristics than its counterparts. The model parameters used are $N_D = 5\times10^{18}$ cm^{-3}, $N_A = 10^{20}$ cm^{-3}, $N_h = 3 \times 10^{17}$ cm^{-3}, $N_c = 4 \times10^{16}$ cm^{-3}, t_{ox}= 3.5 nm, t_{si} = 30 nm, L1= 20 nm, L2 = 70 nm, L = 90 nm. The surface potential distributions of H-DMSGTFET, H-SGTFET and DMSGTFET for different gate to source voltages V_{GS} along the channel are plotted in Fig. 2.It is clearly seen that as the gate to source bias voltage increases, the potential in the source region increases appreciably making a step rise, which diminishes short channel effects and improves current driving capability considerably. The height of the steps will increase with the increase in the halo doping and thickness of oxide and silicon layers. Thus, it is concluded that the gate to source bias voltage has a large impact on the tunneling generation rate at the source and also step shaping of the potential profile reduces the drain control on the channel. Also, from the comparison results, it is seen that halo doping done in Dual Material Surrounding gate TFET gives improved performance. A good degree of analogy is achieved between simulated and calculated results.

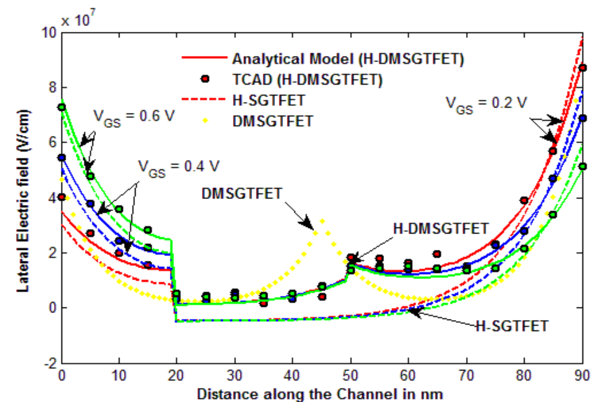

Fig.3.Lateral Electric field along the channel for different gate to source bias voltage and V_{DS} = 0.6 V.

Fig.3. shows the calculated and simulated lateral electric field distribution of H-DMSGTFET for various values of gate voltages. The electric field is essential to both the operation and reliability of the device. The drain to source bias contributes to the lateral electric field distribution. Increase in V_{DS} causes a prominent rise in the lateral electric field and thus decreases the drain control over the channel. The figure also shows a dip in the electric field near the halo boundary in H-DMSGTFET as compared with H-SGTFET and DMSGTFET. This ensures increased carrier acceleration in H-DMSGTFET. Hence, current drive capability is also increased. Also, the electric field peak near the drain end in H-DMSGTFET is lower than DMSGTFET and H-SGTFET, assuring increased suppression of hot carrier effects. The analytical results match well with the simulated results.

Fig.4 shows the vertical electric field distribution of H-DMSGTFET for varying gate to source bias voltages. The gate to source voltage contributes the vertical electric field of the device. High vertical electric field is induced at the source to channel junction as the voltage applied at the gate increases. Hence maximum vertical electric field is present at the tunneling junction. The high electric field leads to minimum tunneling barrier width between the source and the intrinsic channel, resulting in enhanced drain current. Also, the peak electric field is low at the drain end which can be concluded as reduced hot carrier effect in the drain end. Comparison results show better performance of H-DMSGTFET.

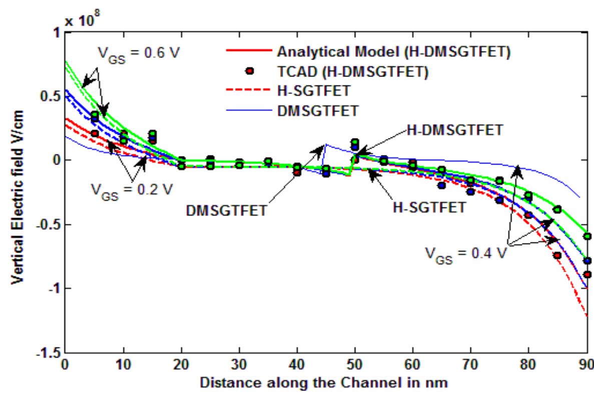

Fig.4.Vertical Electric field along the channel for different gate to source bias voltage and V_{DS} = 0.6V.

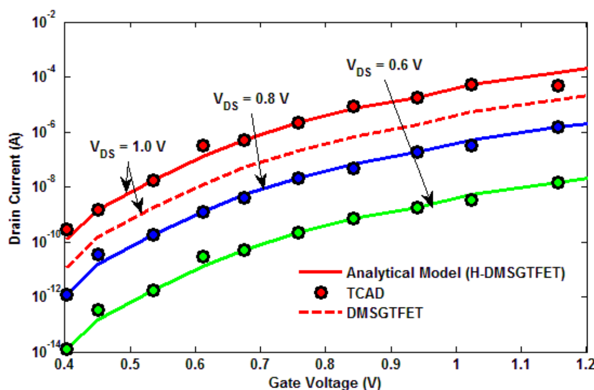

Fig.5. Transfer characteristics of H-DMSGTFET. Comparison results with DMSGTFET are also shown.

Fig.5 shows the transfer characteristics of the proposed device H-DMSGTFET. The figure depicts that leakage current is significantly lowered in the proposed structure and it is an evidence for suppression of SCE. With the positive gate voltage, the energy bands in the intrinsic region are pushed down, and the tunneling occurs between the valence band of the p+ region and the conduction band of the intrinsic region.

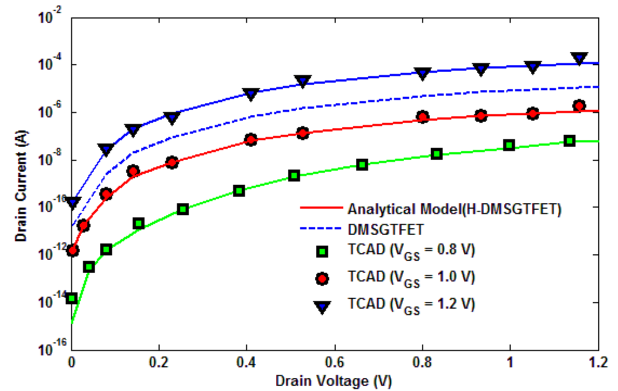

Fig.6. I_D vs V_{DS} characteristics of H-DMSGTFET. Simulation results are shown.

A very high electric field is created, resulting in high I_{ON}. I_D vs V_{DS} characteristics of DMSGTFET for V_{GS} = 0.8V, 1.0V and 1.2V is plotted in Fig.6. Increase in V_{DS} causes barrier lowering. The channel resistance becomes high, resulting in the saturation of drain current. The results predicted by the model are in excellent agreement with the simulation results. The comparison results ensure the better drain characteristics of the proposed structure.

IV. CONCLUSION

In this paper halo doping is done in Dual Material Surrounding Gate TFET to exhibit improved performance. 2-D Poisson's equation has been solved using parabolic approximation technique. Analytical expressions have been derived for surface potential, lateral electric field, vertical electric field and drain current of the new device structure H-DMSGTFET. The calculated results have been compared with the simulation results. The validity of the model is verified by the close proximity of the analytical results and the simulated results. The halo doped device shows considerable reduction in tunneling junction width, and substantial increase in carrier efficiency and hence ON current. This new structure exhibits remarkable characteristics than its counterparts, depicting the diminished SCEs and proves to be a better alternative device for the conventional MOSFETs for future technologies.

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