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Performance Analysis of new Swarm Intelligence based Algorithms in optimizing the design of CMOS Folded Cascode OPAMP and Comparator Circuits

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Abstract
The efficient design of optimum large VLSI Circuits manually has become a tiresome problem mainly because of the complexities associated in the design process and as a result the use of many novel and hybrid algorithms has become a general trend now a days among the researchers. Swarm Intelligence based techniques is a part of the Evolutionary Algorithms family, based on the behavior of swarm of birds and is largely used by researchers now a days, mainly because of their simplicity and efficient evolutionary computational complexities. In this paper, two new techniques based on Swarm Intelligence, namely the Particle Swarm Optimization with Ageing Leader and Challengers (ALCPSO) and the Human Behavior based PSO (HBPSO), have been employed to optimize the design of two important CMOS Analog Circuits, namely, the CMOS Folded Cascode Operational Amplifier (OPAMP) and the CMOS Comparator with PMOS Input driver. The aim is to compare the performance of ALCPSO and HBPSO in their ability to achieve optimum performance of the above two circuits for design specifications such as Slew Rate, Gain, CMRR etc. and also to minimize the overall transistor area required in the design. Based on the experimental results, it can be said that both the Swarm Intelligence based methods were able to match up to theoretical and simulated results, with the ALCPSO being able to achieve better results in terms of minimum transistor area and also better optimum values of design specification such as Gain, Slew Rate etc. and also having a better convergence speed in obtaining the result. The design of both these algorithms were verified by designing the desired circuits using CADENCE Virtuoso Simulator, which showed that Swarm Intelligence based design met with design specification and actual circuit simulation.

Keywords: Evolutionary Algorithms, ALCPSO, HBPSO, Automated Circuit Design, Folded Cascode.

Introduction

As the market demand for System OnChip (SoC) is growing up with more features incorporated in the chip, the complexity of the design is also increasing, especially that of analog part, which do not have efficient and automated CAD systems as compared to its digital counterpart and also involves the computation of various design specifications such as Gain, Slew Rate, Bandwidth etc. which have an inherent trade- off between them. Thus new efficient design methodology for automated design of complex CMOS Analog Circuits, which meet these specifications are required. Absence of automated synthesis or sizing methodology, results in complexity in terms of time and cost of design. As a result, automated methodologies for synthesizing of analog circuits have received much attention from researchers [1] [2] and researchers from time to time have used various heuristic approaches to solve this problem, starting from the use of Mathematical Optimization techniques such as the Geometric Programming [3] to the use of novel and hybrid Genetic [3][4] and Evolutionary Algorithms such as the Particle Swarm Optimization (PSO) [3][5], Ant Colony Optimization[3] etc. PSO is one such algorithms whose basic as well as many hybrid versions have been employed by researchers for optimum and automated design of various Analog Circuits such as the CMOS OPAMP and Differential Amplifer by

Vural et al. [6], Low Power Analog Circuit design [7] etc. Various PSO variants has been developed by researchers till date to overcome drawbacks associated with each previously developed version of it, like Stagnation Effect, poor convergence etc. Human behavior based PSO (HBPSO) proposed by Hao Liu et al. [8] and PSO with Aging Leaders and Challengers (ALC-PSO) proposed by Wei-Neng Chen et al. [9] are two such modified variants of PSO and have been found to be better than the previous versions for mathematical problems, in terms of a better optimum value, stability, convergence speed, time complexity etc. Other popular use of Optimization Algorithms in the design of Analog Circuits includes that of two stage Miller OPAMP using Simulated Annealing [10], GA based noise minimization for OPAMP [11], Differential Evolution and Harmony Search based Comparator design by Vural et al. [12], Folded Cascode. OPAMP design by Nakhei et al. [13] using PSO among others.

The main objective of this work is to make a comparative analysis of the performance of HBPSO and ALC-PSO on the automation of analog circuit sizing problem for two circuits namely the Folded Cascode OPAMP and the CMOS Comparator. Comparison of algorithms are done by measuring performance in terms of design specifications such as Slew Rate, CMRR, Gain, Power Dissipation etc. to achieve optimum value in the desired range and also in achieving a minimum transistor area. This work is inspired from the works of Vural et al. [12] and De et al. [14], who have designed these circuits using some Evolutionary Algorithms like DE, HS, ALCPSO etc. One of the main contribution of this paper is the use of HBPSO algorithm which has not been applied to any analog integrated circuit design problems so far. For the design, we have used the technology parameters from the UMC 180nm technology, which again is not used in any previous works. The circuits are redesigned in the circuit simulator CADENCE Virtuoso using the values of width (W) and lengths (L) of the transistors found by the ALCPSO and HBPSO for validation purpose and the results found were encouraging.

The paper is organized as follow : In Sec. 2, the Swarm based algorithms used, namely, HBPSO and ALC-PSO are introduced and briefly discussed. In Sec. 3 the systematic design procedure of the two selected analog IC's are discussed and the objective function is formulated. In Sec. 4, the application of HBPSO and ALC-PSO in the optimal design of the analog circuit is discussed. In Sec. 5, the simulation results are given, followed by validation of the system performance with CADENCE Virtuoso simulator. In Sec. 5 the conclusions are drawn.

Swarm Intelligence based Algorithms employed in the work :

In this work, we have employed two new algorithms from the Swarm Intelligence family, the most basic form of which is known as the Particle Swarm Optimization (PSO). PSO is based on the social behavior, intelligence and movement of swarm searching for the optimal and best location in a multidimensional search space. It was originally introduced by Kennedy and Eberhart [5] inspired by the social behavior of a flock of birds or colony of fish. In PSO, a group of agents called Particles, which represent a potential solution of an optimization problem, roam in a search space of dimension D to find the global minimum of an objective function and the whole set of particles is called a swarm. Each particle is initialized with a random position value, within the desired range for every dimension and is updated every iteration. The current position of the particle having the best or the minimum fitness constitute our solution. In a d dimensional search space with N particles, the position and velocity of i^{th} particle is given by

$$Xi = [Xi1, Xi2, \ldots\ldots\ldots, Xid] \quad (1)$$

$$Vi = [Vi1, Vi2, \ldots\ldots\ldots Vid] \quad (2)$$

For every iteration, the position and velocity of the i^{th} particle in D dimension search space are updated as follows [5]:

$$v_{id}^{k+1} = \text{w}.\ v_{id}^{k} + \text{c}_1.\ rand_1^k.\ (pbest_{id}^{k} - x_{id}^{k}) + \text{c}_2.\ rand_2^k.\ (gbest_d^{k} - x_{id}^{k}) \quad (3)$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \quad (4)$$

Here the range of i, d, and k indices are defined as { 1..... N }, { 1..... D } and { 1..... max_iteration_number } respectively. The inertia factor w controls the tradeoff between the global and local search capabilities of the swarm. c_1 and c_2 are the acceleration coefficients, $rand_1$ and $rand_2$ are two random numbers uniformly distributed between 0 and 1. k is the iteration number. pbest is an indication of the best fitness obtained by each particle during every iteration whereas gbest is a measure of the best fitness particle among the entire swarm. Although PSO is simple in nature and computationally efficient, but it may suffer from the problem of Stagnation Effect. So, researchers have proposed a number of variants of PSO algorithm. In this paper we consider two such new variants of PSO, the HBPSO and ALC-PSO and compare their performance in solution of analog circuit sizing problem considering Folded Cascode OPAMP and Comparator Circuits.

A. Human Behavior PSO (HBPSO)

A number of variants of original PSO have been proposed by researchers to improve its performance. One such modified version of PSO, based on human behavior, which is called Human behaviour PSO (HBPSO) was originally proposed by Hao Liu et al. [8] in the year 2014. In this model the human behavior is incorporated for improving the performance of the PSO. Here, the algorithm is modelled considering the unique nature of humans who have the ability to understand good and bad activites and learn from them and keep away from bad influence. A new term called the Global Worst (gworst) is introduced and is used in the velocity updating equation in addition to gbest and pbest, so that the swarm learns from it and follows the best fitness particles. This has improved the performance of the basic PSO in terms of better optima, convergence speed, removal of Stagnation Effect etc. Gworst

is worst fitness among the entire swarm and is defined as follows:

$gworst$ =argmax { f ($pbest_1$), f ($pbest_2$),.., f ($pbest_N$)} *(5)*

Where f (.) represents the fitness value of the corresponding particle. Also, to make full use of gworst, a new learning rate r_3 is introduced, which is a random number such that $r_3 \in N(0, 1)$. If $r_3>0$, it is considered as an impelled learning coefficient, which is helpful to enhance the "flying" velocity of the particle; therefore, it can enhance the exploration ability of particle. Conversely, if $r_3<0$, it is considered as a penalized learning coefficient, which can decrease the "flying" velocity of the particle; therefore, it is beneficial to enhance the exploitation. On the other hand $r_3 = 0$, it represents that these bad habits or behaviors have no effect on the particle. To reduce the sensitivity of the equation, c_1 and c_2 are eliminated and two random learning co-efficients $rand_1$ and $rand_2$ are introduced respectively. The velocity update equation is now defined as below:

$$v_{id}^{k+1} = w.\ v_{id}^{k} + rand_1^k.\ (pbest_{id}^k - x_{id}^k) + rand_2^k.$$

$$(gbest_d^k - x_{id}^k) + rand_3^k\ (gworst_d^k - x_{id}^k) \text{.....} \quad (6)$$

The position update equation is same as in (4).
The procedure for the implementation of the HBPSO algorithm is shown in Fig. 1.

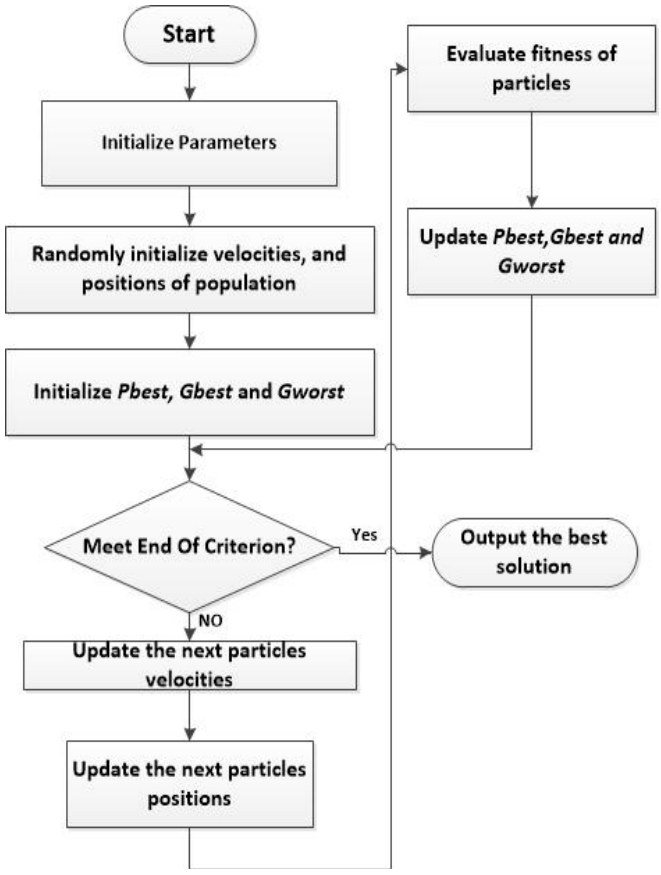

Fig. 1. Flow chart of HBPSO, Liu et al. [8]

B. PSO with Ageing Leader and Challengers (ALC-PSO) :

Another PSO variant known as PSO with Ageing Leader and Challengers (ALC-PSO) was proposed by Wei-Neng Chen et al. [9] in the year 2013, in which an age factor or lifespan is assigned to the leader. The lifespan is tuned as per the leader's leading power. As soon as the lifespan is enervated, the leader is challenged and replaced by a newly generated particles. The crux of ALC-PSO is that it provides a technique to push for a suitable leader which leads the swarm through aging. As all particles are attracted by $gbest$ in the original PSO, $gbest$ is considered as the leader of the swarm [9]. Based on this, the velocity update rule for ALC-PSO is given below:

$$v_{id}^{k+1} = w.\ v_{id}^{k} + c_1.\ rand_1^k.\ (pbest_{id}^k - x_{id}^k)$$

$$+ c_2.\ rand_2^k.\ (Leader_d^k - x_{id}^k) \quad (7)$$

w in the equation (7) is inertia weight whose large value leads to global search and smaller value leads to local search. Value of inertia weight affects convergence. In ALC-PSO, as soon as the leader traps into local optima, new challengers are generated to claim leadership of swarm and lead the swarm towards best solution. This again improves the performance of the swarm in terms of better optima, convergence speed, time complexity, stagnation effect removal etc. The position update of the algorithm is same as given in (4). The flow chart for ALC- PSO is given in Fig. 2. More detailed discussion of the Swarm Intelligence based Algorithms can be found [5][8][9]

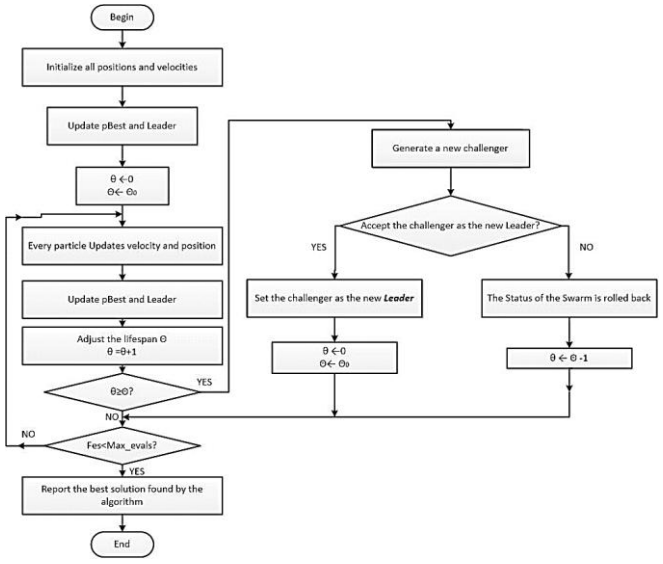

Fig. 2. Flow chart of ALCPSO, Chen et al. [9]

Design procedure for Analog Integrated Circuits used:

In this paper we have considered two analog circuits, one the optimal design of a CMOS Comparator with PMOS input driver as shown in Fig. 3 and other the optimal design of a CMOS Folded Cascode operational amplifier (OPAMP) as shown in Fig. 4, to demonstrate and analyze the performance of both HBPSO and ALCPSO in the design of Analog IC's.

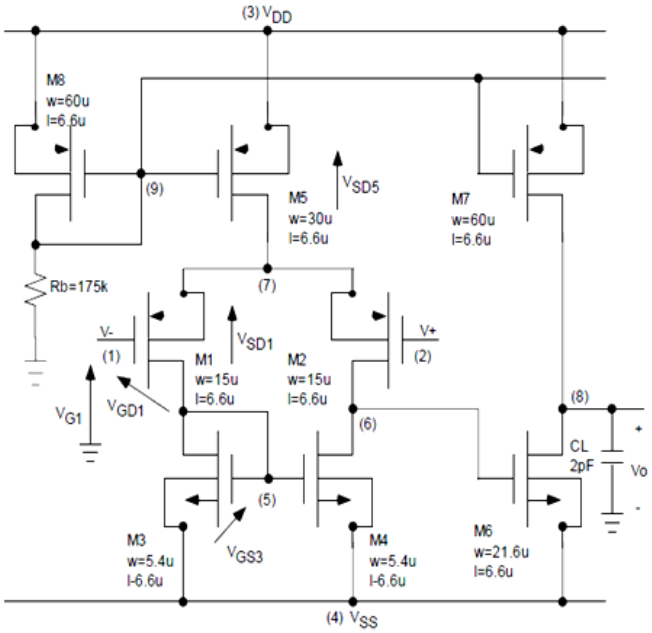

Fig. 3. CMOS Comparator with PMOS Input driver, De et al. [14]

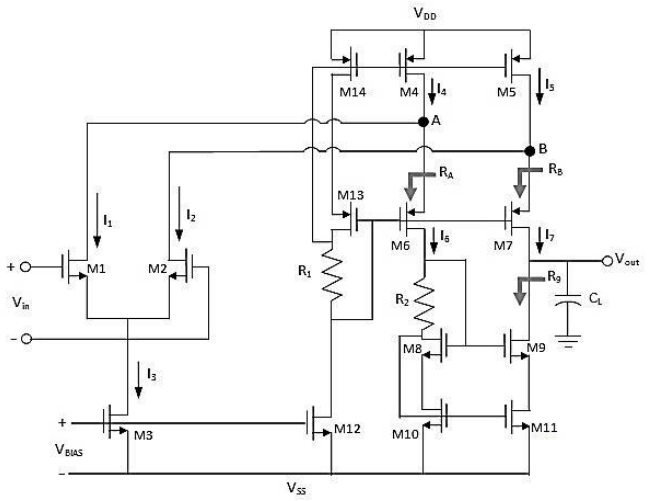

Fig. 4. Practical n channel input Folded Cascode OPAMP, Hollberg [15]

A Comparator is a circuit that gives a binary output by comparison of two analog signals. An important characteristic of the Comparator is that its output does not change until the input difference reached the input offset V_{os}. It is widely used in ADC's, data transmission etc. [12]. The Comparator Circuit can be specified by a number of characterisitcs or design specifications as given below:

- Common mode rejection ration (CMRR).
- Input offset voltage (V_{os}).
- Slew rate (SR).
- Power dissipation (P_{diss}).
- Small signal characteristics (A_v, A_{vd})
- Output Voltage Swing
- Phase margin.
- Input common mode range (ICMR).
- Power supply rejection ratio.
- Unity gain bandwidth.
- Propagation delay

On the otherhand, a Folded Cascode Circuit consists of a differential amplier implemented in a atypical manner and a cascaded output stage. The atypical arrangement of Diffrential Amplifier gives a very good ICMR. It offers higher gain and self-compensation. The design specification for it are same as that for the Comparator Circuit. A more detailed discussion for the circuits can be found in [14].

Some of these design specifications or performance measures as well as the design objectives have to be formulated in terms of the design parameters and as constraints for the problem because many of the design specifications have an inherent trade-off between them. In this paper the design objective which is also defined as Cost Function (CF) is the minimization of the total MOS transistor area given as :

$$CF = \sum_{k=1}^{T} W_k L_k \ldots\ldots\ldots\ldots\ldots \quad (8)$$

Where T is the total no of transistors. T =8 for the Comparator Circuit and T=14 for Folded Cascode Circuit.

The different design specifications or criteria have definite relations among them indicated by design procedure below and forms the particle vector for the optimization problem. The Width (W) and Length (L) of the MOS Transistors are the design variables to be determined such that Area is minimized and also design constraints are met. These equations or relations along with the constraints are utilized by the HBPSO and ALC-PSO algorithms, to find the optimal size of the MOS transistors such that the CF is minimized.

I. Design procedure for CMOS Comparator with PMOS Load:

1. Determine the current drive requirement of M7 to satisfy the SR specification

$$I_{D7} = C_L\left(\frac{dV}{dt}\right) = C_L(SR)$$

2. Determine the size of M6 and M7 to satisfy the output-voltage swing requirement

$$V_{SD7(SAT)} = V_{DD} - V_{o(max)}$$

$$V_{SD7(SAT)} = \sqrt{\frac{2I_{SD7}}{\beta_7}} = \sqrt{\frac{2I_{SD7}}{K_p\,(\frac{W}{L})_7}}$$

$$(\frac{W}{L})_7 = \frac{2I_{DS7}}{K_P\,(V_{DS7(SAT)})^2}$$

Similarly,

$$(\frac{W}{L})_6 = \frac{2I_{DS6}}{K_N\,(V_{DS6(SAT)})^2}$$

3. Calculate the gain of the second stage.

$$A_{V2} = -\left(\frac{g_{m6}}{g_{ds6} + g_{ds7}}\right)$$

$$= -\frac{\sqrt{2K_N I_{DS6}(\frac{W}{L})_6}}{I_{DS6}(\lambda_N + \lambda_P)}$$

4. Calculate the gain of the first stage to satisfy the overall gain

$$A_V = A_{V1}A_{V2}$$

5. Determine the first stage biasing current using the minimum allowable size of 1, and minimum output offset.

(a) Consider M4 and M6.
Using the minimum size for M4, determine the current ISD4 that mirror with M6. That is,

$$I_{DS4} = \frac{(W/L)_4}{(W/L)_6} I_{DS6}$$

$$I_{SD5} = 2I_{DS4}$$

(b) Consider M5 and M7
Using the minimum size for M5, determine the current I_{DS5} that mirror with M7. That is,

$$I_{SD5} = \frac{(W/L)_5}{(W/L)_7} I_{SD7}$$

$$I_{DS4} = I_{SD5}/2$$

$$I_{SD2} = I_{SD1} = I_{SD5}/2$$

(c) Select the larger of the two I_{DS4} and adjust the size of M4 if necessary.

6. Determine the size of M1 to satisfy the gain requirement.

$$A_{V1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}}$$

$$= \frac{\sqrt{2K_p I_{SD1}(W/L)_1}}{I_{SD1}(\lambda_N + \lambda_P)}$$

$$(W/L)_1 = \frac{[A_{V1} I_{SD1}(\lambda_N + \lambda_P)]^2}{2K_p I_{SD1}}$$

7. The minimum size of M5 (=1) in step 5(b) can be adjusted to satisfy the positive ICMR

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - V_{SG1}$$

$$V_{G1(max)} = V_{DD} - V_{SD5(SAT)} - \sqrt{\frac{2I_{SD1}}{K_P\left(\frac{W}{L}\right)_1}} - |V_{T1}|$$

$$V_{SD5(SAT)} = V_{DD} - V_{G1(max)} - \sqrt{\frac{2I_{SD1}}{K_P\left(\frac{W}{L}\right)_1}} - |V_{T1}|$$

$$V_{SD5(SAT)} = \sqrt{\frac{2I_{SD5}}{K_P\left(\frac{W}{L}\right)_5}}$$

$$(W/L)_5 = \frac{2I_{SD5}}{K_P(V_{DS5(SAT)})^2}$$

Select the larger of the two, $(W/L)_5$ and adjust the size of M7 for proper mirroring with M5.

$$(W/L)_7 = \frac{I_7}{I_5}(W/L)_5$$

8. The minimum size of M3 or M4 (=1) in step 5(a) can be adjusted to meet the negative ICMR.

$$V_{G1(min)} = V_{SS} + \sqrt{\frac{2I_{SD1}}{K_P\left(\frac{W}{L}\right)_1}} + V_{T3} - |V_{T1}|$$

Select the larger of the two $(W/L)_3$

$$(W/L)_3 = \frac{2I_{DS3}}{K_p\left(V_{G1(min)} - V_{SS} - V_{T3} + |V_{T1}|\right)^2}$$

9. Determine the size of M8 to provide as the main current mirror for the comparator.

$$(W/L)_8 = \frac{2I_{SD8}}{K_P(V_{SG8} - V_{TP})^2}$$

10. The external resistor Rb connected between VG8 and ground must be chosen to provide the required current for M8.

$$R_b = \frac{V_{g8} - 0}{I_{DS8}}$$

II. Design procedure for Folded Cascode OPAMP:

1. Slew Rate:

$$I_3 = (SR)C_L$$

2. Bias currents in output cascodes

$$I_4 = I_5 = 1.2I_3$$

3. Maximum output voltage $(V_{out(max)})$

$$(\frac{W}{L})_5 = \frac{2I_5}{K_P {V_{SD5}}^2} \text{ And } (\frac{W}{L})_7 = \frac{2I_7}{K_P {V_{SD7}}^2}$$

Let $(\frac{W}{L})_4 = (\frac{W}{L})_{14} = (\frac{W}{L})_5$ and

$$(\frac{W}{L})_{13} = (\frac{W}{L})_6 = (\frac{W}{L})_7$$

4. Minimum output voltage $(V_{out(min)})$

$$(\frac{W}{L})_{11} = \frac{2I_{11}}{K_P {V_{SD11}}^2} \text{ And } (\frac{W}{L})_9 = \frac{2I_9}{K_P {V_{SD9}}^2}$$

Let $(\frac{W}{L})_{10} = (\frac{W}{L})_{11}$ and

$$(\frac{W}{L})_8 = (\frac{W}{L})_9$$

5. Self-bias cascade

$$R_1 = \frac{V_{SD14(SAT)}}{I_{14}} \; and \; R_2 = \frac{V_{DS8(SAT)}}{I_6}$$

6. UGB = $\frac{g_{m1}}{C_L}$

$$(\frac{W}{L})_1 = (\frac{W}{L})_2 = \frac{{g^2}_{m1}}{K_n I_3} = \frac{UGB^2 {C_L}^2}{K_n I_3}$$

7. Minimum input CM $(V_{IC(min)})$

$$(\frac{W}{L})_3 = \frac{2I_3}{K_n \left[V_{in(min)} - V_{SS} - \sqrt{\frac{I_3}{K_n (\frac{W}{L})_1}} - V_{T1} \right]^2}$$

8. Maximum input CM $(V_{IC(max)})$

$$(\frac{W}{L})_4 = (\frac{W}{L})_5 = \frac{2I_4}{K_p \left[V_{DD} - V_{in(max)} + V_{T1} \right]^2}$$

9. Differential voltage gain

$$A_{vd} = \left(\frac{2+k}{2+2k} \right) g_{m1} R_{II}$$

$$where \; k = \frac{R_9 (g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}}$$

$$R_9 \approx g_{m9} r_{ds9} r_{ds11}$$

$$R_{II} = R_9 \parallel [g_{m7} r_{ds7} (r_{ds2} \parallel r_{ds5})]$$

10. Power dissipation

$$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{12} + I_{10} + I_{11})$$

HBPSO and ALC-PSO based circuit design for CMOS Comparator and Folded Cascode OPAMP:

In order to make a comparative analysis of the performance of HBPSO and ALC-PSO algorithms in the optimal design of analog circuit, two basic analog circuit structure have been considered as mentioned earlier. The task of the both the algorithms is to find the optimal dimensions of the MOS transistors, such that the CF defined in (8) is minimized, while satisfying the design specifications and design parameter constraints.

For designing purpose, the technology parameter is set by designer from the library and a criterion for the design is formulated. The range of design parameters, design specifications, power supply values and technology information are set as inputs to both the optimization technique. The task of the algorithms is to find the optimal value of the design parameters (W_i/L_i), where (i = 1..... 8) for CMOS Comparator with PMOS Load and (i = 1..... 14) for CMOS Folded Cascode OPAMP and the design specifications ($V_{IC(max)}$, $V_{IC(min)}$, SR, P_{diss}, A_V, UGB, C_L) within the given ranges.

Circuit simulations are carried out with CADENCE Virtuoso with model parameters of United Microelectronics Corporation (UMC) 0. 180 µm technology for validation purpose. The values of the technology parameters used in design are shown in Table 1.

TABLE 1: Technology, inputs and lengths considered of UMC180.

Inputs, Technology, Lengths	Values used
Vdd (V)	1. 8
Vss(V)	-1. 8
Vtp(V)	-. 42
Vtn(V)	. 42
Kn(µA/V^2)	355
Kp(µA/V^2)	75
Length (FoldedCascode) (µm)	1. 25(for i=1, 2,.. 14);
Length(Comparator)(µm)	2(for i=1, 2,.. 8)

Both HBPSO and ALC-PSO Algorithms are programmed using MATLAB 2013b that runs on a CPU Intel core i5 and having 4 GB RAM. Initial population matrix size was 10 x4 where row number of 10 indicates the number of particles in the population and column number of 4 is the dimension of particle vector for Comparator Circuit and it is 10 x7 for Folded Cascode Circuit. Particle vector structure for each analog circuit structure is expressed in (9) and (10).

$X_{Comparator}$ = [SR, A_{vd}, $V_{IC\ min}$, $V_{IC\ max}$] (9)

$X_{FoldedCascode}$= [SR, C_L, A_{vd}, UGB, $V_{IC\ min}$,

$V_{IC\ max}$, P_{diss}] (10)

Where SR is the slew rate (V/µs), C_L is the output Load capacitance (pF), A_{vd} is the gain (V/V), UGB is Unity gain bandwidth (MHz), $P_{diss}$is the power dissipation (µW),

$V_{IC(min)}$ (V) and $V_{IC\ (max)}$ (V) are the lower and upper limits of ICMR, respectively.

The social and cognitive factors c_1, c_2 of ALC-PSO were kept as. 12 and 1. 2 respectively

The inertia factor w varies from. 9 to. 4 and is updated in every iteration according to the rule in (11)

$$w = wmin + ((wmax - wmin) * (iter_{max} - curr\_iter)/curr\_iter) \ldots\ldots\ldots\ldots \quad (11)$$

The Cost Function has been mentioned in (8). The Table 2, shows the inputs to the Algorithms.

TABLE 2: Algorithm parameters.

Parameters	Values used
Population Size	10
Dimension	7
c1, c2 (for ALC- PSO only)	. 12 and 1. 2 respectively
No. of Iterations	100
Population Matrix	10*4 (Comparator) and 10*7 (Folded Cascode)

Simulation Results

In this section, the results for simulation of HBPSO and ALC-PSO based Analog Circuit Design Methodology is discussed.

A. Simulation Results for CMOS Comparator with PMOS Load

For, HBPSO and ALC-PSO have been employed with current mirror load with the values of design specifications kept in certain ranges. The design specifications and their ranges are as below:

SR≥10V/µs, Av>500V/V, UGB≥7MHz, -1. 5V≤ICMR≤1. 8V, Pdiss≤1000µW. The input technology parameters have been shown in Table 1. Also, aspect ratio (W/L) are kept as $100 \geq (W/L)_k \geq 1$. To minimize Channel Length Modulation, we have 2 µm for Comparator Circuit

The target Cost Function has been kept to be below 500µm^2. The total MOS Area obtained with ALCPSO is 334. 25 µm^2 while that with HBPSO is 384. 19 µm^2 with each MOSFETS width and values of design specifications within the ranges specified. Thus, ALC-PSO showed a better results in terms of minimum area in obtaining the optimum solution. Also, ALC-PSO obtained better values for design specifications of Slew Rate and Gain but with a little higher Power Dissipation as compared to values obtained with HBPSO.

CMOS Comparator with PMOS Load have been simulated using CADENCE Virtuoso to validate wheather HBPSO and ALC-PSO based designs are satisfying desired specifications or not. CADENCE Simulation validates the results obtained by both the Algorithms. The circuit parameter values calculated by both the algorithms, after meeting both design specifications and the area constraints are given in Table 3. The results of comparison of ALC-PSO and HBPSO by design specifications are shown in Table 4.

Table 3: Design parameters obtained with ALC-PSO & HBPSO for the Comparator

Design Paramters	ALCPSO	HBPSO
Rb	14. 8k	14. 8k
W1/L1	7. 82/2	7. 82/2
W2/L2	7. 82/2	7. 82/2
W3/L3	6. 95/2	6. 95/2
W4/L4	6. 95/2	6. 95/2
W5/L5	39. 76/2	47. 15/2
W6/L6	4. 69/2	4. 69/2
W7/L7	46. 67/2	55. 34/2
W8/L8	46. 67/2	55. 34/2

TABLE 4: Comparison of ALC-PSO and HBPSO by design specifications.

Design Criteria	Specific-ations	ALC-PSO	HBPSO
Slew Rate (V/µs)	≥10	150. 25	150
Power Dissipation(µW)	≤1000	507. 45	505. 12
Unity Gain Bandwidth (MHz)	≥7	23. 8	24
Differential Voltage Gain (dB)	>55	60	58
Vic(min) (V)	≥-1. 5	-1. 10	-1. 12
Vic(max) (V)	≤1. 8	1. 447	1. 15
Total Area(µm^2)	≤500	334. 25	384. 19

The convergence plot of both the algorithms are shown in Fig. 5. CADENCE Simulation plots (Figs. 6-9) demonstrate that design based on both the algorithms satisfies allspecifications and design criteria. The Convergence Plot as well as the Cadence Simulation, shows that the ALC-PSO is superior over HBPSO with respect to lesser Area, higher Gain, higher CMRR, higherPSRR, high Slew rate but only with a trade-off being little higher Power dissipation and little less UGB.

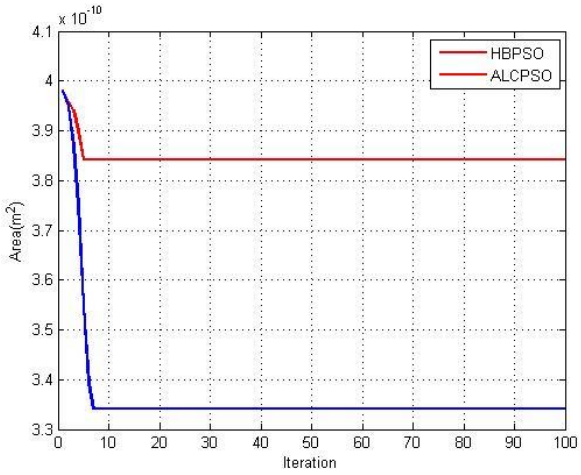

Fig. 5. ALC-PSO & HBPSO convergence plot for Comparator

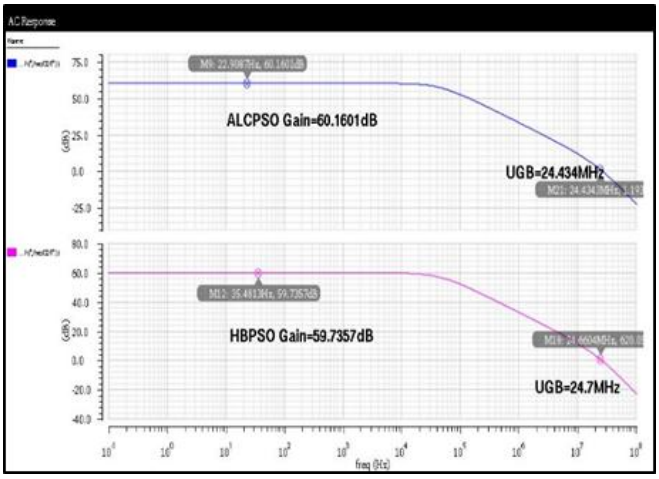

Fig. 6. ALC-PSO & HBPSO gain plot for Comparator

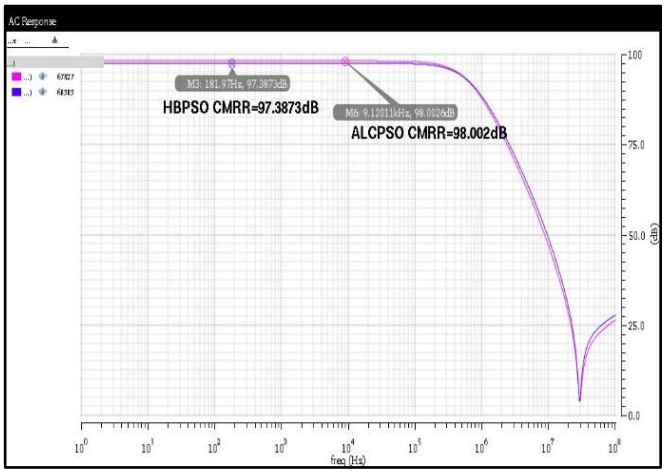

Fig. 7. ALC-PSO & HBPSO CMRR plot for Comparator

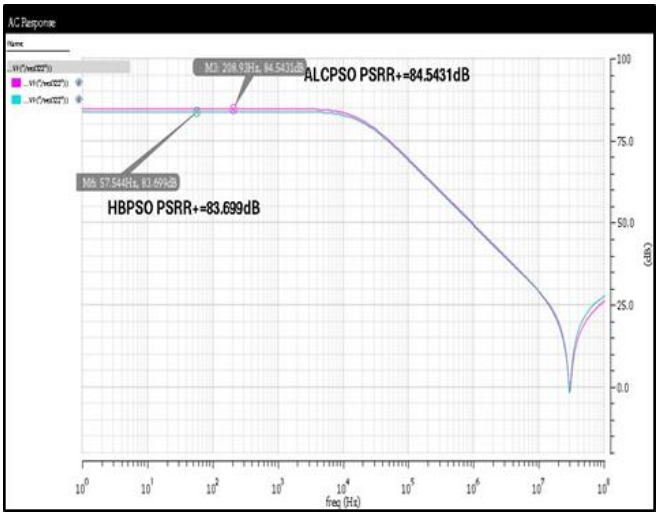

Fig. 8. ALC-PSO & HBPSO PSRR+ plot for Comparator

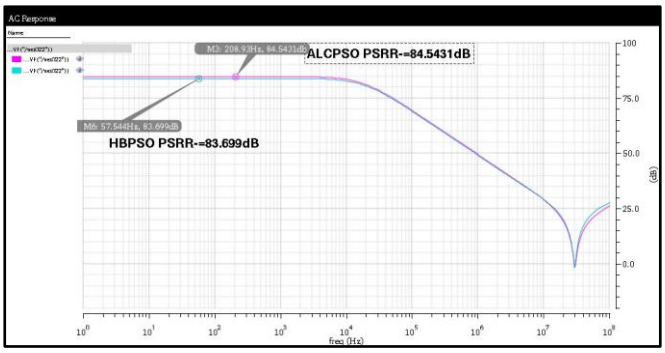

Fig. 9. ALC-PSO & HBPSO PSRR- plot for Comparator

B. Simulation Results for Folded Cascode OPAMP

For Folded Cascode OPAMP design, both the Algorithms have been utilized for obtaining optimum value of circuit parameters satisfying the design specifications given below.

SR ≥10 V/µs, Av>500V/V, UGB≥7 MHz, -1. 5V≤ICMR≤2V, Pdiss≤ 4. 5 mW.

Also the constraints for the design are : Load Capacitance (C_L) is kept as $C_L \geq 10pF$ and aspect ratio is kept as $100 \geq (W/L)_k \geq 1$ for all k To minimize Channel Length Modulation, we have chosen Li=1. 25 µm (for i=1 to 14).
Once Again, the target Cost Function has been kept to be below 300 μm^2. The Area obtained by ALCPSO is 265. 96 μm^2 while that with HBPSO is 263. 8 $\mu m^{2,}$ but ALCPSO having a better convergence speed and better values of Gain and UGB, while HBPSO based design has a lower power dissipation
The Folded Cascode OPAMP have been simulated in CADENCE Virtuoso simulator, to validate whether HBPSO and ALC-PSO based designs are satisfying desired specifications or not. CADENCE simulation validates the results obtained by both the Algorithms. The circuit parameter values calculated by both the algorithms, after meeting both design specifications and the area constraints are given in Table 5. The results of comparison of ALC-PSO and HBPSO by design specifications are shown in Table 6.

TABLE 5: Design parameters obtained with ALC-PSO & HBPSO for the Folded Cascode Amplifier

Design Parameters	ALCPSO	HBPSO
I3(µA)	100	100
I4, I5, I6, I8, I9, I10, I11, I14 (µA)	125	125
I7 (µA)	25	25
R1, R2	2. 4k, 2. 4k	2. 4k, 2. 4k
W1/L1	1. 25/1. 25	1. 25/1. 25
W2/L2	1. 25/1. 25	1. 25/1. 25
W3/L3	1. 9911/1. 25	1. 25/1. 25
W4/L4	46. 293/1. 25	46. 293/1. 25
W5/L5	46. 293/1. 25	46. 293/1. 25
W6/L6	9. 259/1. 25	9. 259/1. 25

W7/L7	9. 259/1. 25	9. 259/1. 25
W8/L8	9. 7809/1. 25	9. 7809/1. 25
W9/L9	9. 7809/1. 25	9. 7809/1. 25
W10/L10	9. 7809/1. 25	9. 7809/1. 25
W11/L11	9. 7809/1. 25	9. 7809/1. 25
W12/L12	2. 489/1. 25	1. 5625/1. 25
W13/L13	9. 259/1. 25	9. 259/1. 25
W14/L14	46. 293/1. 25	46. 293/1. 25

TABLE 6: Comparison of ALC-PSO and HBPSO by design Specifications.

Design Criteria	Specifications	ALCPSO	HBPSO
Slew Rate (V/μs)	≥10	10. 02	10. 02
Unity Gain Bandwidth (MHz)	≥7	8. 87	7. 1
Differential Voltage Gain (dB)	>55	62. 24	56. 34
Vic(min) (V)	≥-1. 5	-1. 5	-. 01
Vic(max) (V)	≤1. 8	1. 447	1. 1
Power Dissipation(mW)	≤4. 5	3. 21	1. 79
Total Area(μm^2)	≤300	265. 96	263. 8

The convergence plot of both the algorithms are shown in Fig. 10. CADENCE Simulation plots (Figs. 11-13) demonstrate that design based on both the algorithms satisfies all specifications and design criteria. These plots also show that although ALCPSO based design has more slightly more Area than HBPSO based design, but it is better with respect to Better Gain, CMRR, but to achieve all these, it has a trade off by having higher power dissipation than the HBPSO.

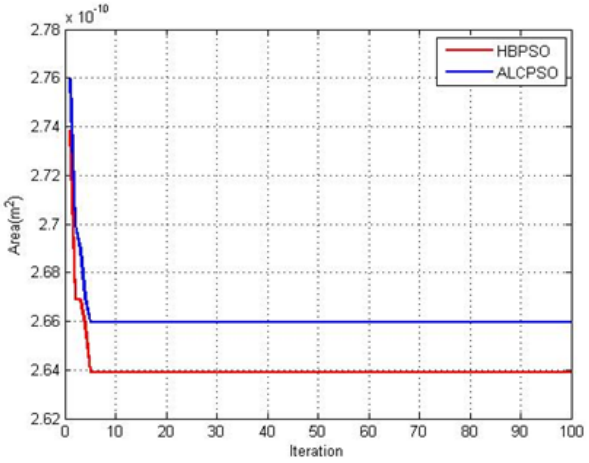

Fig. 10 ALC-PSO & HBPSO convergence plot for Folded Cascode OPAMP

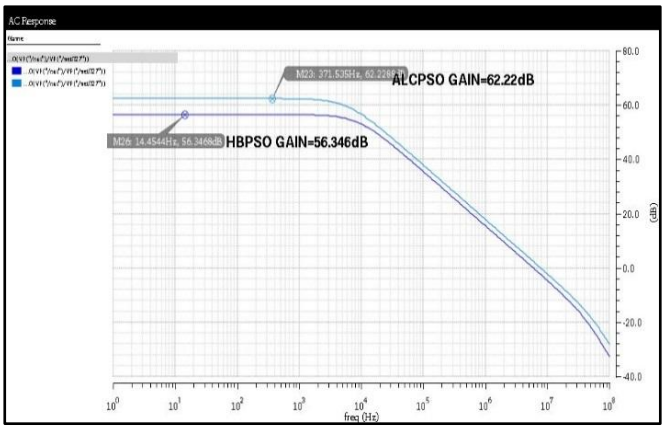

Fig. 11 Gain Plot for Simulation in Cadence Virtuoso for Folded Cascode OPAMP

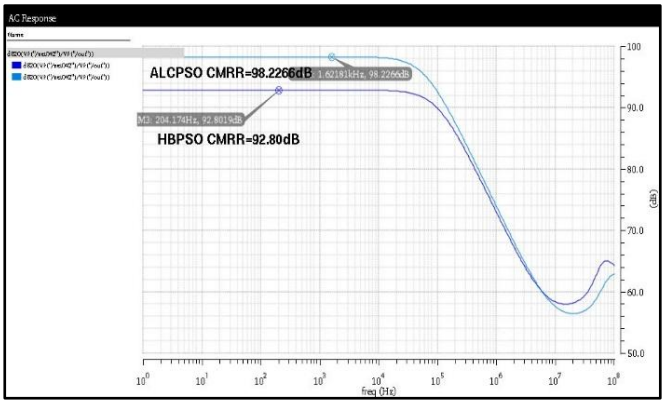

Fig. 12 CMRR Plot for Simulation in Cadence Virtuoso for Folded Cascode OPAMP

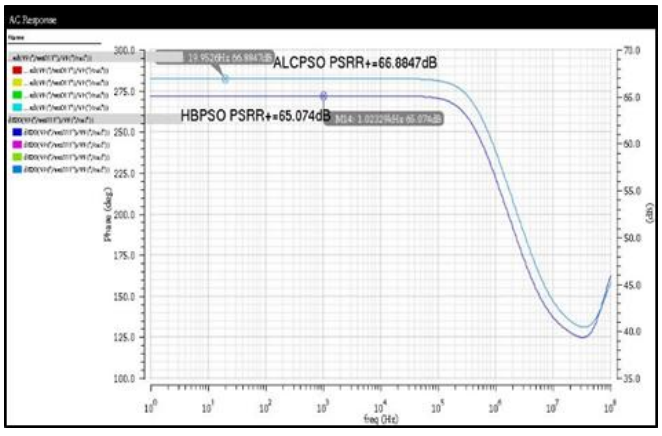

Fig. 13 PSRR$^+$ Plot for Simulation in Cadence Virtuoso for Folded Cascode OPAMP

Conclusion

In this paper, we have employed two algorithms based on swarm intelligence techniques, namely the PSO with Aging Leader and Challengers (ALC-PSO) and the Human Behavior based Particle Swarm Optimization (HBPSO) for optimum design of two Analog Circuits, namely the CMOS Folded Cascode OPAMP and CMOS Comparator. For obtaining the

main design criteria of minimum MOS Transistors Area, these algorithms aim at optimizing the design specifications, variables such as slew rate, gain, power dissipation, etc. From the study of the results obtained from the algorithms, it was found that for the CMOS Comparator Circuit, the ALCPSO based design showed superior results as compared to HBPSO based design in terms of better Gain, CMRR etc, while for the Folded Cascode OPAMP Circuit, although the Area obtained during HBPSO based design is little less but the values of design specifications is higher as compared to the ALCPSO. So, considering the overall aim of the design, the ALCPSO based design can be considered to more suitable. All these results have been verified by simulation of the design using Cadence Virtuoso and have shown satisfactory results.

From the results and study, it can be concluded that both ALC-PSO and HBPSO are efficient technique in finding global optimum solution in Analog Circuit Design than other previously used techniques A direct comparison with previous works is not possible as there is a use of different library technology files which have not been used in any previous works. For Future Works, this algorithm can be used in design of other Analog Circuits such as the CMOS Low Noise Amplifier or the Winner take All Circuits. and also it can be employed for multi-objective problems instead of single objective used in this work.

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