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Design and Implementation of an 8-Bit Double Tail Comparator using Foot Transistor Logic

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Abstract

Now a day, wireless communication designs and applications require high speed, low power and area efficient Analog-to-Digital Converters. Due to this Conventional Comparators has been designed. In order to maximize the speed and power efficiency even better than the existing conventional comparators, the Dynamic Regenerative Comparators came into existence. An analysis on the power consumption and delay time of conventional comparators has been obtained. From this, the main constraints which are responsible for conventional comparator delay time, high power consumption and also how to increase the speed of Dynamic Comparators can be assumed. Based on this analysis, a new Double-Tail Dynamic Comparator using Foot-Transistor Logic has been proposed. Using Foot-Transistor and TSPC Logic a new 8-Bit Double-Tail Comparator has been designed which results in significant reduction of power utilization. By using few transistors a strengthened positive regenerative feedback circuit has been designed, which is also known as Foot-Transistor Logic. The existing conventional comparator has been added with this foot-transistor logic to reduce the power utilization and delay time. This proposed 8-Bit Double-Tail Dynamic Comparator using foot-transistor and TSPC logic has been implemented in 180nm CMOS Technology. Comparison results and design analysis post schematic simulation verify that the power consumption is significantly reduced. Hence, this design results in consuming less power compared to existing comparator.

Keywords: Single Tail Comparator; Double-Tail Comparator; Footed Domino Logic; TSPC Logic; Foot Transistor Logic; Analog to Digital Converters (ADC's.)

INTRODUCTION

Comparators have a critical impact on the overall performance in high speed Analog-to-Digital convertors [1]. The comparators are also known as 1-bit Analog-to-Digital converter due to this feature they are large abundantly used in Analog-to-Digital Converters. They are the basic building blocks in the analog and mixed-mode circuits. It is especially designed for open loop configuration without any feedback [1], [2].

In decision making the response time of the comparator is limited along with the speed. CMOS dynamic latched comparators are very alluring for many applications such as high speed Analog-to-Digital converters, (ADC's), Memory Sense Amplifiers (MSA's), Data Receivers, Zero Crossing Detectors and Peak Detectors due to their special features such as low offset, fast speed, low power consumption, high impedance [2], [8], [15].

The basic operation of a CMOS comparator is to compare an input signal with a reference signal and produce a binary signal as output [6]. It works on two phases: Reset and Regenerative Phase. When the comparator operates in reset phase, the switch is closed and the current in the transistors of the differential pair depends on the input voltage. During the regenerative phase, the switch opens and the two cross coupled inverters implement a positive feedback this makes the output voltage go towards 0 and Vdd [16]. The comparator can be thought of as a decision making circuit. If the positive, V+ input of the comparator is at a greater potential than the negative, V- input then the output of the comparator is a logic 1 signal, whereas if the positive input V+ is at a potential less than the negative V- input then the output of the comparator is a logic 0 signal [10].

To convert the voltage into digital output in a short period of time the comparator uses back-to-back cross coupled inverters [3]. By this mechanism we can convert a smaller voltage difference in full scale digital level output [4]. Some circuits use back-to-back latch stage to generate positive feedback. These circuits are widely used in SRAM, Sense Amplifiers [6]. In the Analog-to-Digital conversion process, it is necessary to first sample the input signal. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal [4].

The performance of the comparator plays an important role in realization of high integration, low power, low cost and good design [3]. Hence, designing high speed comparators is more challenging when the supply voltage becomes smaller. In a given technology, to achieve high speed large amount of

transistors are required to compensate the reduction of supply voltage, which means more die area and power is needed [5].

Common- mode input range is an essential parameter in ADC's; due to the low voltage operations of comparator circuit results in limited common mode input range in ADC's. Clocked regenerative comparators are widely used in high speed ADC's due to its strong positive feedback in the regenerative latch.

To reduce the power consumption and occupying area scaling is used in CMOS transistor. The demand for portable battery operated devices is increasing; a major trust is given towards low power methodologies for high speed applications. By moving towards smaller feature size processes the reduction in power can be achieved. However, as we move towards smaller feature size processes, the overall performance of the device will be greatly affected due to the process variation and other non-idealities. One such application where low power dissipation, low noise, high speed, low offset voltage are required is ADC for mobile and portable devices. The accuracy of the comparator, which is defined by the offset along with the power consumption, delay is taken keen interest in achieving overall high performance of ADC'S [7]. Due to transistor mismatch offset voltage of the comparator exceeds tens mV. In order to convert a small input voltage difference to a full-scale digital level in a short time the comparator circuits use positive feedback mechanism with one pair of back-to-back cross coupled inverters [13].

To overcome this offset voltage problem the dynamic comparators are often used. They make the comparison once in every clock period which requires much less offset voltage. However, these dynamic comparators suffer from large power dissipation [7]. The offset in the comparator is due to mismatch in the load capacitances which leads to more power consumption. Many techniques such as boosting methods, employing body-driven transistors can handle a higher supply voltage which has been developed to meet the low voltage design challenges. These are effective technologies but have reliability issues [9]. However, an input referred latch offset voltage resulting from static mismatches such as threshold voltage Vth & β variations in the regenerative latch, deteriorates the accuracy of such comparators.

During evaluation phase the additional offset term is caused due to dynamic mismatch from the unbalanced parasitic capacitances on the output modes of the latch. Because of this reason, the input referred latch offset voltage is one of the most important design parameters of the latched stage, a low offset can be achieved at the cost of the reduced speed due to slowing the regenerative time & the increased power dissipation [11], [17].

To enhance the comparator speed in low supply voltages additional circuitry is added to the conventional dynamic comparator. This is named as Double-Tail dynamic comparator which is based on separate input and cross coupled stage. But this technique also involves some mismatches in transistor pairs. This can be overcome by strengthening the positive regenerative feedback [9]. In this paper we are going to implement some pair of transistors which is connected in parallel for offset voltage reduction in DTC due to mismatch in transistor pairs. A new technique which uses the latch as load in the first stage is used to reduce the offset voltage in the second stage. Fast speed and low power consumption are the two most important parameters of the comparator which is to be used in high speed ADC's. Hence, the DTC circuit is added with additional circuitry to strengthen the positive regenerative feedback so that the power consumption of the total circuit is reduced. The technology scaling of MOS transistors enables high speed & low power operation but the offset voltage of the comparator is decreased due to this work.

BACKGROUND WORK

A clocked comparator is a circuit element that makes decision as to whether the input signal is high or low at every clock cycle. Due to strong positive feedback in the regenerative latch the clocked regenerative comparators are able to make fast decisions. Here we analyze the power and delay of conventional footed domino logic comparator and proposed double-tail comparator using foot transistor logic for single bit and using this single bit circuit's 8-bit existing conventional footed domino logic comparator and 8-bit proposed double-tail comparator using foot transistor logic has been designed and the power and delay calculations are made. The obtained are compared respectively.

A. Conventional Single Tail Comparator

The schematic diagram of the Conventional Single-Tail Comparator is shown in Figure 1. With high input impedance, rail to rail output swing, and no static power consumption features they are widely used in Analog to Digital converters.

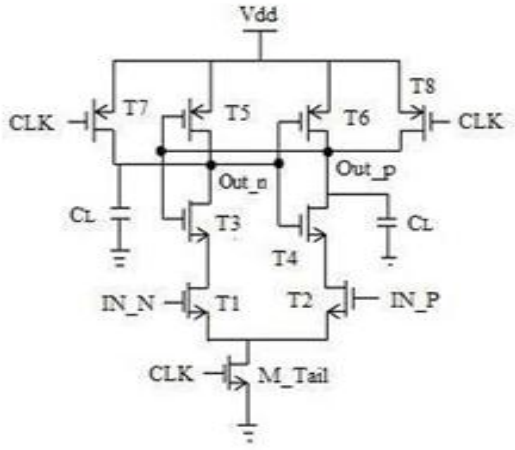

Figure 1: Schematic diagram of Conventional Single Tail Comparator

The circuit operates in two different modes: Reset Phase and Comparison phase. The operation can be explained from the Figure 2. When the input signal VIN_P is greater than VIN_N i.e. VIN_P> VIN_N, then the output Out_p discharges faster *h* than Out_n. When Out_p (discharged by transistor T2 drain current), falls down to Vdd – before Out_n (discharged by transistor T1 drain current), the corresponding PMOS transistor (T5) will turn on triggerring the latch regeneration caused by back to back inverters (T3, T5 and T4, T6). Thus Out_n pulls down to Vdd and Out_p discharges to ground. If VIN_P is less than VIN_N i.e. VIN_P< VIN_N, then the circuit works vice versa. The delay of this comparator is comprises of two time delays, t0 and tlatch.

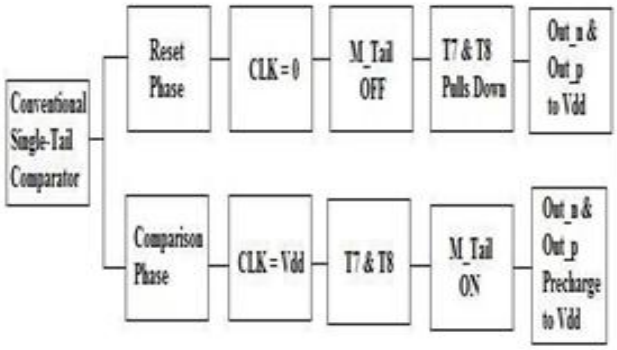

Figure 2: Block diagram representation of Conventional Single Tail Comparator

The delay t0 is represented as the capacitive discharge of the load capacitance (CL) until the transistors (T5/T6) turns ON which are considered as the first 'p' channel transistors. The second term, tlatch, is said to be the latching delay of two cross coupled inverters.

tdelay = t0+tlatch

This circuit cannot operate in low supply voltages to overcome this Conventional Double-Tail Comparator came into existence.

B. Conventional Double Tail Comparator

The schematic of conventional double tail comparator is shown in Figure 3. Compared to Conventional single tail comparators it can operate at lower supply voltages also. This circuit includes an NMOS transistor named as M_Tail2. This double tail enables both large current in the latching stage (wider M_Tail2), for fast latching independent of the Vcm (input common mode voltage), and a small current in the input stage (small M_Tail1), for low offset. Depending on this tail current the input and ground of the circuit is based. When the voltage drop occurs at the nodes f_p and f_n, then the intermediate stage transistor switches.

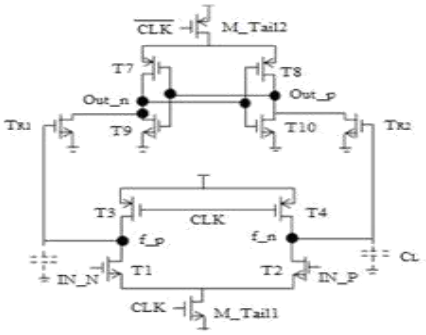

Figure 3: Schematic diagram of Conventional Double Tail Comparator

The operation is explained from Figure 4. The transistors TR1 and TR2 forms an intermediate stage which passes Δf_n/f_p to the cross coupled inverters, due to this between inputs and output a strong shielding is obtained. But the VLSI designers were not satisfied with the leakage current problem so to reduce this they came up with Footed Domino Logic Comparator.

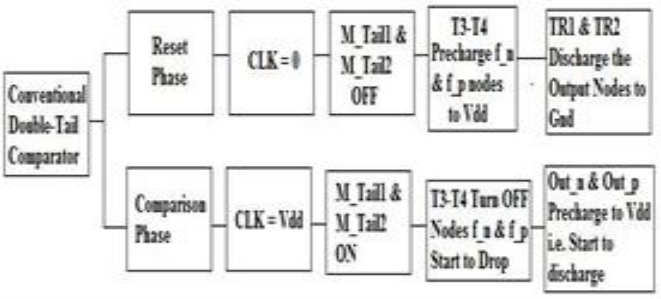

Figure 4: Block diagram representation of Conventional Double Tail Comparator

EXISTING METHOD

A. Footed Domino Logic Conventional Comparator

The schematic of Footed Domino Logic Comparator is shown in Figure 5. An NMOS transistor has been added as N_Foot to the existing circuitry. This N-foot transistor reduces the total power consumption and also improves the noise immunity. The FDLC circuit is used in modern data path, compared to full matches the mismatch occurs with a much higher frequency. So, it will be inefficient that the circuit dissipate energy only on a full match and almost no energy on mismatch.

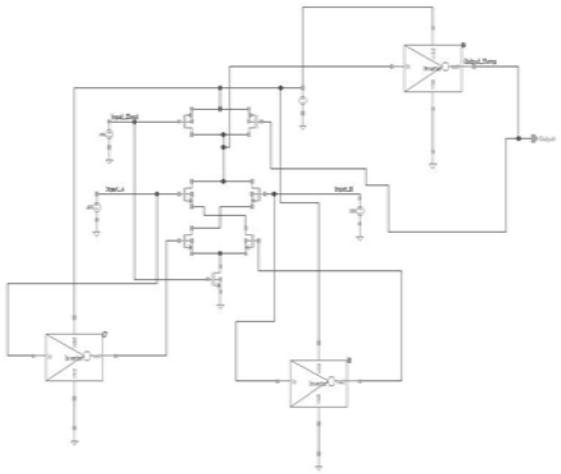

Figure 5: Existing Footed Domino Logic Conventional Comparator

The footed domino logic comparator circuit's exhibit low leakage current, but on the other hand FDLC circuit has more power consumption and lower speed than footless domino logic comparator circuits. This comparator circuit is simulated in 180nm CMOS Technology. The power supply applied in this circuit is 1.8V, due to which the circuit dissipates low leakage current but power consumed is more and has low speed, which is overcome in the proposed comparator.

PROPOSED METHOD

Our proposed Comparator circuit is implemented in 180nm CMOS technology, with a supply voltage of 1.8V due to which the circuit exhibits low leakage and less average power dissipation, than other works. The power consumed by the entire circuit is very less compared to other comparator circuits. The schematic of high speed and a leakage tolerant CMOS comparator based on Footed Domino Logic comparator using foot transistor logic is shown in Figure 6.

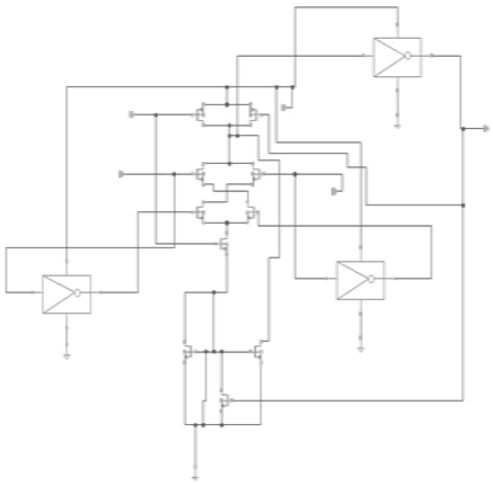

Figure 6: Proposed Double-Tail Comparator using Foot Transistor Logic

This proposed comparator indicates the full match or mismatch of the two binary inputs A and B of 4, 8, 16, 32 or 64 bits applied to the circuit. Basically, this circuit operates on two modes, one is precharge mode and another is evaluation mode. In precharge phase, the clock is low, which makes transistor T1 ON and T2 OFF, then the precharge node is precharged to high and the output goes low and T2 turns ON.

This PMOS transistor T2 keep providing the supply to the pull down network, hence it is known as Keeper Transistor, and Transistor T1 is known as Precharge transistor. During the evaluation mode, when the clock is high, if the corresponding bits of A and B inputs are same than there is no conduction path from precharge node to ground, hence the output remains low. But, if any position of input A and B are different then there exists a conduction path from precharge node to ground, which causes the discharging of that node and hence the output goes high.

So, when the output become high, then the keeper transistor T2 turns OFF, this makes the output high. To provide sacking effect for leakage reduction in evaluation phase transistor T7 is added, but due to this there is an increase in delay, so for reducing the delay in evaluation phase, a current mirror (T8) is added in parallel with evaluation network. The T9 transistor is used to provide feedback from the output to dynamic node, to avoid short circuit current on static inverter. This additional circuit in proposed comparator work in such a way that, in precharge phase, the precharge node is high, then the footer transistor T6 is OFF, therefore the current mirror (T8) is also OFF, and then there is no path for the discharging of precharge node.

In case of evaluation phase, if all inputs are same then stacking effect offered by transistor T7 reduces the leakage of evaluation network. However, when the one of input bit is differ, T8 mirror transistor pulls large current from precharge node, since the output goes to high T9 transistor gets ON to discharge the precharge node completely. So T7 and T8 transistor makes the circuit faster in evaluation phase. Figure 7 and Figure 8 shows the schematic of 8-Bit Conventional footed domino logic comparator and 8-bit proposed double-tail comparator using foot transistor logic. By using the single bit FDLC circuit the 8-Bit FDLC circuit has been designed similarly using single bit Proposed circuit 8-bit proposed circuit has been designed and the respective power and delay calculations are made in 180nm technology and they are compared and tabulated.

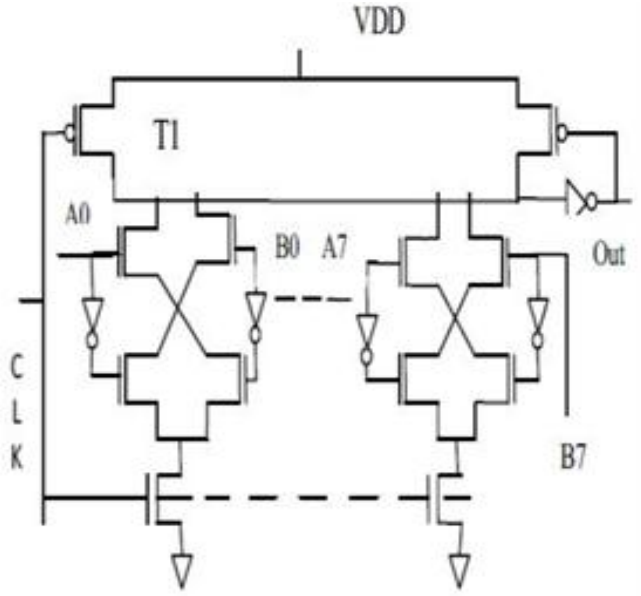

Figure 7: Existing 8-bit Footed Domino Logic Conventional Comparator

During all the transitions the power consumption parameter is the average of power consumption. Hence, the Power Delay Product (PDP) is the multiplication of average power consumption and the delay of a cell.

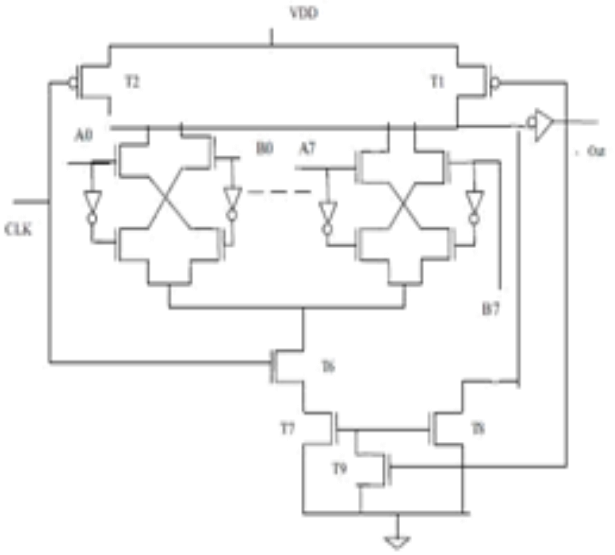

Figure 8: Proposed 8-bit Double-Tail Comparator using Foot Transistor Logic

TABLE I. PERFORMANCE COMPARISON

Technology	**gpdk-180**		
Voltage	**1.8V**	**1.8V**	**1.8V**
	Power (µW)	**Delay (µs)**	**PDP (pJ)**
Existing Single Bit Footed Domino Logic Conventional Comparator	1.772	1.014	1.796
Single Bit Proposed Double Tail Comparator using Foot Transistor Logic	1.507	1.014	1.528
Existing 8- Bit Footed Domino Logic Conventional Comparator	14.18	1.014	14.378
8-Bit Proposed Double Tail Comparator using Foot Transistor Logic	11.439	1.014	11.599

After Simulating in 180nmTechnology, the results obtained for power consumption, delay and PDP has been tabulated in Table 1. For instance, by using 1.8V of power supply, the power consumption of Single Bit Proposed design is 1.507µW, which is 14.9% less than the existing Single Bit Conventional design; whereas the power consumption of 8-Bit Proposed design is 11.439µW which is 19.3% less than the existing 8-Bit Conventional Comparator design.

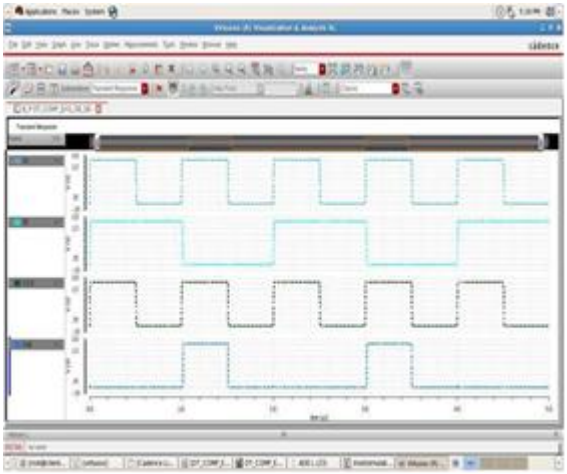

Figure 9: Simulation Results for Existing Single Bit Footed Domino Logic Conventional Comparator Circuit

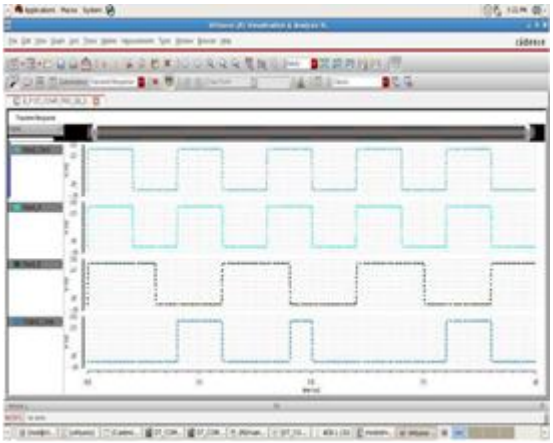

Figure 10: Simulation Results for Single Bit Proposed Comparator Circuit using Foot Transistor Logic

Figure 9 and Figure 10 shows the simulation results obtained for the schematic of single bit Footed Domino Logic Conventional Comparator and Proposed Double-Tail Comparator using foot transistor logic. In these figures the inputs and output for the comparator are labeled as A, B and Out. The circuit is triggered by the input Clock signal. During the positive edge of the clock signal the output of the comparator is obtained. During the negative clock pulse the circuit remains in OFF condition, irrespective of the input signals i.e. the output of the comparator is logic 0 i.e. whenever the clock signal is high the comparator compares the two input signals if there is any match in the input signals then the output is logic 0, if there is any mismatch in the input signals then the output results as logic 1.

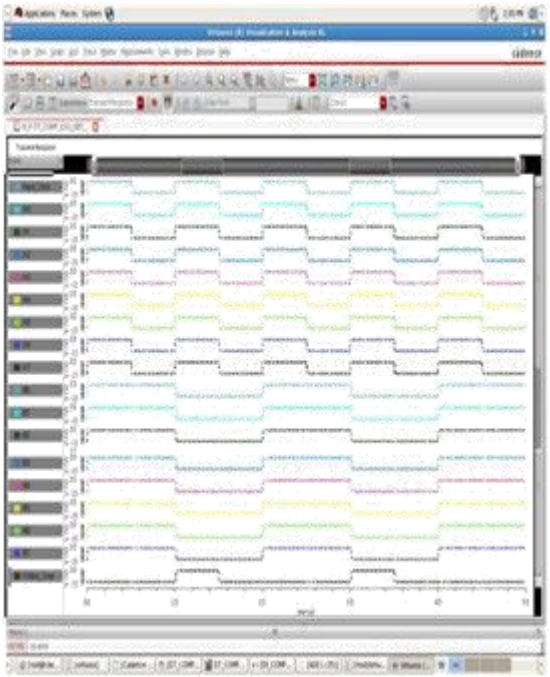

Figure 11: Simulation Results for Existing 8-Bit Footed Domino Logic Conventional Comparator Circuit

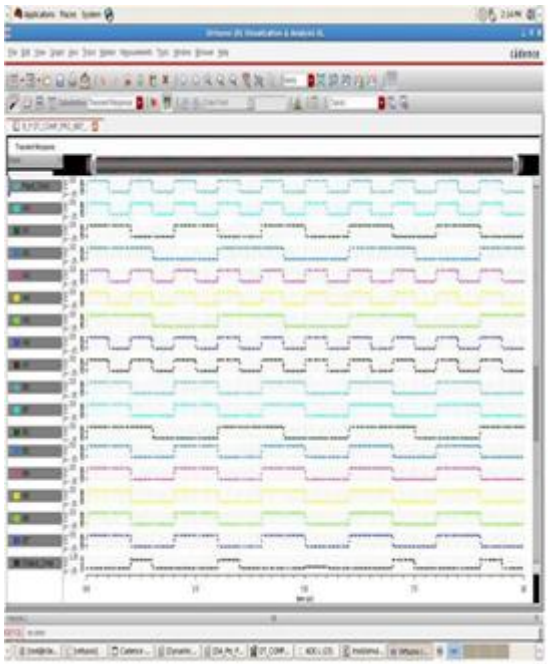

Figure 12: Simulation Results for 8-Bit Proposed Comparator Circuit using Foot Transistor Logic

Figure 11 and Figure 12 shows the simulated waveforms for 8-Bit Footed Domino Logic Conventional Comparator and Proposed Double-Tail Comparator using foot transistor logic circuit. The inputs for these 8-Bit systems are labeled as A0, A1, A2, A3, A4, A5, A6, A7 i.e. A [0:7] and B0, B1, B2, B3,

B4, B5, B6, B7 i.e. B [0:7] whereas the output is labeled as Output_Comp. These 8-Bit existing and proposed systems are triggered by the clock signal labeled as input_clock.

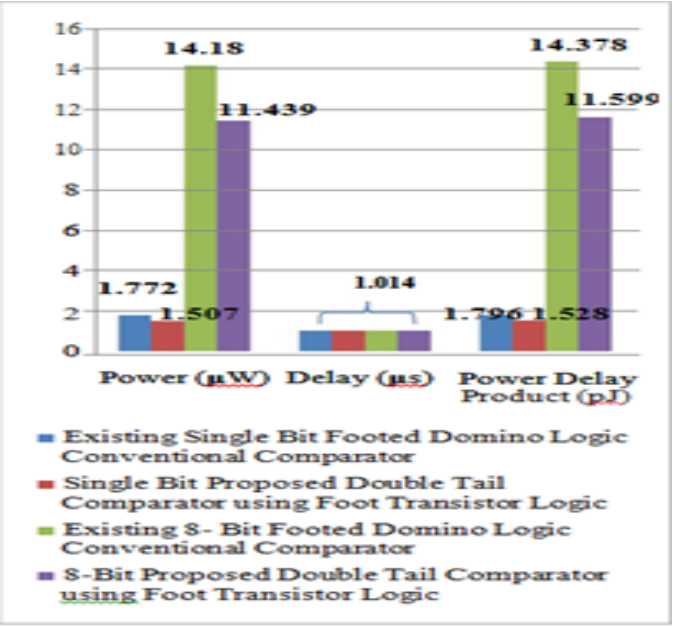

Figure 13: Comparative Analysis

When the clock signal is high if A [0:7] and B [0:7] are equal then the Output_Comp appears as logic 0 else the Output_Comp rises to logic 1. During the negative clock cycle i.e. when Clock =0, the circuit remains in OFF condition, hence the Output_Comp results a logic 0 signal. To analyze the effectiveness of our proposed method, we synthesized the Double-Tail Comparator architecture using Cadence Virtuoso Environment in a 180nm CMOS process technology, in which the design analysis part includes Design Rule Checker (DRC) in Analog Design Editor (ADE) tool. By this the power consumption results are obtained, with the parameters Vdd=1.8V. The Power reduction of our proposed Double-Tail Comparator architecture is shown in Figure 13. By using Foot Transistor Logic in proposed method how the power consumption is reduced compared to existing conventional comparator is indicated in Figure 13. It also shows how the PDP is varied for the existing and proposed circuits and the delay being remained the same. From this Figure 13 we can say that the proposed structure has shown better result in terms of power and PDP.

CONCLUSION

Both the existing system and proposed system are implemented using cadence virtuoso tool using 180nm CMOS technology. The design analysis part includes DRC in Analog Design Editor (ADE) tool. The maximum power and delay timing for single bit and 8-Bit Existing Footed Domino Logic Conventional system are 1.772µW & 1.014µs and 14.18µW & 1.014µs respectively, whereas maximum power and delay timing for single bit and 8-Bit Proposed Double-Tail using Foot Transistor Logic system are 1.507µW & 1.014µs and 11.439µW & 1.014µs respectively. Hence, proposed system will ensure low static power consumption than conventional system. Furthermore the new design reduces the chip area because of Foot Transistor Logic. Hence, the proposed system can be extended for any number of bits depending on designers requirement because the delay timing being the same for any number of bits.

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