International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 12 (2017) pp. 3411-3415
© Research India Publications. http://www.ripublication.com

Design of low threshold Full Adder cell using CNTFET

P Chandrashekar[1], R Karthik[1], O Koteswara Sai Krishna[1] and Ardhi Bhavana[1]

[1] Department of Electronics and Communication Engineering, MLR Institute of Technology, Hyderabad, Telangana, India.

[1]ORCID ID: 0000-0002-1685-8971

Abstract

As there are many drawbacks of CMOS technology such as short channel effects, high power densities, hot carrier affect, decreased gate control, high sensitivity to process variation etc. A new technology called CNTFET (Carbon Nano tube Field effect transistor) has been developed to overcome the drawbacks of CMOS, which was introduced by S.Iijima in 1991 in Nano scale technology. CNTFET and CMOS have the same structure but the channel between the drain and source is replaced with carbon Nano tube. In our study, we have designed a 14 transistor full adder circuit using CNTFET technology with GDI (Gate diffusion input) technique. The GDI approach replaces the wide range of complicated logic function with only few transistors i.e. reduce the count of transistors in the digital circuit. After the designing of the circuit, results of CNTFET and CMOS has been compared using different parameters such as power delay product, propagation delay and power consumption. Simulation result has been carried out using Cadence tool Design System with VIRTUOSO platform.

Keywords: CNTFET; GDI (Gate diffusion input); Power dissipation; Delay.

INTRODUCTION

With the growth in the technology the need for scaling down has increased. The count of transistor in an integrated circuit increases for every two years approximately, this statement is known as Moore's law. There are many false effect of scaling down in CMOS such as high power densities, drain induced barrier lowering and short channel effect[1]. To overcome these effects a new technology has been developed called CNTFET (Carbon Nano tube field effect transistor)[2]. Carbon Nanotube field effect transistor (CNTFET) is the most promising technology to extent due to three reasons: the first one is that the operation principle and the device structure of both the devices (i.e. CNTFET and CMOS) are similar, therefore the CNTFET can use the fundaments of CMOS design. The second reason is that the fabrication process of CNTFET is similar to that of the CMOS. The last reason is that the CNTFET has the current carrying ability[3]-[5].

Based on CNTFET many works have been done, some of them are arithmetic circuits, multiple valued logic circuits and interconnection networks[6]. In many VLSI system such as nano systems, microprocessor and digital signal processing system. Full adder is the basic component which is used in arithmetic circuits[7]-[8]. and the behaviour of the full adder can affect the whole system. Due to extensive use of adder cell in arithmetic function, researchers have come up with the various kinds of distinct logic styles for designing the full adder cell.

CMOS technology is widely used to design a digital circuit, but because of the increase in the demand for high speed, a new technology was developed named pass transistor technology (PTL). The advantage of using PTL is that it uses less number of transistors which leads to low power dissipation, occupies lesser area, lesser interconnection effects and lesser delay[9]-[10]. However there are two main disadvantages of using PTL that is at low power the speed of the circuit is reduced and high rate of power consumption is found. To overcome the disadvantages of PTL a new technology called GDI technology has been introduced which is implemented for low power circuits. The GDI approach replaces complicated logic function by using few transistors i.e. reduces the count of transistors in the circuit.

In our paper we are designing a full adder using Carbon Nano tube FET technology with GDI technique. The simulation result of CNTFET and CMOS is compared (parameters like propagation delay, power consumption and power delay product is also compared).

CARBON NANOTUBE FIELD EFFECT TRANSISTOR

The Nano tube is made up of a graphite sheet which is rolled up in a cylindrical manner. Based on the number of sheets in the Nanotube, it is categorized into two types i.e. Single-wall CNT (SWCNT) and Multi-wall CNT (MWCNT). The property of SWCNT could be metallic or semiconductors which will depend on the chirality vector and is define by (n1, n2) indices. These are used to determine the carbon atom angle along the graphite sheet. It n1 - n2 is not equal to 3k (for all k equal to Z) then SWCNT is known as semiconductor and if

International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 12 (2017) pp. 3411-3415
© Research India Publications. http://www.ripublication.com

n1 – n2 is equal to 3k (for all k equal to Z) then SWCNT is known as conductor. The channel which is used in CNTFET is semiconducting SWCNT. [11] Fig 1 illustrates CNTFET device. The gap between the two carbon nanotubes from its centre is known as pitch and the diameter of the rolled nanotube sheet is denoted as Dcnt. In CNTFET the width of the gate is determined using below equation

$$W_{gate} \approx \text{Min}\,(W_{min},\, N \times pitch) \tag{1}$$

Where, Wmin = gate minimum width

N = Number of Nanotubes

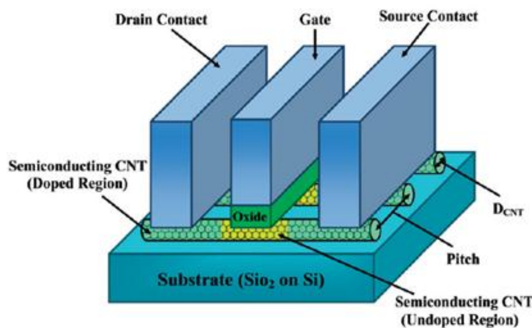

Figure 1: Diagram of CNTFET

The I-V characteristic of MOSFET and CNTFET are same and hence both MOSFET and CNTFET have threshold voltage which is needed for turning on the device. Threshold voltage of the CNTFET can be changed by varying the diameter of the CNTFET.

The threshold voltage of CNTFET is given as follows[11].

$$Vth \cong \frac{Eg}{2e} \cong \frac{\sqrt{3}aV\pi}{3eDcnt} \cong \frac{0.43}{Dcnt\,(nm)} \tag{2}$$

Where,

a ≈ 0.249nm (carbon to carbon atomic distance)

Vπ ≈ 3.033 eV (carbon π-π bond energy)

e = unit electron charge

D_{cnt} = diameter of CNTs

The diameter of CNTs can be calculated using below equation

$$Dcnt \approx \frac{a\sqrt{n1^2+n2^2+n1n2}}{\pi} \approx 0.0783\sqrt{n1^2+n2^2+n1n2} \tag{3}$$

From equation (2) and (3) it is clear that by changing the diameter and wrapping vector i.e. chirality indices (n1, n2), the band gap and threshold voltage of CNTFET will differ.

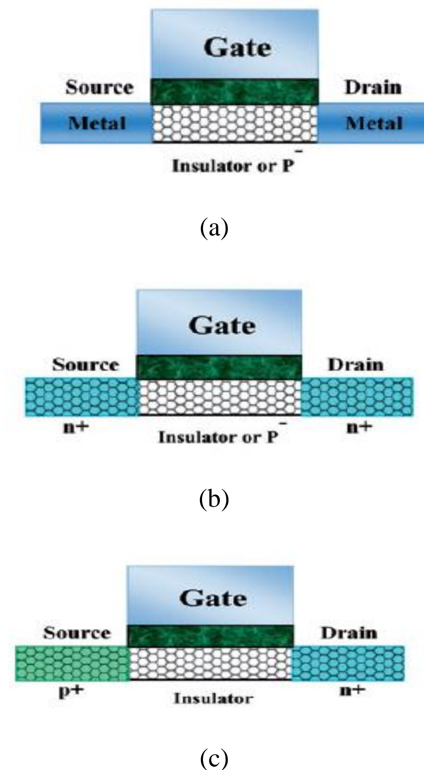

Figure 2: (a) SB-CNTFET (b) MOSFET-like CNTFET (c) T-CNTFET

The three different types of CNTFET are as follows, shown in fig 2

(a) SB-CNTFET

(b) MOSFET-like CNTFET

(c) T-CNTFET

SB-CNTFET is defined as a device where the electrons are tunnelled through SB. Fabrication of CNFET is done using direct contact of the semiconducting nanotube and metal. One of the most important disadvantages of this type is that, the ON state transconductance of the CNTFET will not be allowed by the energy barrier at SB and reduces the current delivery capability, which is directly proportional to the speed of a device.

SB-CNFETs have ambipolar property, due to which these devices are not used in CMOS logic families. This type of CNFET is suitable for high-performance applications. To overcome the drawbacks of SB-CNFET, a new type is developed called MOSFET-like CNTFET (fig 2(b)) which would operate like normal MOSFETs but gives high performance. This type of CNTFET works on the principle of barrier height modulation by the application of the gate

potential. One of most important advantage of MOSFET-like CNFET is that the source channel junction has no SB and therefore, it has higher ON current. As a result, MOSFET-like CNFETs is appropriable for ultra-high-performance of digital devices. The third type of CNFET is called the partially gated CNFET (Fig 2c), has very low current and high cut off characteristics which is suitable for low power applications [12]-[13]. Depending upon the mentioned merits and demerits of CNFETs, different type of CNTFETs is used.

BACKGROUND OF GDI STRUCTURE

Gate Diffusion input (GDI) a new technique of low-power digital circuit design. The GDI approach replaces the wide range of complex logic function with only few transistors i.e. reduce the count of transistors in the digital circuit. It has a simple structure which has less delay and power consumption in digital circuit. Figure 3 shows the basic cell of GDI.

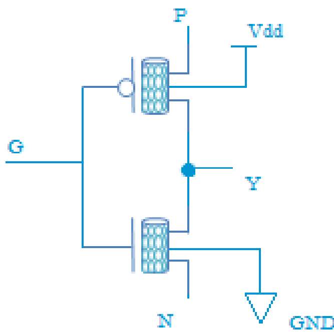

Figure 3: Basic cell of GDI

In the structure of GDI, there are three inputs. Node G is the common input for the gate of PCNT and NCNT, node P is the input source for PCNT and N node is the input source for NCNT. Moreover output node is the drain output for both the gates i.e. PCNT and NCNT. GDI cell is known to be the most efficient methods for implementing high speed and low power logic functions and reducing the chip area[14]-[15]. Various logic function of GDI cell for different input configurations is shown in Table 1.

TABLE I. DIFFERENT LOGIC FUNCTIONS OF GDI CELL FOR DIFFERENT INPUT CONFIGURATION

N	P	G	Out	Function
‘0’	B	A	A’B	F1
B	‘1’	A	A’ + B	F2
‘1’	B	A	A + B	OR
B	‘0’	A	AB	AND
C	B	A	A’B +AC	MUX
‘0’	‘1’	A	A’	NOT

PROPOSED FULL ADDER CELL

1- Bit Full adder cell with three inputs A, B and C and two outputs Sum and Carry as output can logically defined as follow,

$$Sum \quad = ABC + AB'C' + A'BC' + A'B'C$$
$$= A(BC + B'C') + A'(B'C + BC')$$
$$= A(B \oplus C) + A'(B \oplus C)'$$

$$\text{Sum} = A \oplus B \oplus C \quad (4)$$

$$Carry \quad = AB + BC + AC$$
$$= AB + BC(A' + A) + AC(B' + B)$$
$$= AB + A'BC + ABC + AB'C + ABC$$
$$= AB(1 + C) + C(A'B + AB')$$

$$\text{Carry} = AB + C(A \oplus B) \quad (5)$$

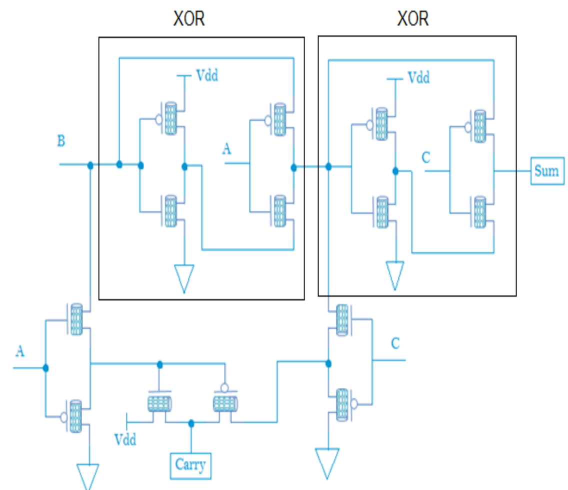

Figure 4: Proposed full adder cell

According to the equation (4) and (5), the full adder cell can be designed using two XOR gates, two AND gates and one OR gate, which gives sum and carry collaterally. The proposed Full adder cell is shown in the Figure 4.

The design consists of seven connecting pairs of GDI cell which produces carry and sum signals. In which GDI based XOR gates are connected serially to generate the sum signal. Carry is generated using the OR gates, AND gates and XOR gates.

SIMULATION RESULTS

The proposed full adder design is evaluated and compared with the CMOS based full adder. All the designs are simulated using spectre simulation model parameters with a supply voltage of 0.6V. The simulation result of CNTFET based full adder is shown in Figure 5.

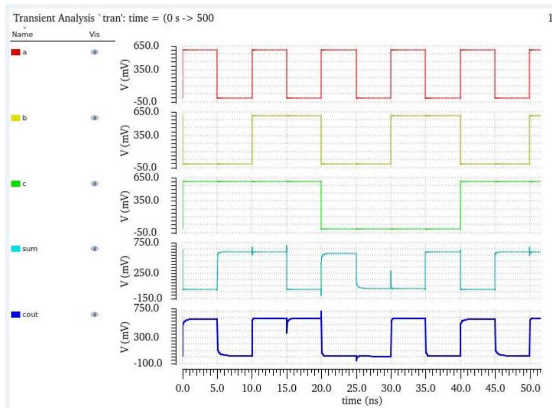

Figure 5: Simulation result of proposed design

Figure 6:

PERFORMANCE EVALUATION

The proposed circuit is simulated using 0.8V. To evaluate the performance of circuit, it is compared with CMOS circuit in term of delay, power consumption and power delay product.

TABLE II. RESULT OF CNTFET ADDER

Parameters	**CMOS**	**CNTFET**
Power dissipation	20289.6 uW	0.00151 uW
Delay	0.031 ns	0.0059 ns
Power delay product (PDP)	$6.29 \times 10^{-13} J$	$8.91 \times 10^{-21} J$

CONCLUSION

In this paper a new full adder circuit has been designed using CNTFET. The various parameters such as propagation delay, power delay product and power consumption are calculated for this proposed design and compared with CMOS. This has resulted in significant reduction in the propagation delay and power consumption of the full adder cell when compared to the existing model.

ACKNOWLEDGMENT

The authors would like to thank the management of MLR Institute of Technology for their support and encouragement.

REFERENCES

[1] P. Saini et.al. " Leakage Power Reduction in CMOS VLSI Circuits," Inernational Journal of Computer Application, pp. 42-48, vol-55- no. 08 , October 2012.

[2] Ali Ghorbani et. al., "energy efficient full adder cell design with using carbon nanotube field effect transistors in 32 nanometer technology", International Journal of VLSI design & Communication Systems (VLSICS) vol.5, no.5, October 2014.

[3] J. Deng, et. al., "Device Modeling and Circuit Performance Evaluation for Nanoscale Devices: Silicon Technology beyond 45 nm Node and Carbon Nanotube Field Effect Transistors", doctoral dissertation, Stanford University, 2007.

[4] M.H. Moaiyeri, et. al., "Design and Evaluation of CNFET-Based Quaternary Circuits," Circuits, Syst.,Signal Process pp. 1631-1652, vol. 31, no. 5, Oct. 2012.

[5] P A Aui, et. al., "carbon nanotubes field effect transistor" A review, Indian Journal Of Pune And Physics, pp.899-909, vol.43, Dec 2005,.

[6] M.A Tehrani, et. al., "Design and implementation of multi-stage interconnection networks using quantum-dot cellular autodata," Microelectronic journal, pp.913-922, vol.42, no.6, june 2011.

[7] A. Molahosseini, et. al., "Efficient reverse converter design for the new 4-moduli set sand based on new CRTs," IEEE Trans. Circuits Syst. I, pp.823-835, vol.54, no., 2010.

[8] K. Navi, et. al., "A hardware-friendly arithmetic method and efficient implementations for designing digital fuzzy adders," Fuzzy Sets and Systems, pp.111-124, vol.185, no.1, 2011.

[9] T. Sakurai, et. al., "Closed form expressions for interconnection coupling, crosstalk, and delay in VLSI's," IEEE Trans. Electron Devices, pp. 118–124, vol. 40, , Jan. 1993.

[10] E. G. Friedman et. al., "Delay and power expressions for a CMOS inverter driving a resistive-capacitive load," Analog Integrate. Circuits Signal Process. pp. 29–39, vol. 14, 1997.

[11] J. Deng, et.al., "Device modelling and circuit performance evaluation for nano scale devices: silicon technology beyond 45 nm node and carbon nanotube field effect transistors", Ph.D. Thesis, Stanford University (2007).

[12] A. Raychowdhury, et. al., "Carbon nanotube electronics: design of highperformance and low-power digital circuit"s, IEEE Trans. Circuits Syst. I Regul. Pap. pp. 2391–2401, vol.54 no.11, (2007).

[13] M.H. Moaiyeri, et. al., "Efficient CNTFETbased ternary full adder cells for nanoelectronics", Nano-Micro Lett, pp.43-50, vol.3 no.1, (2011).

[14] A. Morgenshtein, et. al., "Gate-diffusion input (GDI) - A power efficient method for digital combinatorial", IEEE Trans. VLSI Syst. pp.566-581, 2002.

[15] A. Morgenshtein, et. al., "Asynchronous gate-diffusion-input (GDI) circuits", IEEE Trans. VLSI Syst. pp.847-856, vol.12, no.8, 2004 .