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A Differential Subthreshold SRAM Cell for Ultra-Low Voltage Embedded Computing Applications

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Abstract

With scaling of CMOS technology, data stability of SRAM at ultra-low supply voltage has become a critical issue for embedded wearable computing applications. In this work, we suggest an advanced 8T SRAM cell which can operate properly in subthreshold voltage regime. The cell utilizes a differential swing in the read and write path, and allows an efficient column-interleaving structure. In the read operation, a column-wise assistline scheme of the cell leads to the cell being unaffected by the read disturbance. In addition, the bit-cell keeps the noise-vulnerable data 'low' node voltage close to the ground level during the dummy-read operation, thus producing near-ideal voltage transfer characteristics essential for robust SRAM functionality. In the write access, the boosted wordline facilitates to change the contents of the memory bit. Implementation results with 180 nm CMOS technology exhibit that the proposed cell remains unaffected by the read disturbance, while achieves 59 % higher dummy-read stability and 3.7 times better write-ability at a subthreshold supply voltage compared to the conventional 6T SRAM cell. The stability enhancement provided with the proposed bit-cell is confirmed under process, voltage and temperature variations.

Keywords: SRAM, embedded memory, subthreshold, data stability, 8T cell

INTRODUCTION

Embedded memories are pervasive in modern VLSI system and system-on-chip (SoC) designs. Current embedded memories are dominated by the 6-transistor (6T) SRAMs because of their preferable embedded attributes: logic CMOS compatibility, high speed and low power operation. They are used in different sizes ranging from a few kilobits to a few hundred megabits, and occupy a large area in modern SoCs. However, with scaling of CMOS technology, the SRAM stability at ultra-low supply voltage has become an important issue for wearable computing applications. The 6T based SRAM shows poor functionality in read and write operation, and exhibits a half-select issue in the write operation.

Figure 1 shows a conventional 6T SRAM cell, where N1 and N2 are the drive, P1 and P2 are the load, and N3 and N4 are the access transistors, respectively. The fundamental stability issue of this 6T cell occurs during the read operation. In the read access, the wordline (WL) makes a transition from low to high while the bitline pairs (BL, /BL) are maintained high. The internal node (DN, /DN) of the cell that represents a zero gets upward through the access transistor due to voltage dividing effect across the access transistor and drive transistor. Moreover, the voltage transfer gain of the cell inverter (P1-N1, P2-N2) is lowered due to the parallel connection of the access transistor and the load transistor. This severely deteriorates the cell immunity to the noise. If the 'low' node voltage is higher than the logic threshold of the other cell inverter, the cell contents may be flipped, resulting in a read failure. This also causes the half-select disturbance during the write access. Furthermore, the 6T based cell in the write operation cannot flip easily the contents of the data storage node under ultra-low supply voltage regime. Deteriorating the bit-cell stability increases the fail-bit rate in embedded SRAM array, and thus it often limits the yield of SoCs.

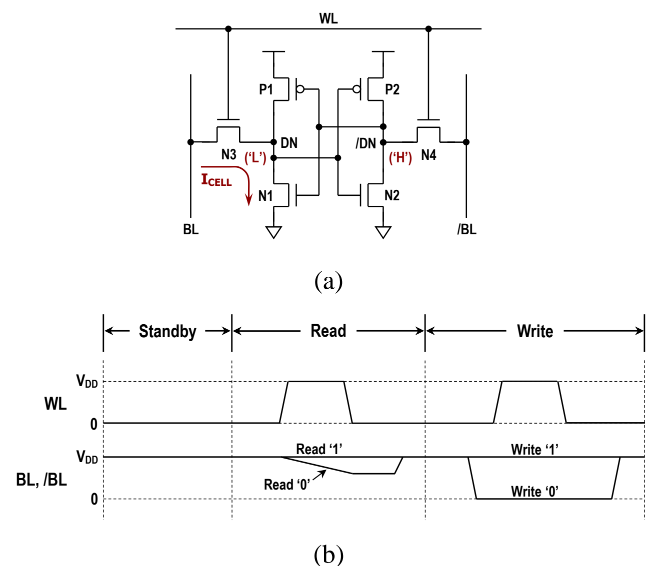

Figure 1: Conventional 6T SRAM cell: (a) schematic, (b) bias conditions for standby, read and write access. (WL: wordline, BL: bitline, /BL: /bitline, DN: data-node, /DN: /data-node, I_{CELL}: read-cell current)

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To overcome this stability issue, many different structures of SRAM bit-cell have been explored. For examples, the 8-transistor (8T) cell [1] may improve the read stability by cutting off pull-down path of the data storage latch during read access, but it has a severely limited read and write capability due to the single-ended bitline structure. Another 8T cell [2], 9-transistor cell [3] or 10-transistor cells [4, 5] decouple the data storage elements and the data output elements, and hence making the read stability equal to the stability during hold mode. Write-ability is equal to that of the 6T cell. However, they suffer the half-select disturbance during the write access, which might be critical to cope with multi-bit errors. They also might suffer an access time degradation due to the single-ended read-bitline structure [2, 4, 5]. A data-aware 8T cell [6], which circumvents the half-select issue in the write operation, consumes a substantial dynamic power because all the non-selected wordlines in the memory array should be toggled during each read and write access. The other 8T cell [7] achieves an exceptional improvement in the read stability, but it finds a difficulty in it's operation at ultra-low supply voltage. The other cell options [8, 9] may increase the read stability, but they carry considerable penalty in the bit-cell area and hence making unacceptable for most applications.

In this work, a novel 8T SRAM cell which can operate properly at subthreshold voltage regime are addressed. The cell utilizes a differential swing in the read and write path. A column by column assistline scheme leads to the cell being unaffected by the read disturbance. It also improves the dummy-read stability, thus there is no half-select issue in the write access. Furthermore, the boosted wordline scheme improves the write-ability. All the results in this work were obtained in a 180 nm logic CMOS technology. Typical threshold voltages of NMOS and PMOS are 0.5 V and -0.47 V, respectively.

Proposed Subthreshold SRAM Bit-Cell

The proposed 8T SRAM cell is shown in Figure 2(a). In its structure, two PMOSs (P3, P4) are added between the access transistor and the drive transistor. Their gates are controlled by a column-wise assistline (CAL). Figure 2(b) illustrates the memory cell bias conditions during the standby mode, read access and write access. In the standby, the bitline pairs (BL, /BL) are connected to the supply voltage (V_{DD}), and the wordline (WL) and CAL are tied to the ground. When the cell is not being accessed, two cross-coupled inverters (P1-N1, P2-N2) hold their bi-stable data.

In the read access, P3 and P4 are initially turned off by raising CAL to V_{DD}, and BL and /BL are discharged to the ground. When WL is going to a boosted voltage V_{PP} ($1.3V_{DD}$ in this design), one of the bitlines is charged depending on the data on the storage nodes (DN, /DN). For example, if DN and /DN store logic '0' and '1' respectively, then the transistor P2 conducts. Hence, a read-cell current (I_{CELL}) will flow to /BL through P2 and N4. Because the data nodes (DN, /DN) are decoupled from the bitline pairs (BL, /BL) during reading the cell, this 8T cell provides a read mechanism that does not disturb the internal stored data, thereby eliminating the read disturbance. After WL goes low and CAL returns to the ground, the positive feedback of cross-coupled inverters (P1-N1, P2-N2) restores the respective data states.

In the write access, the CAL signal is changed to a negative voltage NV_{GG} ($-0.9V_{DD}$ in this design). Initially assume that DN = V_{DD} and /DN = 0. In order to write a zero to the node DN, BL is set to '0' and /BL to V_{DD}. When WL is going to a boosted voltage V_{PP} ($1.3V_{DD}$ in this design), the node PN makes a transition from V_{DD} to a zero. Since the gates of two PMOSs (P3, P4) are biased to a negative voltage, the node DN can be discharged easily from V_{DD} to a zero state. Falling of the node DN brings the inverter P2-N2 to trigger. The positive feedback inside the cell changes the contents of the memory bit.

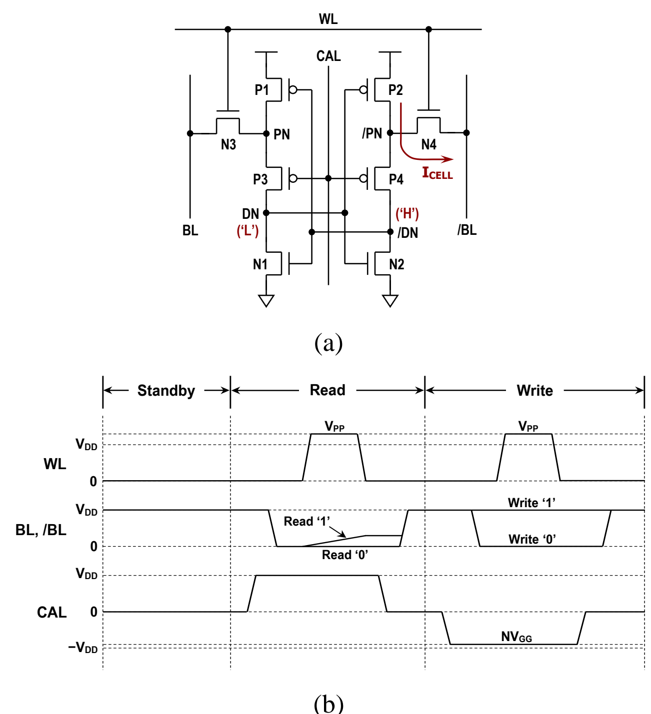


Figure 2: Proposed 8T SRAM bit-cell: (a) schematic, (b) bias conditions for standby, read and write access. (WL: wordline, BL: bitline, /BL: /bitline, CAL: column-wise assistline, DN: data-node, /DN: /data-node, PN: passing-node, /PN: /passing-node, I_{CELL}: read-cell current)

Figure 3 depicts the logical and physical organization of memory block incorporating the proposed 8T SRAM cell. The 32-kbit memory array contains 256 WLs and 128 bitline pairs. The wordlines are driven by row decoders. Each WL selects 128 bits out of which 8 bits are selected by 16:1 column multiplexing. A wordline is selected by 8 address bits. The block is a basic memory building accessible independently

with dedicated address, data-in and data-out buses. Inside the memory array, sense amplifiers, ground dischargers, column gates and column signal drivers are located on the bottom. The CAL drivers and V_{DD} prechargers are positioned on the other side of the array. The CAL drivers control the CAL signal running parallel to the bitlines and feeds eight CALs in common. The remaining core circuits (BSA: block sense amplifier, WDR: write driver) are essentially same as those of conventional SRAM. For each read or write access, a column signal driver and a CAL driver decoded by column address activates only eight of interleaved columns. Whereas, the cells from remaining columns on a selected row will experience a dummy read operation with bitline pairs (BL, /BL) and CALs kept to V_{DD} and the ground respectively.

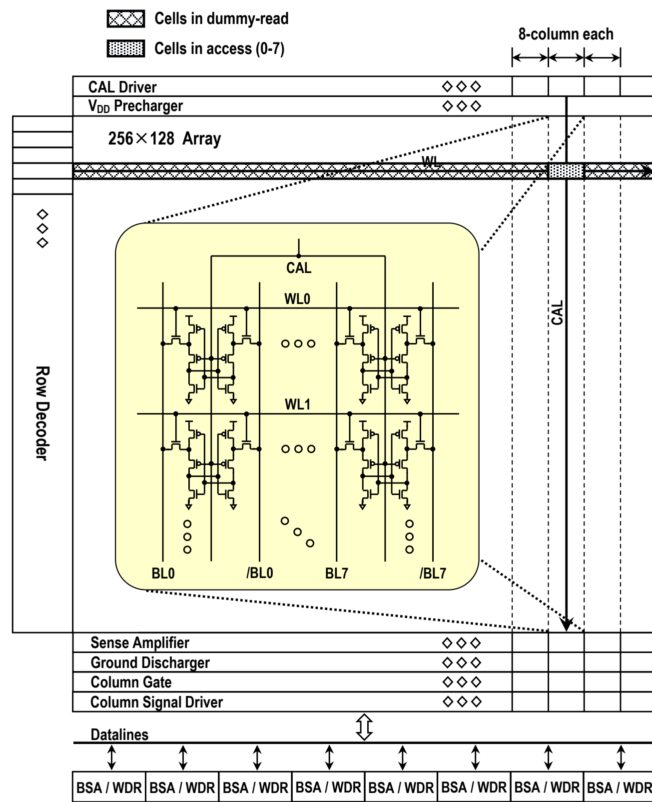
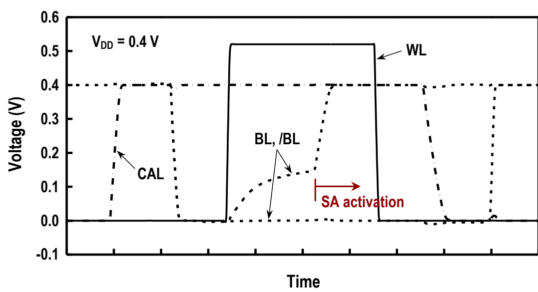
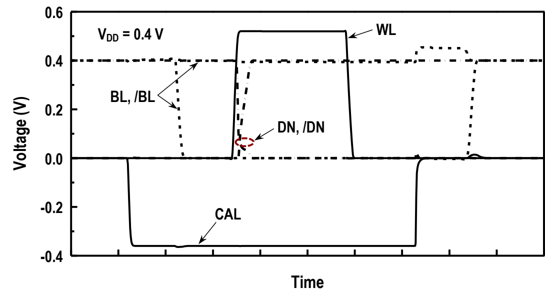


Figure 3: Configuration of proposed 8T SRAM memory block. (BSA: block sense amplifier, WDR: write driver)



(a)



(b)

Figure 4: Simulated waveforms at V_{DD} = 0.4 V: (a) read operation, (b) write operation.

Signal waveforms for the read operation at 0.4 V supply are shown in Figure 4(a). After the V_{DD} prechargers are disabled, a read operation begins by pulling CAL up to V_{DD}. Next, the bitline pairs (BL, /BL) are discharged to the ground. When WL is going up to a boosted V_{PP} level (0.52 V in this work), a read-cell current flows depending on stored data status. If DN is low and /DN is high, I_{CELL} flows to /BL through P2 and N4. This raises the voltage level of /BL with BL maintained to the ground. On the other hand, if /DN is low and DN is high, I_{CELL} flows to BL through P1 and N3. This also raises the voltage level of BL with /BL maintained to the ground. The voltage differences in BL and /BL are sensed and amplified to full-swing signals by the sense amplifier (SA). Figure 4(b) shows waveforms for the write operation at the same 0.4 V supply. After the V_{DD} prechargers are disabled, the write operation begins by pulling CAL down to the negative voltage (-0.36 V in this work). Next, the bitlines are driven with the new data. When the wordline is activated later on, the cell data nodes (DN, /DN) flip from one state to another immediately. After the wordline is switched again to the ground, CAL returns to the ground, and both BL and /BL are precharged to V_{DD}.

Bit-Cell Performance

A. Bit Area

For comparisons of various SRAM stability metrics, the conventional 6T and proposed 8T SRAMs have been implemented in a 180 nm logic CMOS technology. Figure 5 shows the layouts of the 6T and 8T cells. For the 6T cell, the width of drive transistor (N1, N2) is 420 nm while the width of other transistors is 220 nm. For the proposed 8T cell, the width of access transistor (N3, N4) is 420 nm while the other transistors have a width of 220 nm. All devices in both cells have a minimum channel length of 180 nm to minimize the cell area. The proposed 8T SRAM cell consumes about 44 % larger area compared to the 6T cell. In more scaled CMOS technology such as 65 nm, 45 nm and beyond, the area overhead may be remained in a same degree since both 6T and 8T cells will be scaled in a same way.

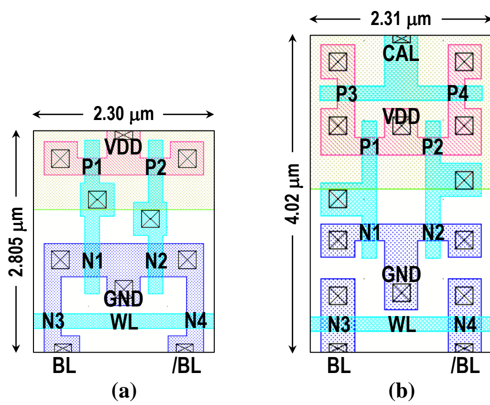


Figure 5: SRAM cell layout in 180 nm CMOS technology: (a) conventional 6T cell, (b) proposed 8T cell.

B. Read Stability

Figure 6 shows the butterfly curve for the conventional 6T SRAM cell. The static noise margin (SNM) [10], which is a common measure of the ability for the cell to maintain their state during the read operation, is graphically defined as the length of side of the possible maximum square between the normal and inverse voltage transfer characteristic of two identical cell inverters. At 0.4 V and room temperature, the SNM of the conventional 6T cell is 92 mV. On the other hand, the read operation of the proposed 8T cell is performed with CAL kept high. The CAL signal decouples the data nodes (DN, /DN) from the bitline pairs (BL, /BL) during reading the cell, which reduces the read failure probability and improves the read operating margin. The read operation is ultimately performed without affection of disturbance.

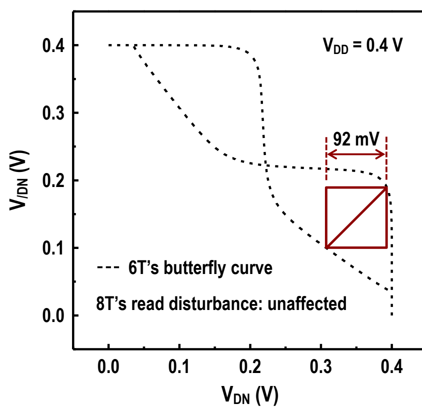
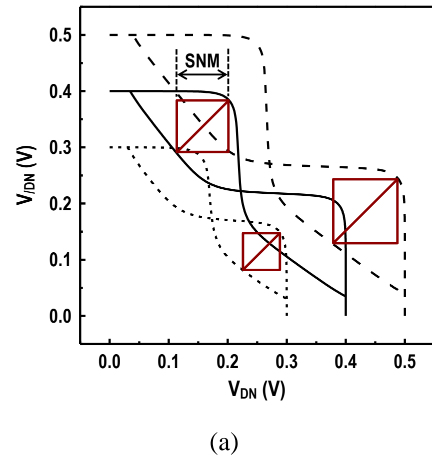
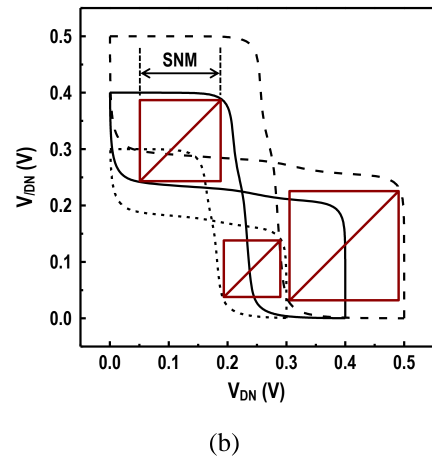


Figure 6: Butterfly curve for 6T cell read operation at V_{DD} = 0.4 V and room temperature.



(a)



(b)

Figure 7: Butterfly curves for dummy-read operation at T = 25 ℃: (a) conventional 6T cell, (b) proposed 8T cell. (dashed curve: V_{DD} = 0.5 V, solid curve: V_{DD} = 0.4 V, dotted curve: V_{DD} = 0.3 V)

C. Dummy-Read Stability

Figure 7 shows the butterfly curves for the memory cells experiencing a dummy read operation during the read or write access. In the 6T cell, the dummy-read SNM is exactly same as the read SNM. When DN is increased from 0 to V_{DD} with WL = high and BL = /BL = V_{DD}, the other node /DN makes a transition from V_{DD} to 0. During this time, the /DN voltage of the proposed 8T cell is much lowered to the ground, due to an additional voltage drop in P4. This gives near-ideal voltage transfer characteristics essential for robust SRAM cell design. At 0.4 V and 25 ℃, the dummy-read SNM of 8T cell is 147 mV while that of 6T cell is 92 mV, exhibiting 59 % higher dummy-read stability.

The dummy-read stability for different process corners is evaluated in Figure 8. Process parameters have a three-sigma (3σ) variation. Here, TT means typical-NMOS and typical-PMOS, FS means fast-NMOS and slow-PMOS, and SF means slow-NMOS and fast-PMOS, etc. At typical (TT, 25 ℃),

worst-speed (SS, -40 ℃) and worst-power (FF, 85 ℃) conditions, the dummy-read SNM of 8T cell is 59 %, 155 % and 28 % higher compared to the 6T cell counterpart. In a specific FS corner, the logic threshold voltage of the cell inverter would be decreased and thus getting the stability worse. At 0.4 V room temperature, the dummy-read SNM variation between extreme corners (TT, FS) is 25 mV in the 8T cell compared to 50 mV in the 6T cell, indicating better process variation tolerance.

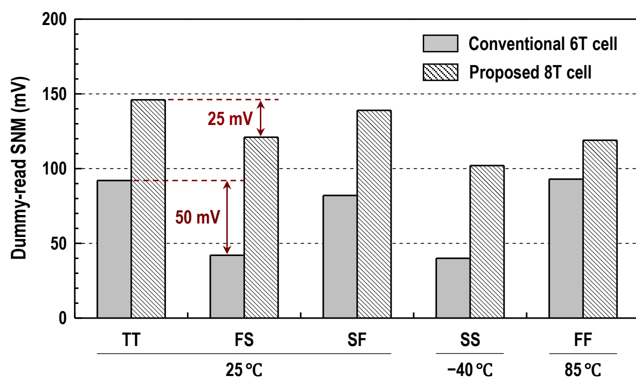
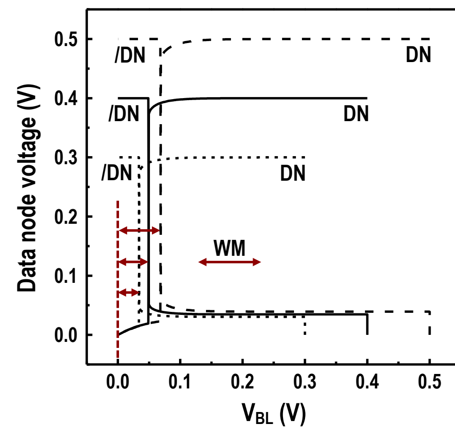


Figure 8: Comparison of dummy-read SNM at V_{DD} = 0.4 V. (TT: typical-NMOS/typical-PMOS, FS: fast-NMOS/slow-PMOS, SF: slow-NMOS/fast-PMOS, SS: slow-NMOS/slow-PMOS, FF: fast-NMOS/fast-PMOS)

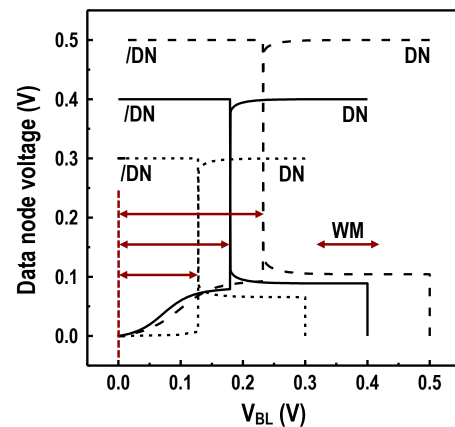
D. Write-Ability

Data write-ability, which indicates how easy or difficult to write into the cell, is also compared in Figure 9. The write margin (WM) in this work is defined as the BL voltage needed to flip the cell content when the BL voltage is swept downward from V_{DD} with WL = high [11]. The larger BL voltage, the easier it is to write into the cell. At 0.4 V and 25 ℃, WM of the 8T cell measures 180 mV while that of 6T cell is 48.6 mV. The proposed cell exhibits 3.7 times larger write-ability compared with that of 6T cell.

The write-ability for different process corners is illustrated in Figure 10. In the write operation of the proposed 8T SRAM cell, a boosted voltage on the wordline enables the bit-cell to achieve better write-ability for ultra-low supply voltage. As the result, WM of 8T cell remains 3.7 to 5.4 times higher over the 6T cell except FS corner. In a specific FS condition, the current conducting capability of the access transistors (N3, N4) is much stronger compared to the load transistors (P1, P2), getting better write-ability than other process conditions in both cells. But the variation in WM across skewed process corners (FS, SF) at 0.4 V and 25 ℃ is 68 mV in the 8T cell compared to 184 mV in the 6T cell, showing better process variation tolerance.



(a)



(b)

Figure 9: Data write-ability at T = 25 ℃: (a) conventional 6T cell, (b) proposed 8T cell. (dashed curve: V_{DD} = 0.5 V, solid curve: V_{DD} = 0.4 V, dotted curve: V_{DD} = 0.3 V)

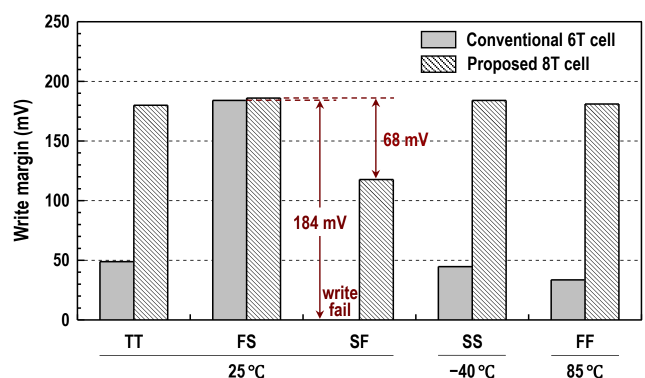


Figure 10: Comparison of write margin at V_{DD} = 0.4 V.

CONCLUSION

In this paper, we have presented a subthreshold 8T SRAM cell realized with the addition of two extra PMOS transistors. It incorporates a differential read and write path suitable for high-performance wearable computing applications. In

addition, the cell allows an efficient column-interleaving structure for soft-error immunity. In the dummy-read condition, the 8T cell represses the data 'low' node voltage rising, thereby enhancing the static noise margin by 59 % at 0.4 V supply compared to the conventional 6T SRAM cell. The cell also exhibits 3.7 times higher write margin with the aid of a boosted wordline scheme. The bit-cell itself bears an improved variability tolerance that gives much tight stability distribution across skewed process corners. Furthermore, the cell remains unaffected by the read disturbance. Using a 180 nm CMOS technology, the effectiveness of the proposed SRAM cell, which can be applicable to the deep scaled logic CMOS process, has been verified under various process, voltage and temperature variations. The bit-cell can be an attractive choice for ultra-low voltage SRAM applications.

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