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Linearity Enhancement Technique for GHz-Band LNA

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Abstract

This paper presents linearity enhancement technique for GHz-band low noise amplifier (LNA). To verify this technique, we designed LNA using 0.18-µm BiCMOS process. Linearity is very important parameter for LNA. The MOS-BJT derivative superposition (MBDS) technique is exploited by a parallel LC tank in the emitter of bipolar transistor to reduce the second-order non-linear coefficient (g_{m2}) related to the enhancement limitation of linearity performance. To adjust the phase of third-order non-linear coefficients of bipolar and MOS transistors, and to improve the linearity characteristics, we use two feedback capacitances in parallel with the base-collector and gate-drain capacitances. The proposed LNA showed excellent IIP3 of 25.2dBm and 7.5dBm at the frequency of 2.4GHz and 24GHz as compared to conventional results, respectively.

Keywords: Linearity, BiCMOS, Low Noise Amplifier (LNA), RF IC, MBDS technique, Derivative Superposition (DS)

INTRODUCTION

One may only need to high third-order linearity for narrowband RF IC design, while we need to consider both the second-order and third-order distortions for UWB circuit design due to the large numbers of in-band interferences and the cross-modulation/inter-modulation caused by blockers or transmitter leakage [1-8]. In the modern wireless communication systems such as WLAN, UMTS, PCS and 4G LTE due to the large-scaled interference signals at the input port of the low noise amplifier (LNA) and mixer, high linearity is an important requirement for broadband receivers. Several techniques have been proposed to obtain high linearity such as pre-distortion method, feedforward technique, Derivative superposition (DS), etc. Numerous publications have reported this field, and active study is still underway [1-12].

In this paper, we present linearity improvement technique for LNA and mixer with GHz band. LNA and mixer are designed using 0.18-µm RF BiCMOS technology. We suggest the MOS-BJT derivative superposition (MBDS) technique by a parallel LC tank in the emitter of bipolar transistor to reduce the second-order non-linear coefficient.

CIRCUIT DESIGN AND LINEARIZATION

Overview of Linearization

Several techniques have been proposed to obtain high linearity such as pre-distortion method, feedforward technique, Derivative superposition (DS), etc. The pre-distortion method adds a nonlinear element (also called linearizer) prior to an amplifier such that the combined transfer characteristic of the two devices is linear [9]. It is practically impossible to cancel all orders of nonlinearity simultaneously. Therefore, the linearizer is usually designed to cancel the nonlinearity of a certain order. Optimum gate biasing technique is based on the bias condition of the transistors at zero crossing point. The LNA achieves high linearity but the bottlenecks of this technique are that the bias point is bound to change due to the process variations, and the region over which this linearity boost can be obtained is very narrow [9].

The feedforward system has been used in many applications because of its unconditionally stable characteristics and ability to provide a broad-band and highly linear amplifier [4, 10]. However, the feedforward technique is very sensitive to component tolerance and drift, and it requires adaptive control [10].

Derivative superposition (DS) is the most favorite linearization technique to achieve high linearity [11-12]. The DS is a special case of the feedforward technique. It consists of two parallel transistors. Main transistor works in the strong inversion region and the auxiliary transistor works in the weak inversion region. In DS method, by tuning the sizes and bias conditions of the transistors, the third-order nonlinear transconductance coefficient (g_{m3}) can be closed to zero. However, it is not necessary to completely eliminate the second-order nonlinear transconductance coefficient (g_{m2}) contribution to third-order intermodulation (IM_3). It is noteworthy that since DS method employs multiple transistors in parallel with their gates

connected together, it is also called the "multiple gated transistor technique (MGTR)". Since in the DS technique the auxiliary transistor is biased in the triode region, the negative peak magnitude of g_{m3} is much smaller than the g_{m3} positive peak of the main transistor.

Fundamentals

The major factor for nonlinear behavior of the RF blocks in transistors is the nonlinear voltage-current relationship, and it is further degraded as the scaling down of the technology. The voltage-current relationship of transistors is described in Eq. (1) [2].

$$i = g_{m1}v + g_{m2}v^2 + g_{m3}v^3 \quad (1)$$

where g_{mi}, (i=1,2,3) is the i^{th}-order nonlinear coefficient. The *IIP3* is the most important parameter for monitoring the linearity performance of the whole LNA circuit and can be expressed as Eq. (2) [4, 13-15].

$$IIP3 = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{g_{m3}}\right|} \quad (2)$$

Therefore, g_{m3} is the main source of non-linearity in LNAs, and the linearity can be enhanced by cancelling out it. The Taylor expansion series of bipolar transistor can be approximated as Eqs. (3)~(4) [2, 13-14].

$$i_{CE} = \alpha_1 v_{be} + \alpha_2 v_{be}^2 + \alpha_3 v_{be}^3 \quad (3)$$

$$i_{CE} = I_{S0} e^{\frac{V_{BEQ}+v_{be}}{\varphi_t}} = I_{S0} e^{\frac{V_{BEQ}}{\varphi_t}} e^{\frac{v_{be}}{\varphi_t}} = I_Q e^{\frac{v_{be}}{\varphi_t}} \quad (4)$$

where V_{BEQ} is the base-to-emitter bias voltage, I_{S0} is saturation current, and φ_t is the thermal voltage. The third-order coefficient can be written as Eq. (5) [2, 13-14].

$$\alpha_3 = \frac{I_Q}{6\varphi_t^3} \quad (5)$$

According to Eq. (5), α_3 has positive value due to the exponential relationship between the collector current and base-to-emitter voltage. For MOS transistor with negative third-order coefficient the voltage-current relationship is expressed as Eqs. (6)~(10) [2, 13-14].

$$i_{DS} = \beta_1 v_{gs} + \beta_2 v_{gs}^2 + \beta_3 v_{gs}^3 \quad (6)$$

$$i_{DS} = K\frac{x^2}{1+\theta x} \quad (7)$$

$$x = 2\eta\phi_t \, ln\left(1 + e^{\left(\frac{V_{gs}-V_{th}}{2\eta\phi_t}\right)}\right) \quad (8)$$

$$\beta_3 = -\frac{\theta K}{(1+\theta V_{eff})^4} \quad (9)$$

$$\begin{aligned} i_{out} = i_{DS} + i_{CE} &= (\alpha_1+\beta_1)v_{in} + (\alpha_2+\beta_2)v_{in}^2 \\ &+ (\alpha_3+\beta_3)v_{in}^3 \\ &= g_{m1}v_{in} + g_{m2}v_{in}^2 + g_{m3}v_{in}^3 \end{aligned} \quad (10)$$

where K =0.5$\mu_o C_{ox} W/L$, μ_0 is the mobility, C_{ox} is the gate capacitance per unit area, θ is the normal field mobility degradation factor, V_{eff} =V_{gs0}-V_{th}, and V_{gs0} is the gate source dc bias voltage.

Proposed Linearization Technique

In this paper, we employ the MOS-BJT derivative superposition (MBDS) technique by cascode configuration to further reduce the second-order nonlinear coefficient. It is connected by a parallel LC tank in the emitter of bipolar transistor to reduce the second-order non-linear coefficient (g_{m2}) related to the enhancement limitation of linearity performance [2].

Figure 1 shows the second-order and higher harmonics with and without the LC tank. The LC tank attenuates specially second-order harmonics.

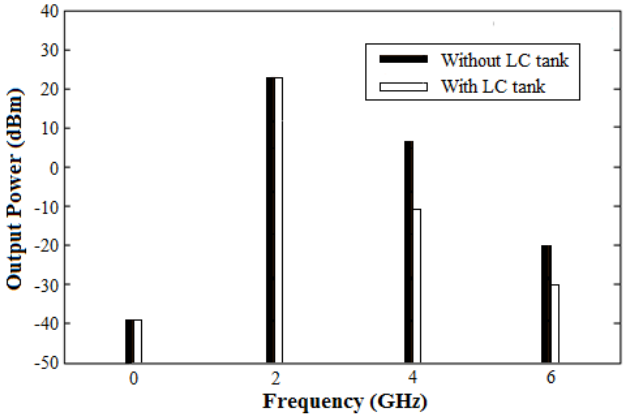

Figure 1: Rejection of second and higher harmonics of the output power by using LC tank.

RESULTS

Figure 2 shows third-order intercept point (*IIP3*) of the low noise amplifier (LNA) at the operation frequency of 2.4GHz. Linearity in LNA is typically measured in terms of *IIP3* which is required to be maximized in reference [2]. Two-tone test was performed at 2GHz with the spacing of 100MHz. The *IIP3* of the LNA was maximized by employing MBDS

technique. We analyze the effect of nonlinear capacitances such as gate-to-source (or base-to-emitter) and gate-to-drain (or base-to-collector) as well as transcoundactance, g_m (or β_F) to improve the linearity. As shown in Figure 2, the proposed LNA showed highest *IIP3* of 25.2dBm as compared to conventional results [9-12].

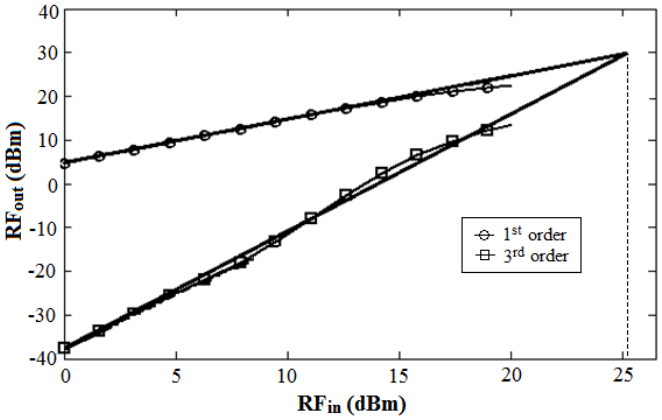

Figure 2: *IIP3* of 2.4GHz LNA.

With the nature of cascading stages, the linearity of the receiver frontend mainly depends on the LNA and mixer. In this paper, the complementary push-pull topology is adopted in the 24GHz LNA stage for the improvement of gain compression and third-order intercept point (*IIP3*). Alternatively, the desirable circuit linearity is achieved by optimizing the device size and bias condition of this particular design. Figure 3 shows *IIP3* at the operation frequency of 24GHz. The proposed LNA showed excellent *IIP3* of 7.5dBm for the 24GHz. As shown in Figure 2, the proposed LNA showed highest *IIP3* as compared to conventional results [9-12].

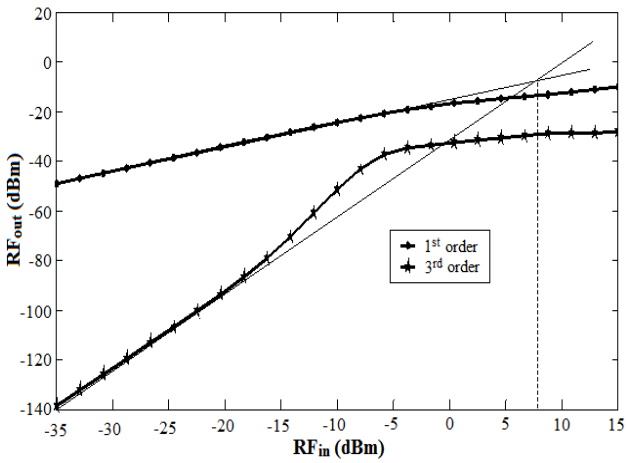

Figure 3: *IIP3* of 24GHz LNA.

CONCLUSION

In this paper, we propose linearity enhancement technique for GHz-band LNA. We designed low noise amplifier (LNA) using 0.18-µm BiCMOS process to verify this technique. We also examined the MOS-BJT derivative superposition (MBDS) technique by a parallel LC tank in the emitter (or source) of bipolar transistor (or MOSFET) to reduce the second-order non-linear coefficient. The proposed LNA showed excellent *IIP3* of 25.2dBm at the frequency of 2.4GHz. The 24GHz LNA also showed excellent *IIP3* of 7.5dBm at the operation frequency as compared to conventional results.

ACKNOWLEDGMENTS

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