International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 20 (2017) pp. 9459-9466

A Framework for Non-Contact Wafer Level Testing of Wireless NoC-based SoCs

Muhammad Adil Ansari[1,*], Umair Saeed Solangi[1], Mohsin Shaikh[2], Kashif Hussain Memon[3], Shafiullah Soomro[4], Abdul Rahim Ansari[5]

[1]*Electronic Engineering Department, Quaid-e- Awam University, College of Engineering, Science & Technology, Pakistan.*
[2]*Computer Engineering Department, Quaid-e- Awam University, College of Engineering, Science & Technology, Pakistan.*
[3]*Computer Engineering Department, The Islamia University of Bahawalpur, Pakistan.*
[4]*Computer Engineering Department, Chung-Ang University, South Korea.*
[5]*Computer Science & Engineering Department, Hanyang University, South Korea.*

Abstract

Computational power and customers' demand of sophisticated devices are evolving complex systems integrated into a chip. Recently, wireless network-on-chip (WiNoC) is developed as an on-chip interconnect for complex integrated circuits (ICs) to resolve the issues of latency, power consumption, throughput etc. The post-fabrication testing of such complex ICs is also a challenging job, especially in order to perform direct contact testing of wafer level VLSI chips. One of the reasons is the increasing density of contact pads that has direct impact from the increasing complexity of ICs. This paper presents a framework for non-contact wafer-level testing of WiNoC-based system-on-chip, while reusing on-chip communication infrastructure. It is scalable with respect to the technological advancements and offers significant advantages over conventional direct-contact and non-contact testing methods.

Keywords: Design-for-testability, non-contact testing, wafer-level VLSI testing, wireless NoC.

INTRODUCTION AND MOTIVATION

The continued advancements in semiconductor industry has evolved multicore system-on-chip (SoC), which serves wide range of applications, e.g., computation, instrumentation, automation, electronic communication. For modern multicore SoCs, the on-chip interconnect is one of the major concern to achieve high throughput, scalability, power efficiency and concurrency. Network-on-chip (NoC) is considered a potential candidate to overcome the issues of the traditional bus-based interconnects and it has qualified to integrate a large number of cores into a single chip, e.g., 1600 cores [1]. However, with metallic planar interconnects, the communication between the distant cores results utilization of more network resources, routing troubles, significant power consumption and higher latency due to multi-hop path [2]. To overcome these issues, wireless NoC (WiNoC) architecture has been evolved [3]–[6]. In WiNoC, certain routing nodes are optimally replaced with wireless nodes, which improve communication latency between distant nodes. A wireless node includes a router, a transceiver, and an antenna. The succeeding section introduces WiNoC architecture and their developments.

Such developments evolve new challenges in the domain of design-for-testability (DfT) [7]. The scan testing is widely used DfT technique, which allow to control the state of circuit nodes and observe response of a circuit node based on the applied test stimulus data [7]. During scan test, (1) test stimuli data is sequentially shifted in to the controllable points by automatic test equipment (ATE), (2) the shifted data is applied to the combinational logic and the response is captured into the observation points, and (3) the captured responses is sequentially shifted out to ATE. Due to long shift operation, the switching activity causes significant dynamic power consumption [8]; thus, the shift operation is performed at low frequency, e.g., 50 MHz [9]. However, due to developments in test equipment, the tester channel frequency has reached in giga-hertz range [10]. To improve yield, a chip is tested at wafer-level to sort good dies, which are then packaged and tested again (package-level test).

Besides, the downscaling of semiconductor devices shrinks the dimensions of I/O pads that causes difficulties at wafer-level testing. The probe needles' size cannot pace with the scaling of the size and pitch of I/O pad. This technological bottleneck constrains further miniaturization of the I/O pads, which in turn limits the density of dies per wafer as well as the maximal utilization of the developments in the test equipment.

Moreover, the I/O pads are susceptible to direct contact of probe needles, which can cause severe damage to the pads, while establishing an adequate electrical contact.. On the other hand, the regular cleaning of probe needles and the number of mechanical contacts limit the life of probe needles, which require regular replacement.

These factors may collectively make the conventional direct contact testing methods costly for the future dense integrated circuits. To circumvent these issues, wireless or non-contact testing methods have been proposed (see Section "NON-CONTACT TEST METHODS"), in which the digital test data is exchanged between the probe card and the device-under-test

(DUT) without physical contact. However, the power is distributed with direct physical contacts, which might also be replaced with non-contact links in future. Thus, the requirement of number probe needles per DUT decreases, which decreases the needle cost, reduces the efforts to clean, replace and align them; moreover, the number of die per wafer increases. However, the conventional non-contact test methods require test dedicated wireless nodes.

However, we attempt to reuse on-chip wireless communication infrastructure of WiNoC for wafer-level testing and present a framework in Section "NON-CONTACT WAFER-LEVEL TESTING OF WINOC-BASED SOCS". The proposed method can result in wider alignment margin, copes with signal interference, efficiently utilizes on-chip communication infrastructure, increases die density per wafer.

WIRELESS NOC (WINOC)

Figure 1 illustrates a generic WiNoC architecture. The example in the figure illustrates four wireless nodes and each is directly connected to four different cores through metallic wires. An antenna and a transceiver are important component of a wireless node. On-chip communication through directional [11][2] and omni-directional [12][5] antennae have been demonstrated. A directional antenna provides high gain to a certain direction; however, an omni-directional antenna essentially radiates to all directions. For high throughput and energy efficient communication, the transceiver circuitry should provide a wide bandwidth and low power consumption [4].

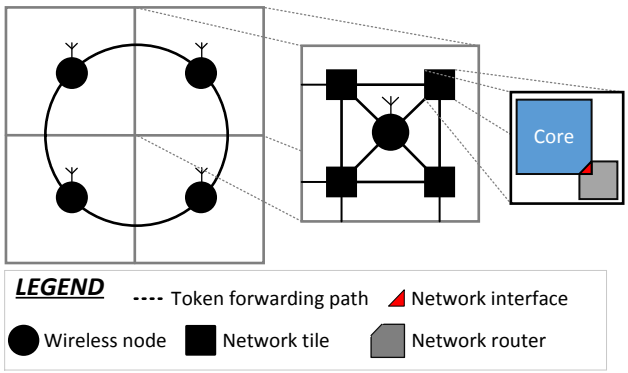

Figure 1: Generic WiNoC architecture

The inter-channel interference for on-chip communication can be avoided by using token passing protocol [3], low transmission power [13], time-division-multiplexing (TDM) and frequency-division-multiplexing (FDM) [12] or multiple access mechanism such as frequency-division-multiple-access (FDMA) [14], code-division-multiple-access [15]. This work considers token passing protocol to discuss the proposed framework.

The token passing ring path among wireless nodes is shown as a circle in Figure 1. In token passing protocol, the token bearer gets the access of wireless channel and initially broadcasts the packet header over the wireless channel. Since all omnidirectional antennae are tuned on the same frequency band, each wireless node receives the header flit. A wireless node accepts the entire packet, if the destination address matches with the corresponding receiver's address.

NON-CONTACT TEST METHODS

The wireless link in non-contact testing methods can be developed by radio frequency coupling (RFC) [13], [16]–[18], capacitive coupling (CC) [19]–[21] or inductive coupling (IC) [22], [23]. Non-contact testing increases misalignment margin and reduces the proximity issue compared to the direct contact testing [19]. These schemes require multiple test dedicated on-chip wireless nodes to establish parallel link.

The CC-based interface is cost effective as compared to the other two interfaces, in terms of fabrication fineness and footprint area [19]. However, a higher communication range and data rate can be achieved with RFC-based interface. According to the recent investigations, the communication at mm-wave range is a viable technology [3]. Lin et al. [24] demonstrated silicon integrated antenna and corresponding circuitry for intra- and inter- chip communication. However, such technology is restricted by the inter-channel interference to develop parallel link between probe card and DUT.

Trichopoulos et al. [25] have presented a validation of a new non-contact testing method, which allows to be operated at THz frequencies. However, its practical ability is yet to be decided because of its cost. In contrast, the work in hand exploits the wireless communication infrastructure of WiNoC to exchange the test data between probe card and DUT and the power is supplied through direct contact.

NON-CONTACT WAFER-LEVEL TESTING OF WINOC-BASED SOCS

Significant research has been conducted to reuse on-chip interconnects as test access mechanisms (TAMs) to transport the test data between the connected cores and ATE. Since the developments on WiNoC architectures offer significant advantages over the planar NoC, we reuse the WiNoC infrastructure as TAM.

The principal concept of the proposed test method is illustrated in Figure 2. In order to achieve a contactless testing, we need to develop the probe card that complies with the technology and the protocol of the on-chip wireless interconnect infrastructure. The desired probe card development is not the scope of this paper. The WiNoC architectures with different kinds of transmission techniques have been discussed in [3]. We confine

our discussion to the WiNoCs with Omni-directional antenna having token passing protocol [3], [4], [12], [26], [27].

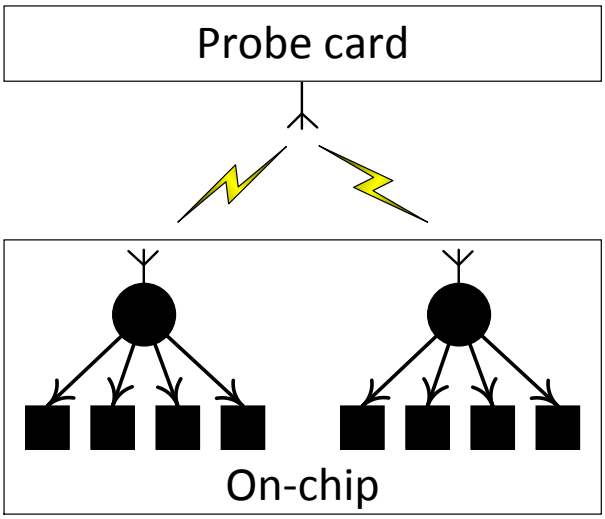

Figure 2: Basic concept of non-contact test method for WiNoC-based SoCs

The omni-directional antenna can be reused for the test access; in contrast, if the WiNoC uses directional antennae [3], then a test dedicated antenna is required that is directed (upwards) towards the probe card. The test dedicated directional antenna can either share one of the on-chip transceiver in time-division or token-sharing manner, or a test dedicated transceiver is embedded.

During test mode the wireless node on the probe card needs to be the part of token ring of on-chip wireless nodes. Since each on-chip wireless node has its unique address (from 1 to r), on-probe wireless node is also assigned a unique address (i.e. $r+1$). Figure 3 shows the logical path for a token ring among on-chip and on-probe wireless nodes. During test mode the r^{th} wireless node forwards the token to $(r+1)^{th}$ node rather than node 1. The red dashed lines show the token forwarding path during test mode. Since the wireless nodes offer high data rate and the test is performed at low frequency due to scan-test power constraint, the test data bandwidth can be leveraged by exchanging the test data with multiple cores-under-test (CUTs)

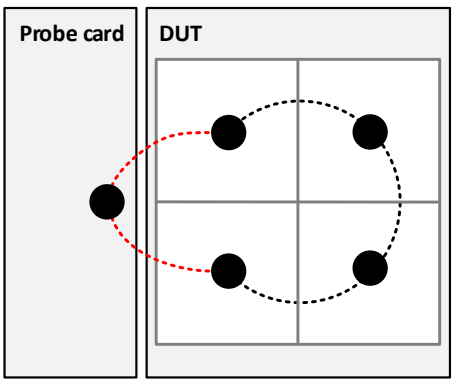

Figure 3: Token ring formation during test mode

of a DUT in time-division manner, as discussed in sub section "Time-Multiplexed Testing". The on-probe wireless node transmits multiple test stimuli packets, while it bears the token custody, and then forwards the token to node 1. The on-chip wireless nodes transmit the response packets for the on-probe wireless node while they hold the token custody. The number of packets to be transmitted by the on-probe wireless node depends upon the number of time-slots, as discussed in sub section "Case Study for Scalability".

Since the token passing protocol grants permission to only one wireless node to transmit over the wireless medium, a single wireless node is sufficient on probe card for both the test stimuli and the test response sharing. However, the WiNoCs with directional antennae can allow using multiple wireless nodes to share the test data between probe card and DUT, which increases the bandwidth between them. However, the frequency allocation to on-probe wireless node needs to be considered by design and DfT engineers.

The WiNoC-based SoCs can be tested by three methods (see Figure 4); with traditional single or multiple direct contact access points [1], [28], [29], with conventional non-contact test methods [13], [19], [21] and with the proposed non-contact test method. The access point translates between the tester protocol and network protocol.

In both the direct contact and the conventional non-contact testing methods, there is physical contact between access point and I/O pads. However, the link between I/O pads and the probe card is made with physical contact of probe needles and any non-contact coupling method, respectively (refer Figure 4). The conventional non-contact testing methods require multiple test dedicated wireless nodes. Each wireless node is associated with an I/O pad and those can be connected to one or more access points. The test parallelism can be achieved with TDM [30], [31], using multiple access points [28], [31] or test packet multicasting [32]. On-chip phase-locked-loop (PLL) is used to derive faster clocks, which consumes significant power. Following subsections analyze different aspects of testing WiNoC-based SoCs.

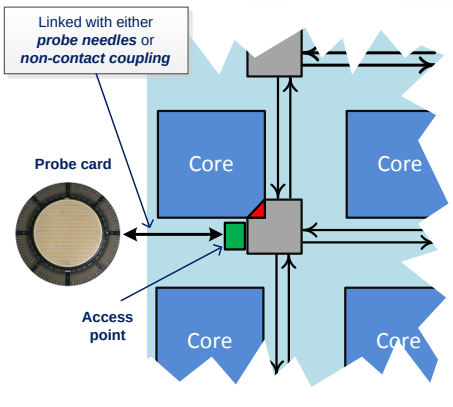

Figure 4: Interface between probe card and NoC

A. Alignment Margin

In direct contact wafer level testing, probe pins must be accurately aligned to touch I/O pads. The smaller size and pitch of probe needles reduce the misalignment margin, which demands more efforts to ensure proper contact with I/O pads. Since the WiNoC is suitable for dense SoCs, the size and the pitch of I/O pads can cause serious issues regarding alignment margin. Although, the conventional non-contact testing schemes offer wider alignment margin [19], the I/O pad size and the pitch may still be influenced by the size of transceivers and interference factor. Because the conventional non-contact testing schemes require one-to-one link between probe pins and DUT I/O pads, which restricts the density of dies per wafer. On the other hand, the developments in the on-chip radio communication cannot be exploited.

However, the suggested scheme requires a single RFC-based link per DUT, which significantly increases the misalignment margin.

B. Interference

Adjacent channel interference can be experienced by all type of couplings. However, the CC based links experience relatively low adjacent channel interference but it is only suitable for very short range communication like faced chips of stacked ICs [33] and IC testing [21], [34] but not for on-chip interconnection.

Despite the RFC-based link offers more advantages and improves with the technological advancements, it is not suitable for conventional non-contact testing methods due to the parallel interface by using multiple transceivers, where the interference is the major concern. In the suggested test framework, a single wireless link is required between probe card and DUT, which overwhelms the interference. Furthermore, the power probe needles may be used to shield the wireless nodes, which is not the scope of this paper.

However, interference may be observed while testing adjacent chips, which can be overcome by testing the chips in checkerboard pattern. Figure 5 shows a wafer with multiple dies. The on-probe wireless node is placed over the die in such a way that it could communication with all the wireless node of corresponding die. This also allows to set minimal transmission power, which also aids in reducing interference. Figure 5(a) shows the mapping of interference between adjacent wireless nodes. For example, the adjacent on-probe wireless nodes cause interference for each other, which is represented by red line and the green line represents a sufficient radio isolation between the nodes. Considering this mapping, the dies can be tested in checkerboard pattern, as shown in Figure 5(b) and (c). In this way, the test time doubles but the number of on-probe wireless nodes is halved, yet the density of dies per wafer is higher as compared to the conventional testing methods (refer sub section "Case Study for Scalability").

C. Time-Multiplexed Testing

TDM is an effective approach for better utilizing the communication channel bandwidth and it has been used to improve the utilization of tester channel bandwidth in few researches [31][35][36][37]. TDM approach can be used to test the embedded cores while exploiting high data rate wireless links. The number of time slots (n) can be given as:

$$n = \left\lfloor \frac{DR_{ATE\_DUT}}{DR_{CUT}} \right\rfloor$$

where DR_{ATE_DUT} represents the data rate between ATE and DUT through the probe card, and it is used for both the test data delivery and the test response collection. DR_{CUT} represents the data rate of a CUT. The floor function ensures that n is an integer. DR_{ATE_DUT} can be given as:

$$DR_{ATE\_DUT} = w_{ATE} \times DR_{ATE\_ch}$$

where w_{ATE} represents ATE channel width for a DUT and DR_{ATE_ch} represents the data rate per ATE channel.

DR_{CUT} can be calculated with the TAM width of CUT and the test frequency (f_T). We assume that the TAM width of a CUT

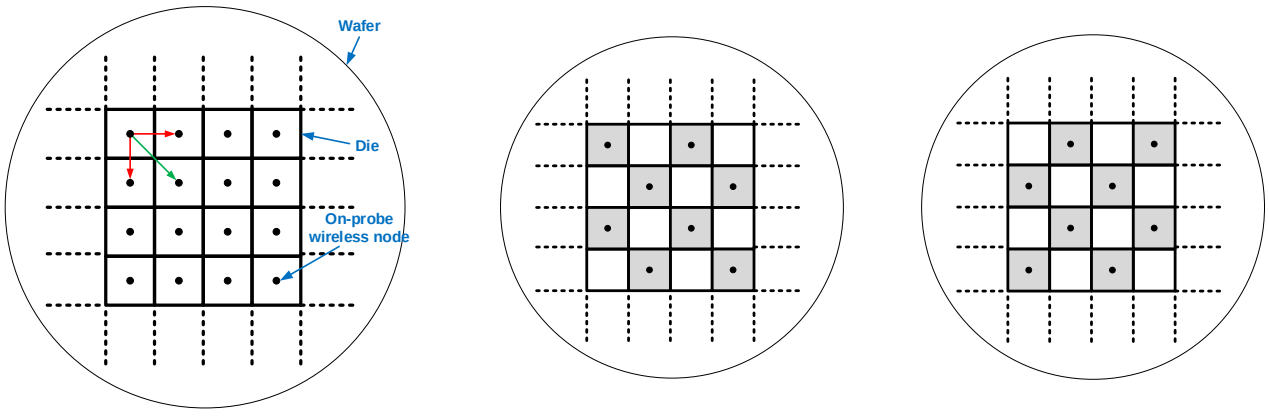

Figure 5: Wafer level testing (a) interference mapping (b) configuration 1 for testing (c) configuration 2 for testing

is twice the flit size (FS), half of that is used for test data-in and half for the test data-out.

$$DR_{CUT} = 2 \times FS \times f_T$$

Furthermore, DR_{ATE_DUT} can be distributed among $nodes_{WL}$ on-chip wireless nodes in time-division manner, i.e., $\frac{DR_{ATE\_DUT}}{nodes_{WL}}$. Therefore, through each wireless node, $\frac{n}{nodes_{WL}}$ cores can be tested.

Let us assume that $DR_{ATE\_DUT} = 20Gbps$, $FS = 16\ bits$ and $f_T = 100MHz$, which means $DR_{CUT} = 3.2Gbps$. The number of wireless node is $nodes_{WL} = 3$. With this arrangement, we can test $n = 6$ cores in time-division manner and through each wireless node, we can test 2 cores.

D. *Case Study for Scalability*

The trouble in further shrinking the size and pitch of the probe needles is a bottleneck in miniaturizing the IO pads. Thus, the capacity of the advanced testing equipment is underutilized. However, the proposed test method leverages the technological advancements and results in significant test cost reduction.

To observe the scalability, the following case is assumed. The probe card can accommodate 80000 probe needles and each die has 800 I/O pads. Both the probe needles and the I/O pads are distributed between the power and the functional contacts by 50%, i.e., 40000 (400) needles for power contact per wafer (die), and same for functional contacts. With the direct contact and conventional non-contact tests, the probe card can make contact with $\frac{40000}{400} = 100$ dies on the wafer.

Furthermore, we assume that the surface area of a probe needle is $4225\mu m^2$ ($65\mu m \times 65\mu m$), including the pitch [38][39], and it is same at all technology nodes. The area occupied by the probe pins on the probe card for a single DUT is:

$$(400 + 400) \times 0.00425mm^2 = 3.4mm^2$$

The area of wireless nodes processed with $90nm$, $65nm$ and $40nm$ technology are roughly estimated from [5], [17], [40], [41], see Table 1. However, the wireless node area with $20nm$ and $10nm$ technologies are approximated based on the fact that the device area ideally scales as $1/k^2$ (k is scaling factor) with downscaling of the process technology [42].

Table 1: Approx. area of a wireless node at different technology nodes

Process technology (*nm*)	90	65	40	20	10
Wireless node area (mm^2)	1.848	0.759	0.409	0.102	0.026

For the proposed method, 400 power pins and a wireless node is required for a DUT. With $65nm$ technology, the area of a wireless node is approximately $0.759mm^2$ [5], [41]. Therefore, the area occupied by power pins and a single wireless node on a probe card for a single DUT is:

$$(400 \times 0.00425mm^2) + 0.759mm^2 = 2.459mm^2$$

Now the total area occupied by total probe pins on a probe card is:

$$(40000 + 40000) \times 0.00425mm^2 = 340mm^2$$

That allows $\frac{340mm^2}{3.4mm^2} = 100$ dies on a wafer. However, in such probe area, $\frac{340mm^2}{2.459mm^2} = 138$ wireless nodes can be embedded.

The line chart in Figure 6 shows that the proposed non-contact test framework exponentially scales with the downscaling of technology, which allows increasing the density of dies per wafer. However, the density of dies per wafer is not affected due to the saturation in shrinking of probe needle size, regardless of the technology node.

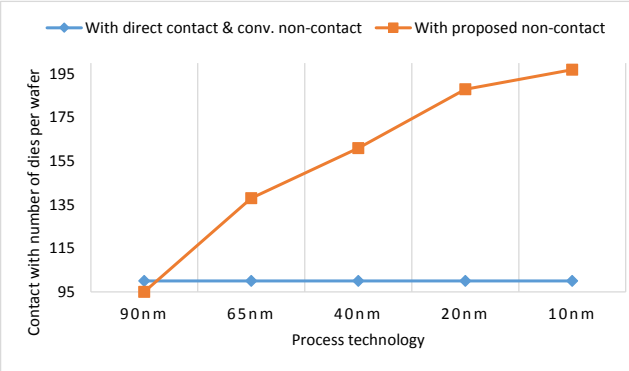

Figure 6: The number of allowed dies per wafer by direct contact and non-contact test methods with different process technologies.

Table 2 summarizes different aspects of all three types of testing methods. It is clear that the suggested method outperforms in all the mentioned fields.

Table 2: Summary of Test Techniques

Test technique	**Alignment margin**	**Probe needle cost**	**Boundary for number of time-slots**	**Test dedicated wireless nodes**
Direct contact with an access point	Narrow	High	Low	---
Conventional non-contact	Wide	Low	Low	Yes
Proposed non-contact	Wide	Low	High	No

CONCLUSION

A non-contact wafer-level test framework is proposed for WiNoC-based SoCs, which reuses on-chip wireless communication infrastructure. Discussions show that the proposed framework is a scalable solution and better utilizes the technological advancements compared to the conventional direct-contact and non-contact wafer-level testing methods.

FUTURE WORK

The future version of this work will include the development of the probe card for the proposed method, the extension for WiNoC with directional antennae and development of test cost function. Furthermore, it will include extensive experiments for demonstration.

REFERENCES

[1] M. Agrawal, M. Richter, and K. Chakrabarty, "A Dynamic Programming Solution for Optimizing Test Delivery in Multicore SOCs," in *Proc. of IEEE International Test Conference*, 2012, pp. 1–10.

[2] A. Ganguly, K. Chang, S. Deb, P. P. Pande, B. Belzer, and C. Teuscher, "Scalable Hybrid Wireless Network-on-Chip Architectures for Multicore Systems," *IEEE Trans. Comput.*, vol. 60, no. 10, pp. 1485–1502, 2011.

[3] S. Deb, K. Chang, X. Yu, S. P. Sah, M. Cosic, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Design of an Energy-Efficient CMOS-Compatible NoC Architecture with Millimeter-Wave Wireless Interconnects," *IEEE Trans. Comput.*, vol. 62, no. 12, pp. 2382–2396, 2013.

[4] K. Chang, S. Deb, A. Ganguly, X. Yu, S. P. Sah, P. P. Pande, B. Belzer, and D. Heo, "Performance Evaluation and Design Trade-Offs forWireless Network-on-Chip Architectures," *ACM J. Emerg. Technol. Comput. Syst.*, vol. 8, no. 3, pp. 1–25, Aug. 2012.

[5] S. Deb, A. Ganguly, P. P. Pande, B. Belzer, and D. Heo, "Wireless NoC as Interconnection Backbone for Multicore Chips : Promises and Challenges," *IEEE J. Emerg. Sel. Top. Circuits Syst.*, vol. 2, no. 2, pp. 228–239, 2012.

[6] W.-H. Hu, C. Wang, and N. Bagherzadeh, "Design and Analysis of a Mesh-based Wireless Network-on-Chip," in *Proc. 20th Euromicro International Conference on Parallel, Distributed and Network-based Processing*, 2012, pp. 483–490.

[7] L.-T. Wang, C.-W. Wu, and X. Wen, *VLSI Test Principles and Architectures: Design for Testability*. 2006.

[8] E. Alpaslan, Y. Huang, X. Lin, W. T. Cheng, and J. Dworak, "On Reducing Scan Shift Activity at RTL," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 29, no. 7, pp. 1110–1120, 2010.

[9] A. Sehgal, V. Iyengar, and K. Chakrabarty, "SOC Test Planning Using Virtual Test Access Architectures," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, no. 12, pp. 1263–1276, 2004.

[10] H. Vranken, I. C. Design, D. Design, and P. Holstlaan, "Enhanced Reduced Pin-Count Test for Full-Scan Design," *J. Electron. Test.*, vol. 18, pp. 129–143, 2002.

[11] K. Kempa, J. Rybczynski, Z. Huang, K. Gregorczyk, A. Vidan, B. Kimball, J. Carlson, G. Benham, Y. Wang, A. Herczynski, and Z. Ren, "Carbon Nanotubes as Optical Antennae," *Adv. Mater.*, vol. 19, no. 3, pp. 421–426, 2007.

[12] D. DiTomaso, A. Kodi, S. Kaya, and D. Matolak, "iWISE: Inter-Router Wireless Scalable Express Channels for Network-on-Chips (NoCs) Architecture," in *Proc. IEEE 19th Annual Symposium on High Performance Interconnects*, 2011, pp. 11–18.

[13] S. Bernard, D. Andreu, M.-L. Flottes, P. Cauvet, H. Fabrice, and F. Verjus, "Testing System-In-Package Wirelessly," *Proc. Int. Conf. Des. Test Integr. Syst. Nanoscale Technol. DTI*, pp. 1–5, 2007.

[14] S.-B. Lee, L. Zhang, J. Cong, S.-W. Tam, I. Pefkianakis, S. Lu, M. F. Chang, C. Guo, G. Reinman, C. Peng, and M. Naik, "A Scalable Micro Wireless Interconnect Structure for CMPs," in *Proc. ACM Annual International Conference on Mobile Computing and Networking*, 2009, pp. 20–25.

[15] A. Vidapalapati, V. Vijayakumaran, A. Ganguly, and A. Kwasinski, "NoC Architectures with Adaptive Code Division Multiple Access based Wireless Links," in *Proc. IEEE International Symposium on Circuits and Systems*, 2012, pp. 636–639.

[16] C. V Sellathamby, M. M. Reja, L. Fu, B. Bai, E. Reid, S. H. Slupsky, M. Igor, and K. Iniewski, "Non-Contact Wafer Probe Using Wireless Probe Cards," in *Proc. IEEE International Test Conference*, 2005, pp. 1–6.

[17] K. Kawasaki, Y. Akiyama, K. Komori, M. Uno, H. Takeuchi, T. Itagaki, Y. Hino, Y. Kawasaki, K. Ito, and A. Hajimiri, "A Millimeter-Wave Intra-Connect Solution," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2655–2666, Dec. 2010.

[18] B. Moore, M. Mangrum, C. Sellathamby, M. Reja, T. Weng, B. Bai, E. Reid, I. Filanovsky, and S. SLupsky, "Non-Contact Testing for SoC and RCP (SIPs) at

Advanced Nodes," in *Proc. IEEE International Test Conference*, 2008, pp. 1–10.

[19] M. Daito, Y. Nakata, S. Sasaki, H. Gomyo, H. Kusamitsu, Y. Komoto, M. Takamiya, and T. Sakurai, "Capacitively Coupled Non-Contact Probing Circuits for Membrane-based Wafer-Level Simultaneous Testing," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2386–2395, 2011.

[20] M. Scandiuzzo, S. Cani, L. Perugini, S. Spolzino, R. Canegallo, C. Gozzi, F. Maggioni, L. Perilli, R. Cardu, and E. Franchi, "Input/Output Pad for Direct Contact and Contactless Testing," in *Proc. 16th IEEE European Test Symposium*, 2011, pp. 135–140.

[21] M. Takamiya and T. Sakurai, "A 25-mV-Sensitivity 2-Gb/s Optimum-Logic-Threshold Capacitive-Coupling Receiver for Wireless Wafer Probing Systems," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 56, no. 9, pp. 709–713, Sep. 2009.

[22] N. Miura, Y. Kohama, Y. Sugimori, H. Ishikuro, T. Sakurai, and T. Kuroda, "A High-Speed Inductive-Coupling Link With Burst Transmission," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 947–955, Mar. 2009.

[23] Y. Yoshida, K. Nose, Y. Nakagawa, K. Noguchi, Y. Morita, M. Tago, M. Mizuno, and T. Kuroda, "An Inductive-Coupling DC Voltage Transceiver for Highly Parallel Wafer-Level Testing," *IEEE J. Solid-State Circuits*, vol. 45, no. 10, pp. 2057–2065, 2010.

[24] J.-J. Lin, H.-T. Wu, Y. Su, L. Gao, A. Sugavanam, J. E. Brewer, and K. O. Kenneth, "Communication Using Antennas Fabricated in Silicon Integrated Circuits," *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1678–1687, 2007.

[25] G. C. Trichopoulos, C. Caglayan, and K. Sertel, "Hybrid Electromagnetic Modeling of Non-Contact Probes for Terahertz Device Characterization," in *Computational Electromagnetics International Workshop*, 2013, pp. 52–53.

[26] P. Wettin, P. P. Pande, D. Heo, B. Belzer, S. Deb, and A. Ganguly, "Design Space Exploration for Reliable mm-Wave Wireless NoC Architectures," in *Proc. IEEE 24th International Conference on Application-Specific Systems, Architectures and Processors*, 2013, pp. 79–82.

[27] S. Deb, A. Ganguly, K. Chang, P. Pande, B. Belzer, and D. Heo, "Enhancing Performance of Network-on-Chip Architectures with Millimeter-Wave Wireless Interconnects," in *Proc. IEEE International Test Conference*, 2010, pp. 73–80.

[28] M. Richter and K. Chakrabarty, "Optimization of Test Pin-Count, Test Scheduling, and Test Access for NoC-Based Multicore SoCs," *IEEE Trans. Comput.*, vol. 63, no. 3, pp. 691–702, 2013.

[29] M. A. Ansari, J. Song, M. Kim, and S. Park, "Parallel Test Method for NoC-based SoCs," in *Proc. IEEE International SoC Design Conference*, 2009, pp. 116–119.

[30] J.-H. Ahn and S. Kang, "Test Scheduling of NoC-Based SoCs Using Multiple Test Clocks," *ETRI J.*, vol. 28, no. 4, pp. 475–485, Aug. 2006.

[31] C. Liu, V. Iyengar, J. Shi, and E. Cota, "Power-Aware Test Scheduling in Network-on-Chip Using Variable-Rate On-Chip Clocking," in *Proc. 23rd IEEE VLSI Test Symposium*, 2005, pp. 349–354.

[32] M. A. Ansari, D. Kim, J. Jung, and S. Park, "Hybrid Test Data Transportation Scheme for Advanced NoC-Based SoCs," *J. Semicond. Technol. Sci.*, vol. 15, no. 1, pp. 85–95, 2015.

[33] A. Fazzi, L. Magagni, M. Mirandola, B. Charlet, Lé. Di Cioccio, E. Jung, R. Canegallo, and R. Guerrieri, "3-D Capacitive Interconnections for Wafer-Level and Die-Level Assembly," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2270–2282, Oct. 2007.

[34] D. Y. Lee, D. D. Wentzloff, and J. P. Hayes, "Wireless Wafer-Level Testing of Integrated Circuits via Capacitively-Coupled Channels," in *Proc. 14th IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems*, 2011, pp. 99–104.

[35] J. M. Nolen and R. N. Mahapatra, "Time-Division-Multiplexed Test Delivery for NoC Systems," *IEEE Des. Test Comput.*, vol. 25, no. 1, pp. 44–51, 2008.

[36] F. Vartziotis, X. Kavousianos, K. Chakrabarty, A. Jain, and R. Parekhji, "Time-Division Multiplexing for Testing DVFS-based SoCs," *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 34, no. 4, pp. 668–681, 2015.

[37] M. A. Ansari, J. Jung, D. Kim, and S. Park, "Time-Multiplexed Test Access Architecture for Stacked Integrated Circuits," *IEICE Electron. Express*, vol. 13, no. 14, pp. 1–6, 2016.

[38] Microprobe, "Meeting the Economic and Technical Challenges of Wafer Test," 2010. [Online]. Available: http://www.formfactor.com/_site/wp-content/uploads/ctr_0384471.pdf.

[39] "Summary of CSE Company." [Online]. Available: http://www.proberworld.com/images/Company_Profile.pdf.

[40] J. Lee, Y. Huang, Y. Chen, H. Lu, and C. Chang, "A Low-Power Fully Integrated 60GHz Transceiver

System with OOK Modulation and On-Board Antenna Assembly," in *Proc. IEEE International Solid-State Circuits Conference*, 2009, pp. 316–318.

[41] D. Zhao and R. Wu, "Overlaid Mesh Topology Design and Deadlock Free Routing in Wireless Network-on-Chip," in *IEEE/ACM Sixth International Symposium on Networks-on-Chip*, 2012, pp. 27–34.

[42] R. H. Dennard, F. H. Gaensslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design of Ion-Implanted MOSFET'S with Very Small Physical Dimensions," *IEEE J. Solid-State Circuits*, vol. 9, no. 5, pp. 256–268, 1974.