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Self-Time Tracking Circuit to Improve Access Time of SRAM

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Abstract

We are entering in to a VLSI design era where few Pico seconds of memory access or cycle times will make a big impact on SOC designs performance. So, improving each Pico second of SRAM memory performance will lead to many design wins at the present competitive market. In SRAM memory design it's important to see that sufficient voltage differential is created by the time sense amplifier is turned on. If not, we need to delay the sense amplifier enable signal till sufficient voltage differential is created. This minimum sense amp differential voltage requirement varies with PVT corners. Assume in order to improve sense amp differential i.e., yield at fast process corner it may require to increase the voltage difference between bit line and bit line bar at sense turn on time. It will be achieved by delaying the sense amp enable signal by few Pico seconds. But, delaying sense amp enable signal at fast process corner by few Pico seconds will pushout sense amp enable signal even more at slow process corner thereby impacting the access time of the memory. In this paper we are presenting a self-time circuit method which will improve the yield at faster process corner at the same time it will not impact the memory access time at slow process corner.

Keywords: **s**elf-timing, sense amp enable, word line track, bit line track and PVT.

INTRODUCTION

As the technology is shrinking and we are entering into deep nanometer technologies the process variations results in write, read and retention failures in Static Random Access Memories (SRAM), and also impacts the yield. By using higher supply voltage and bigger transistors we can control these memory failures and can improve the yield. But it results in more power consumption and area overhead. [1].

The robustness of the self-time circuits in SRAM designs helps to decrease the failure rates and also consent to improve the yield and performance, decrease the power consumption. As the technology is shrinking, the RC parasitic delay is not varying much with process corners whereas the device delay variation is huge from fast (small delay) to slow (large delay) process corners [2]. In addition, word line and bit-line resistance is becoming a limiting factor in fast process corner. The gate delays in the self-timed path are less than the RC delays of the word line and bit lines in fast process corner. As a result, the word line pulse width is insufficient for the signals to attain full voltage levels, hence degrades the write margin and sense amplifier differential. In the bit line path design of SRAM will need larger margins because large delay develop across the PVT (process, voltage and temperature) conditions. So, it affects the more performance reduction and power consumption. A self-timed circuit techniques approach will solve the problem which is designed using replica bit line path, delay generators and also track the delays along the process, voltage and temperature conditions [3].

The SRAM can be accessed into two paths [4]: First one is the decode path, it is from the address lines to wordline and used the enable the memory cell to access the data. Another one is the data path, it is from the memory cells to data input and output ports and is used to write/read the data to/from the memory cells. During the SRAM cell read operation the enabling of the sense amplifier will play an important role. Power consumption in read operation will be reduced by enabling the sense amplifier when the required voltage sensitivity reached.

In the write operation, the closing of the wordline pulse will be the critical part. The closing of the wordline at the precise time will disconnect the SRAM cell from the bit line, then the action of the bit line and its energy consumption reduced. The sense amp enable and wordline closure is under the control of delay generators or pulse generators [3] is shown in the Figure 1. Delay chain based self-time control will introduce more variability. In order to reduce the variability we need to add more RC component in to the self-time path.

Normally, to hold the delay variations of the bit line swing to sense amp activation the pulse generator circuits required high margins [5]. Its effects the extra time to discharge the bit line from the connected SRAM cells or activation of the sense amp and wordline closure.

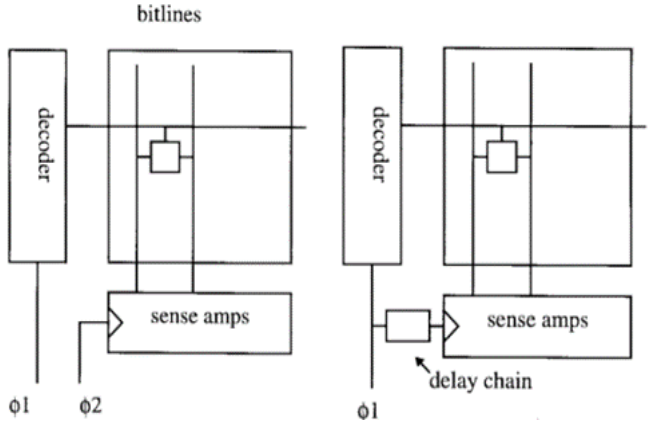

Figure 1: Circuit techniques for the generation of wordline and sense amplifier signal

This results can cause the more power and loss of speed. Hence, the optimum circuit technique is required to time close the wordline and sense amp enable. The bit line delay path is a function of RC components and depends on the no. of memory cells coupled to its [6]. To complete proper read operation, it needs a high margin in the bit line delay path. In order to activate the sense amp enable signal (SAE) using the delay chain circuit techniques, it must require that the delay of the bit line swing and inverter delay should match. Because of process corners, voltage and temperature conditions the delay of the bit line and inverter chain delay match failed. It cause the functionality loss of the memory [7]. This can be minimized by using the replica path delay technique.

The remaining sections are organized as follows. Section I: review the conventional self-time circuit methods. Section II: discusses the proposed replica bit line path circuit technique. Section III: presents the simulation results carried out using the Cadence virtuoso tool.

REVIEW OF PRIOR WORK

In conventional memory designs the self-timed word line and self-timed bit line paths will be designed such a way that the self-time path will work efficiently for the entire memory compiler range and at all the process corners. But, as the technology is shrinking the RC parasitic delay is not varying much with process corners whereas the device delay variation is large from fast to slow process corners.

The SRAM memories use a critical self-time signal to generate a sense amplifier enable signal and to close the wordline signal. Self-time technique helps in reducing the timing skew in data-sensing for synchronous SRAMs [8] across various process, voltage and temperature (PVT) conditions. This self-timing signal is generated in two ways. 1st method is by using inverter based logic delay inside the control block to adjust the sense amp enable timing and wordline closing time as shown in the Figure 1. Other method is by tracking the actual read and write paths using the self-timed world line and bit line (Figure 2) called replica paths [9]. This is the widely used technique in embedded SRAM memories for wordline pulse width control and sense amplifier enable triggering. The self-timed row/column based tracking method has fine grain control over the delay and tracks RC delay of actual read and write paths, but it is not area efficient. The inverter delay based approach is area efficient but it is not timing or performance efficient for smaller memories generated through a memory compiler.

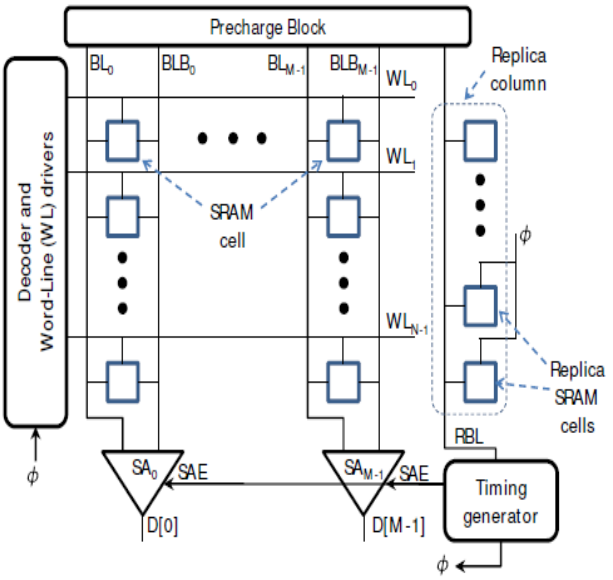

Figure 2: Self-time replica bit line control circuit

The replica bit line technique is more vigorous than the delay chain to the enable of sense amp of SRAMs and in closing the wordline at the required time. Due to the constricted tracking of the replica paths, the power and performance of the memory variants are minimized [10].

For a memory with minimum number of columns and maximum number of rows the bit line path delay is well tracked but the row replica path gate delay will be less at fast process corner due to less number of pass gate devices

connected to the wordline resulting in early sense amp triggering signal generation and early wordline closure. It will create functional/yield issues as sense enable signal is arriving before a sufficient voltage difference is created at sense amp nodes. Depending on sense amp differential voltage requirement we can delay the sense amp enable signal to get the correct functionality at fast process corner. But, delaying sense enable signal at fast corner will results in more delay in sense enable at slow corner thereby impacts the access time at slow process corner leading to memory performance degradation.

The self-time circuit which we are presenting in this paper will slow down the bit line discharge rate resulting in delayed sense enable signal generation at fast process corner for memory configurations with minimum number of columns. It will improve the functional yield. But, at the same time it will not affect the self-time bit line delay/discharge rate at slow corner; hence it will not affect the performance at slow corner and for larger memory configurations.

PROPOSED METHOD

The conventional replica path of row/column schemes generate a self-time signal which will be used in both read and write operations. The self-time signal will improve the performance and reduce the power consumption if properly tuned across the PVT conditions [11].

The proposed scheme offered an efficient self-time read and write bit line tracking circuit for memories to improve the functional yield at fast process corner without affecting the performance at slow corner and also without affecting the performance of the largest (having max. no. of rows & columns) memory configurations of the latest technology memory compiler designs. Especially for memory configurations of larger no. of rows and minimum no. of columns, self-timed tracking circuitry tends to time out too soon, causing the functional failures/yield loss due to inadequate word line pulse width during write and insufficient sense amplifier differential during read.

The conventional approach to improve the yield (of tall/narrow memory configurations at fast process) is to add additional delay to the self-timed tracking path. However, this negatively impacts the performance (due to delayed sense amp turn on time) at the critical slow process corner or at maximum array configurations. In latest technologies, for high speed memory designs, the conventional tracking system does not work as well across the memory compiler range. The presented scheme addresses both yield & performance issues as explained below.

The proposed self-time bit line control circuit solves the functional/yield problem at fast corner without impacting the performance at slow process corner and improves the tracking circuit for tall/narrow memory configurations without impact the performance for memories for larger memory configurations.

It has the following novel features:

1) an adaptive self-time bit line discharge rate control circuit technique which ensures the circuit functionality/yield/margin at fast process corner without impacting the circuit performance at other process corners;
2) no extra tracking bit lines or no extra tracking word lines are needed to implement the proposed scheme (small area impact);
3) this technique allows us to speed up the self-time circuitry in the slow process corner (without impacting the fast process corner);
4) improves the sense differential during read and write margin during write at fast process corner without impacting the performance at critical slow process corner;

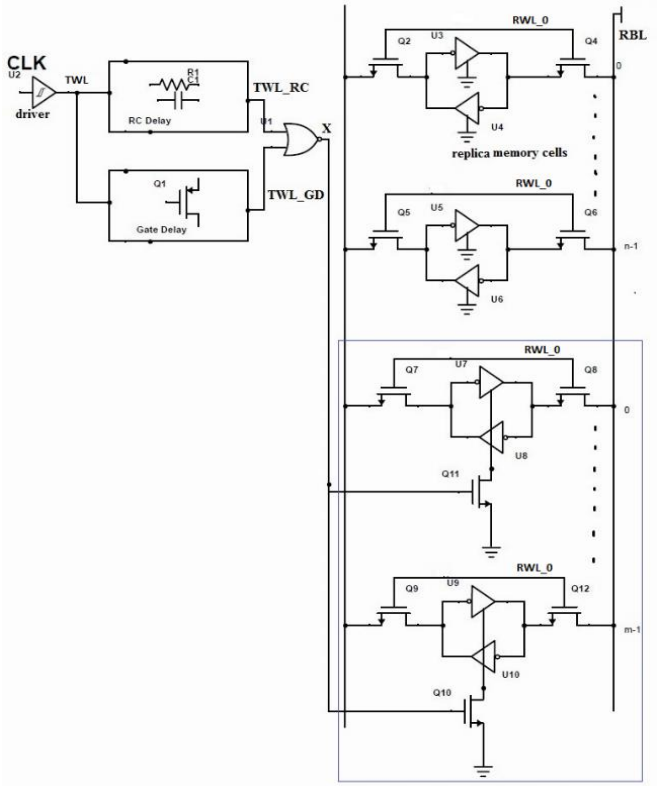

Figure 3: Proposed self-time circuit diagram

Circuit Description:

The circuit for the proposed method is shown in Figure 3. The tracking replica bit line (RBL) discharge rate has two components, i.e., fixed & variable discharge rates controlled by two groups of memory cells connected to it. The upper memory cells block connected to the tracking bit line (RBL)

will provide the fixed RBL discharge rate independent of the process corner. Whereas the bottom memory cells block connected to the tracking bit line (RBL) will vary the RBL discharge rate based on the process corner. The number of memory cells in each group will be decided based on the memory compiler range (no. of rows/columns) and the RBL discharge rate.

The tracking word line (TWL) near end signal along with internal clock (CLK) is used to generate a TWL_GD signal (Gate delay). TWL_GD is responsible for tracking word line device delay & TWL_RC is responsible for tracking RC delay. TWL_RC is an RC component which varies with length of the wordline and the metal layer in which wordline is routed. At the beginning of the read/write cycle, signals TWL_RC and TWL_GD will be at low (0) so the X node will be high (1) and ground path to the bottom of the bit cells shown in Figure 3 (blue colored box) is enabled. When the wordline (WL) goes high tracking bit line (RBL) starts discharging. If the process corner is fast, TWL_GD will go high quickly and make X low (before RBL fully discharge, depending on RBL RC parasitic) which will slow down the RBL discharge rate. Since RBL is used to gate the self-timed circuitry reset signal, the read and write margins will improve due to increased word line pulse width and additional read signal development time, resulting in yield improvement.

If process corner is slow and the array configuration is tall/narrow, TWL_RC goes high first than TWL_GD and make X low. But by that time X goes low, RBL has fully discharged and not impacting the sense amp turn on time during read and wordline closure during write operation. So, in this case there is no role of signal X. For the maximum array configuration and slow process corner, RBL discharges normally (prior to X is going low) without any additional delay and there will be no performance impact.

RESULTS AND DISCUSSION

The simulation waveform of self -timed control signal generation (X) at FF (Fast Fast) process corner is shown in the Figure 4. It shows that when the read/write cycle begins, signals TWL_RC and TWL_GD will be low (0) so the NOR gate output i.e. X node goes to high (1). When the wordline WL goes high tracking bit line (RBL) starts discharging. In the FF process corner, device delay is fast compare to RC delay, therefore, TWL_GD signal will goes to high quickly and made X signal low which will slow down the RBL discharge rate.

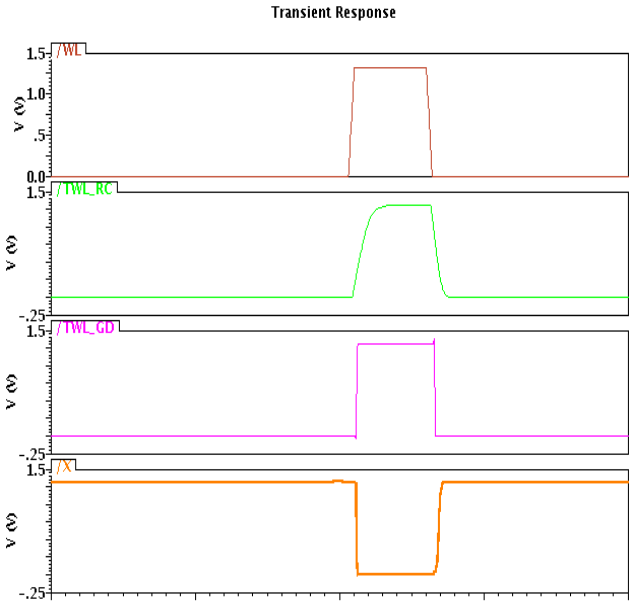

Figure 4: Self-time control signal (X) generation at FF/125ºC/1.32V

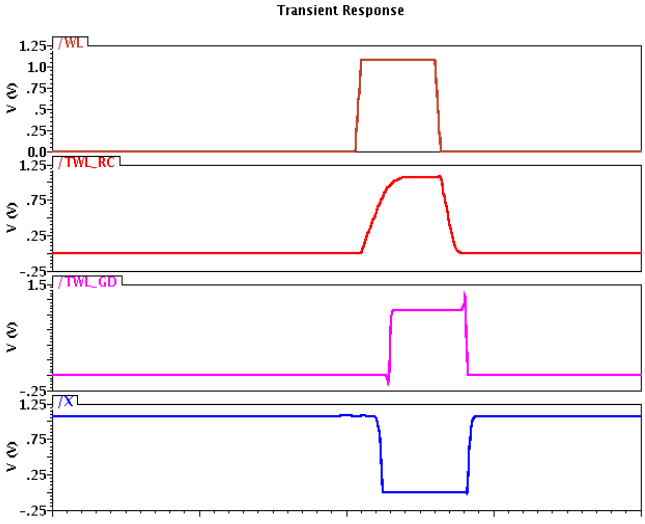

Figure 5: Self-time control signal (X) generation at SS/-40ºC/1.08V

Figure 5 shows that the simulation waveform of self-time control signal (X) generation at SS (Slow Slow) process corner. Initially the WL signal is low, so both TWL_RC and TWL_GD signals are also at low voltage levels and signal X being high. When the wordline WL goes high tracking bit line (RBL) starts discharging. In the SS process corner, TWL_RC signal will go to high first compared to TWL_GD and made X signal low (RBL fully discharged before X goes to low), which will not impact the RBL discharge rate.

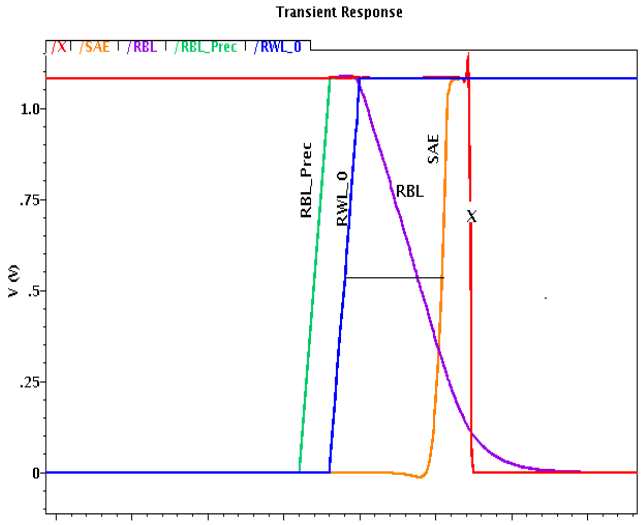

Figure 6: Generation of SAE signal at SS/-40ºC/1.08V

The activation of the sense amplifier at slow corner is shown in the Figure 6. Before the read operation begins the replica bit line (RBL) is at the pre-charge state (at VDD). When the replica wordline (RWL_0) is high, then RBL starts discharging and it will generate the sense enable signal (SAE). At slow process corner signal X is generated after the sense amp enable signal is generated. So, there will be no impact on sense enable timing or in wordline pulse width. So there will be no penalty in access time or performance.

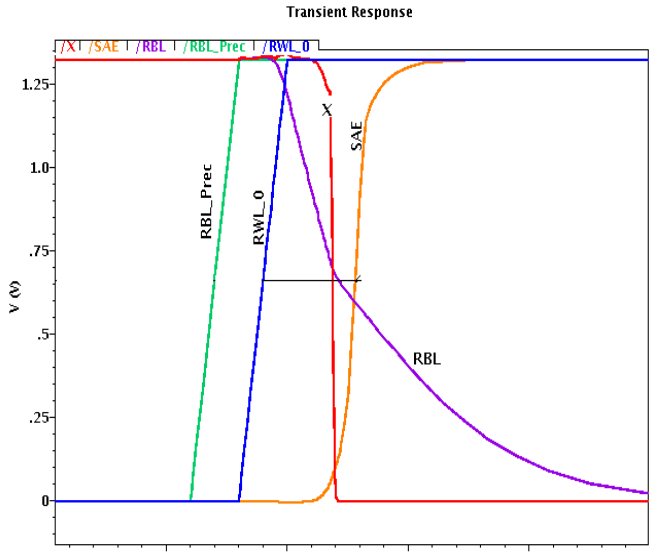

Figure 7: The delayed SAE signal generation at FF/125ºC/1.32V

In the fast corner the device delay variation is less compared to slow corner, consequently the SAE signal early turn on before getting the required differential voltage to enable SAE signal. This will impact the yield. At fast process corner signal X is generated before the sense amp enable signal is generated. Therefore, the proposed circuit scheme will provide 300ps delay in the RBL discharge rate. The delayed discharge rate of the RBL is depicted in the Figure 7. The self-timed bit line discharge rate control circuit technique increase the write word line pulse width during write & to delay the sense amp turn on time (SAE enable) during read at fast process corner to make successful write and read operations respectively, thereby to increase the chip yield.

CONCLUSION

This paper presented a circuit technique to improve the yield at fast process corner and to avoid the performance hit at slow process corner for taller memory configurations. At fast process corner the sense amplifier enable signal is delayed by 300ps which is not timing critical corner. But sense enable signal generation timing and wordline closure unchanged at timing critical slow process corner. So, the proposed self-time circuit scheme improves the yield at faster process corner for taller memories at the same time it will not impact the memory access time at slow process corner. This scheme will increase the wordline pulse width at fast process corner but it will not impact the wordline pulse width at slow process corner.

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