International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 23 (2017) pp. 13232-13238

A Low Power 4th order ΔΣ ADC using 6-bit SAR Type Quantizer

M. Appa Rao
Research Scholar, Department of Electronics and Communication Engineering,
Jawaharlal Nehru Technical University Ananthapur, Ananthapuramu, Andhra Pradesh, India.
Orcid Id: 0000-0003-2030-8689

Dr. P. Ramana Reddy
Professor, Department of Electronics and Communication Engineering,
Jawaharlal Nehru Technical University Ananthapur, Ananthapuramu, Andhra Pradesh, India.

Abstract

This paper presents a switched-capacitor fourth-order ΔΣ analog-to- digital converter (ADC) for sensing and audio applications. The proposed fourth-order modulator ΔΣ ADC with input-feed forward architecture is used to reduce the voltage swing of the integrators, which facilitates low-power amplifiers. By considering the characteristics of the modulator architecture, low-quiescent operational trans-conductance amplifiers are designed, which use positive feedback to increase dc gain. A novel and low power 6-bit asynchronous successive approximation register (SAR) type internal quantizer is used for power efficient design by incorporating the analog summer with the quantizer. Dynamic element matching (DEM) technique is applied with tree based algorithm to reduce the distortion resulted from the capacitor mismatch in the feedback digital-to-analog converter (DAC). The prototype ΔΣ ADC implemented in a 40nm CMOS process achieves 95.4 dB peak signal-to-noise ratio (SNR), 92.3 dB peak signal-to-noise and distortion ratio (SNDR) and 107.2 dB dynamic range (DR) for a signal bandwidth of 32 kHz while consuming 300uW at 0.9V supply voltage. The designed low voltage ΔΣ ADC modulator shows very high figure of merit with optimized performance.

Keywords: Delta-sigma modulator, dynamic element matching, feed-forward successive approximation analog-to-digital converter, low power, high figure of merit.

INTRODUCTION

In sensor and audio applications, the data converter with high resolution, high precision, low power consumption and wide bandwidth becomes more and more popular [1]. Recently, the proliferation of battery operated systems has demanded even more power-efficient circuits than ever. Low voltage delta-sigma modulators for ADC designs have been presented in various papers [2]-[6], and our work shows a 0.9-V design with only 300uW for the 107.2-dB dynamic range .However, a new process development has facilitate low-threshold voltage transistors for modulator design [7],[8], which reduce the need for charge pumps or switched-op amps. We used 40nm CMOS process, and this facilitates a simple circuit design, which in turn facilitates a more power-efficient modulator. We also exploit the advantage of the feed-forward modulator for low-power circuit design. Feed-forward modulator architecture has gained popularity recently because of the small voltages wings in the loop filter of the modulator. This allows further room for more efficient circuit design. The low-distortion feed-forward architecture, though, generally requires an analog adder in front of the quantizer. In case of single-bit or low-resolution internal quantizer, comparators integrated with passive type adder by using additional capacitors are typically used. However, as the resolution of the quantizer increased, number of required unit capacitor is exponentially increasing and therefore, active type adder with an additional op-amp becomes more competent even though it requires extra area and power utilization. In this paper, we will present a multi-bit feed-forward fourth order ΔΣ modulator and 6-bit SAR type internal quantizer. By combining the advantages of feed-forward architecture and the low-power operational trans-conductance amplifier (OTA), 6-bit SAR type quantizer the implemented ADC achieves very high figure-of-merit (FOM) among the state-of-the-art modulators.

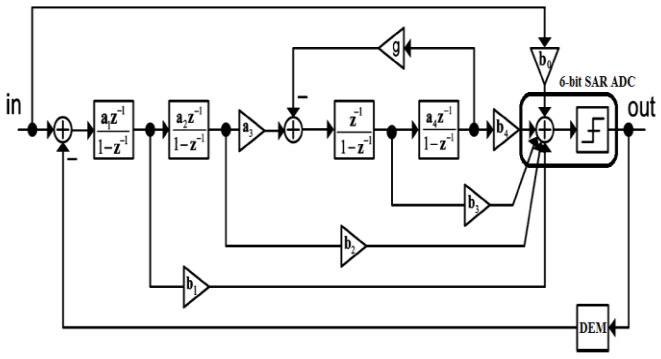

Figure 1: Block diagram of the proposed modulator

The organization of this paper is as follows. Section II describes the proposed fourth order ΔΣ modulator architecture. The circuit implementation of the modulator is discussed in Section III and Section IV describes the simulations results and overall conclusion is presented in Section V.

PROPOSED DESIGN ARCHITECTURE

The block diagram of the proposed design is illustrated in figure 1 and figure 2 illustrates proposed fourth -order feed-forward ΔΣ modulator with a 6-bit SAR type internal quantizer. The 6-bit SAR ADC incorporates the analog adder with the quantizer by using binary-weighted capacitor arrays, one comparator and SAR control logic. To avoid the use of high frequency clock for the SAR operation, the asynchronous control is exploited. Since the multi-bit quantizer is used, the DEM technique is employed in feedback DAC to reduce the distortion resulted from capacitor mismatch. Oversampling ratio (OSR) of 64 is chosen for a 32 kHz signal bandwidth. The overall output signal of the proposed modulator is given by

$$Y(Z) = U(Z) + \left(1 - \frac{1}{z}\right)^4 {}_{*}Q(z) \quad (1)$$

Where U (z) is the input signal and Q(z) is the quantization noise of the internal quantizer. In the proposed feed-forward architecture, the input signal of the first integrator is given by

$$E(Z) = \left(1 - \frac{1}{z}\right)^4 {}_{*}Q(z) \quad (2)$$

A 6-bit SAR type ADC which consists of a binary weighted capacitor array, a comparator and SAR control logic is employed for the internal quantizer. By lessening the number of comparators in comparison with the conventional flash type ADC, the recommended modulator reduces the area and power consumption. The analog adder in front of the quantizer is implemented by using the binary-weighted capacitor array of the SAR ADC to avoid the use of extra op-amp [9].In the ΔΣ modulator with multi-bit quantizer, distortion of the feedback DAC for the first integrator limits the overall linearity. To reduce the distortion resulted from the multi-bit DAC capacitor mismatch, a tree-structured DEM is employed [10].

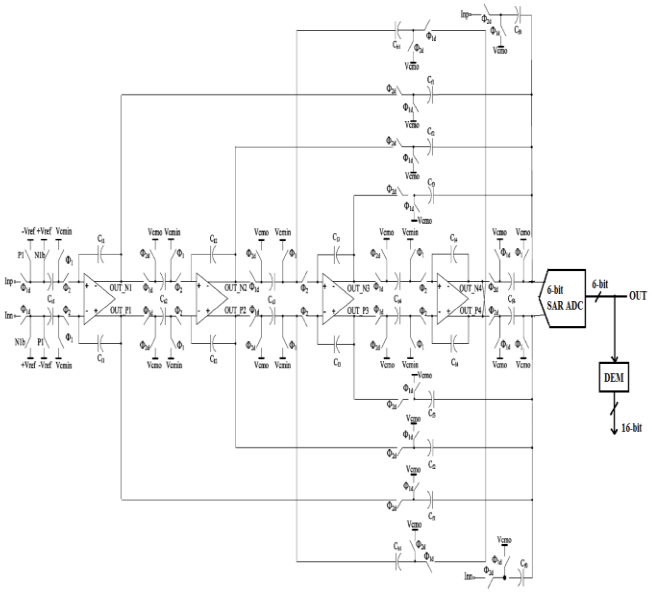

Figure 2: Switched-capacitor circuit implementation

PROPOSED DESIGN IMPLEMENTATION

A schematic diagram of the recommended switched-capacitor (SC) based ΔΣ ADC is shown in figure. 2. It consists of 4-th order modulator realized by switched capacitor based integrators, a 6-bit SAR type quantizer and DEM logic in feedback DAC. The key analog building blocks in the modulator are explained in this section. The 6-bit SAR type quantizer is explained first followed by OTA which are more critical block and other significant blocks are subsequently explained.

A. Low Power Operational Trans conductance Amplifier

The most critical part of the delta-sigma modulator is the operational trans-conductance amplifiers (OTAs). In particular, the first OTA has prevailing impact on modulator recital, hence, the first OTA consumes about half or sometimes more than half of the entire power. The class-AB circuit is known to be more power efficient; therefore, it is a widely used OTA architecture [11]. However, a drawback of the class-AB architecture is that it requires extra circuit to supply battery voltage to control the quiescent current of the pMOS and nMOS output transistors. Our design goal is to decrease power consumption; therefore, complex circuitry to implement a class-AB OTA is avoided. Another important design criteria in an OTA is the high-gain and wide bandwidth not only for the integrator settling but also for the high power supply rejection ratio (PSRR). The folded-Cascode amplifier is one of the most prevailing selections in delta-sigma modulators [12]. It achieves high-gain by transistor cascoding without multistage amplification. Due to its single-stage nature, the frequency compensation is achieved by a load capacitor in a switched-capacitor circuit. However transistor cascoding requires extra voltage headroom, and is usually avoided in low-voltage design. In our circuit design, which is shown in figure.3, we use a simple single-stage class-A architecture with local positive feedback [12], to increase amplifier gain and gain-bandwidth product (GBW).

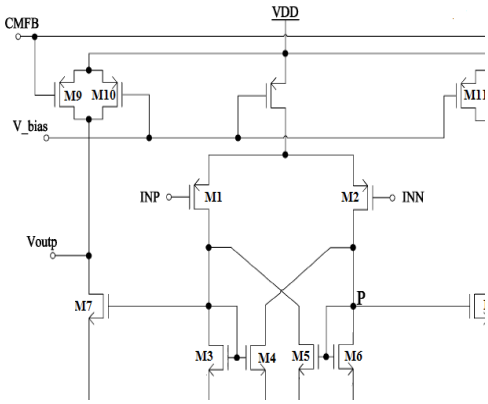

Figure 3.Schematic of the first OTA

Table I: Dimensions of the First Ota

Device Name	Device W/L (Dimensions)
M1, M2	*W/L=1.5u/2u, M=8*
M3-M6	*W/L=0.6u/2u, M=2*
M7, M8	*W/L=0.6u/2u, M=10*
M9, M11	*W/L=1.2u/2u, M=12*
M10, M12	*W/L=1.2u/2u, M=2*

Table I shows the dimensions of the designed OTA and Table II shows the simulation results of the designed OTAs. In order to evaluate the performance of the OTAs in the capacitive feedback configuration, the effective load capacitances, $C_{L,eff}$, are estimated. In our circuit configuration, the OTAs in the sampling phase, when Ø1 is high, have lower $C_{L,eff}$, which means that they will have a lower phase margin than in the integrating phase.

$$C_{L,eff} = C_L + (C_i * C_p)/(C_i + C_p) \quad (3)$$

Where CL is the load capacitance, Ci is the integrating capacitance, and Cpis the parasitic capacitance at the OTA input node. With the estimated effective load capacitance of 4 pF, the first OTA has 72-dB DC gain and 12-MHz GBW, which is sufficient for the designed modulator, as shown in Figure. 2. With the 4-pF load capacitor, the phase margin of the first OTA is obtained as 62ºC, which is sufficient for good stability. The other OTAs are relatively less critical than the first OTA; therefore, the current and performance are scaled down to reduce power consumption.

Table II: Dimensions of the First Ota

Parameters	OTA1	Other OTAs
Supply Voltage (V)	*0.9*	*0.9*
Static Supply Current (µA)	*40*	*30*
DC gain (dB)	*72*	*64*
Phase Margin (degree)	*62*	*69*
Load Capacitance ($C_{L,eff}$) (pF)	*4*	*1.2*
GBW (MHz)	*12*	*8*

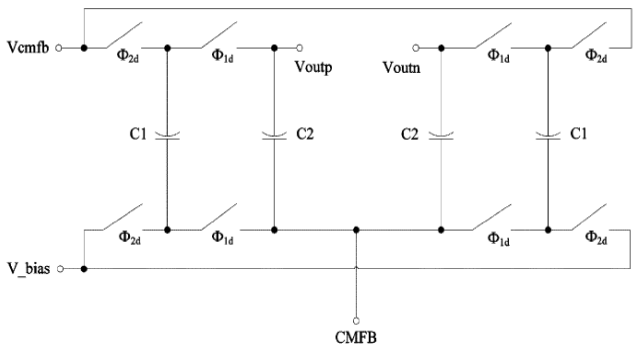

Figure 4: Schematic of the switched capacitor CMFB circuit

Figure-4 show the switched-capacitor common-mode feedback(SC-CMFB) circuit that is used for the fully-differential circuit implementation [13]. The CMFB circuit senses the output common-mode voltage and supplies the control voltage to balance the OTA's positive and negative outputs. The switches are implemented using nMOS transistors except for the two switches connected to the outputs of the OTA, which are implemented as CMOS switches to accommodate wider voltage swings. The capacitor values in this circuit are 0.1 pFand 0.4 pF for C1and C2, respectively.

B. Asynchronous 6-bit SAR ADC with summing operation:

Figure-5 show the schematic diagram of the recommended SAR ADC with adder. The operation of the recommended SAR ADC is as follows. During the sampling phase φ2, capacitors in the array are connected as shown in Fig. 6(a). The top plates of the capacitors are reset to the common-mode voltage VCMO while the bottom plates are connected to signals from input(VINP and VINN) and outputs of the each integrators (VOP1, VON1,VOP2 and VON2). During the next φ1 phase, the top plates are disconnected from VCMO and the bottom plates of the capacitors are switched to VCMO.

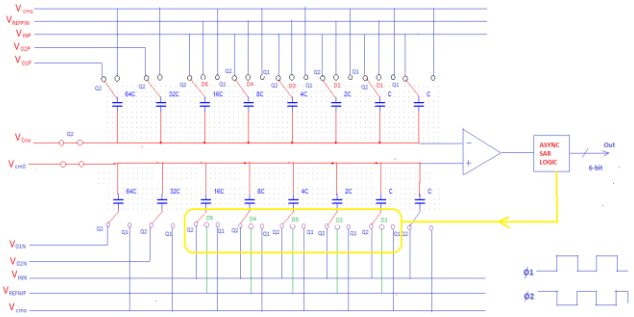

Figure 5: Proposed 6-bit SAR ADC with summing operation circuit implementation

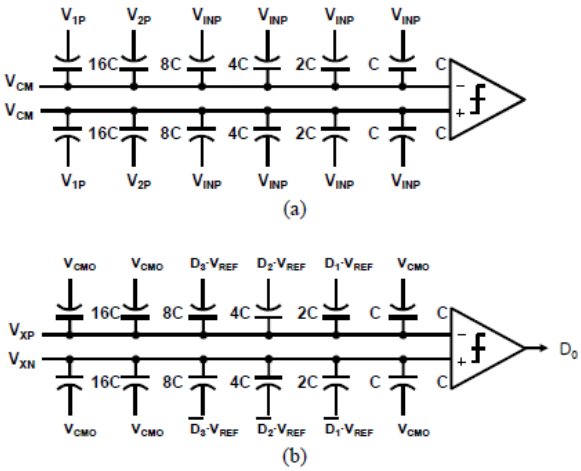

Figure 6: SAR ADC capacitor array; (a) during sampling, (b) when LSB is decided

Then a comparator decides most important bit (MSB) [14]. According to the MSB output, the bottom plates of the first 4C capacitors are switched to VREFP or VREFN. The operation is repeated until the less significant bit (LSB) is decided with binary weighted capacitors, 2C and C. Figure. 6(b) shows the comparator input signal after finishing the complete decision which is given by

$$V_+V=0.25*[(V_{IN}+2*V_{o1}+V_{o2})((1/2)*D_5+(1/4)*D_4+(1/8)*D_3 +(1/16)*D_2+(1/32)*D_1)*V_{REF}] \quad (4)$$

Where *VIN = VINP-VINN*, *VO1 = VOP1-VON1*,

VO2 = VOP2-VON.

The control signals of these operations are generated by asynchronous SAR logic to avoid the use of faster external clock.

C. Comparator :

Figure 7 demonstrates the design of the comparator used for SAR type ADC [12]. The design requisites of a 1-bit comparator can be relaxed in delta-sigma modulators since the non-idealities of the comparator also experience noise-shaping the same as the quantization noise. The operation of the comparator is described as follows, when the $Ø_{1d}$signal is low, two pMOS transistors pull up the *out p* and *out n* nodes, while the nMOS pull-down path is disconnected. At this timing, both output signals are high. When $Ø_{1d}$ signal goes high, two pMOS pull-up transistors turn off, and at the same time the two nMOS transistors turn on. Now the *out p* and *out n* nodes experience voltage drops from the power supply. The speed of the voltage drop is decided by the input voltage of the comparator. Because of the positive latch in the comparator, the regenerative process begins to speed up the comparator decision.

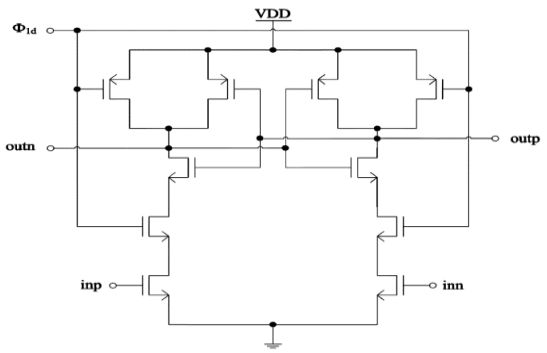

Figure 7: Schematic of the comparator circuit

D. Proposed ADC Circuit :

The complete modulator circuit is shown in figure. 2. It has four integrators with a 6-bit SAR type internal quantizer. The 6-bit SAR ADC incorporates the analog adder with the quantizer by using binary-weighted capacitor arrays, one comparator and SAR control logic. DEM technique is employed in feedback DAC to reduce the distortion resulted from capacitor mismatch. We have used two kinds of common-mode voltages. The input common-mode voltage is set to 0.25 V while the output common-mode voltage is set to the middle of the power supply voltage. The input common-mode voltage is lowered to give the OTA input differential pair ample voltage operating room. The capacitor value of the first integrator is chosen to satisfy the KT/C noise requirement as shown below [12]

$$C_s= 8KT\ (DR)\ /V_{DD}^2M \quad (5)$$

Where T is the absolute temperature, DR is the dynamic range, M is the oversampling ratio, and V_{DD} is used as the amplitude of a full-scale sinusoidal input. The oversampling ratio M is 64 in our design, and the DR is set to 107.2dB for a design margin. For the power supply of 0.9 V, the required capacitance is calculated as 3.6 pF. With the extra noise margin, the final sampling capacitance is selected as 4pF. The values of the modulator capacitors are calculated considering modulator coefficients. The third integrator has another input path, which is the local resonator with a coefficient value of only 1/36. In order to apply this small ratio, the size of the resonator capacitor is chosen to be 0.06 pF and the integrating capacitor as 2.16 pF. Then, the third sampling capacitor is decided as 0.96 pF for the integrator gain of 0.44. If we try to reduce the sampling capacitor further, the resonator capacitor becomes too small, so the sampling and integrating capacitors of the third integrator look larger than those of the second and the fourth integrators. Similarly we calculate all capacitors of the integrator by considering KT/C noise.

SIMULATION RESULTS

The recommended design 4-th order ΔΣ ADC with 6-bit SAR based quantizer is designed in 40nm standard CMOS technology, and occupies 0.312 mm2 active die area. The chip layout is shown in Figure.8, figure9shows the measured output spectrum for shorted input signal. 95.4dB peak SNR, 92.3dB peak SNDR and figure 10 shows measured 107.2dB dynamic range (DR) is achieved over 32-kHz signal bandwidth. The total power consumption is 300μW at 0.9V supply voltage. The measured performance is summarized in Table III.

The working of the designed ADC is compared with other lower supply designed modulators in Table IV. To contrast performances, the common FOM equation [15] is used, which is shown below.

$$FOM = DR_{dB} + 10\log\left(\frac{BW}{P}\right) \quad (6)$$

The presented ADC design modulator shows the highest FOM among the modulators. The high FOM can be explained by several reasons. The low-voltage swings of the modulator caused by the feed forward architecture make the OTA circuits very power-efficient. With very low output swing, low-

quiescent current OTA is designed without concern for slewing. Another reason comes from the simplicity of our circuit components. Our design does not include charge pumps, switched-op amps, or switched-RC-integrators, which may require extra control circuits and extra current.

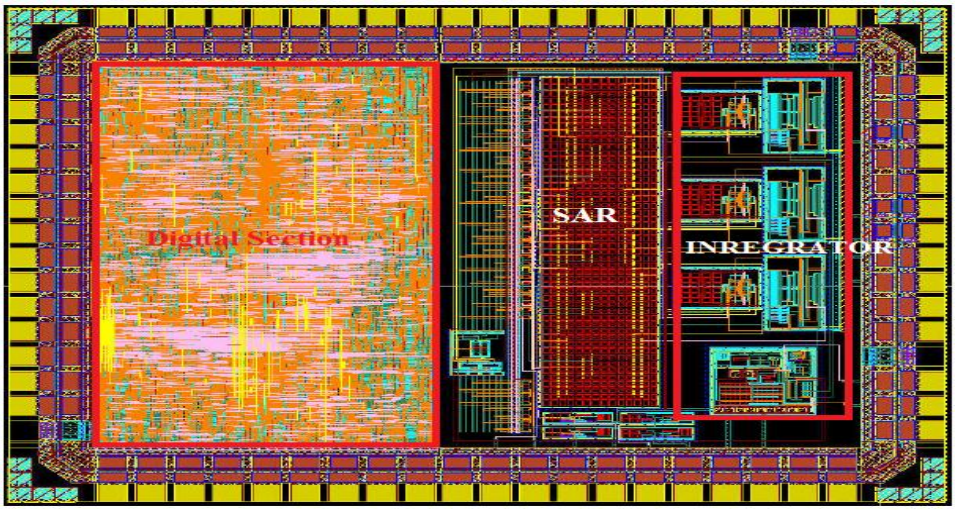

Figure 8: Recommended Design Chip Layout View

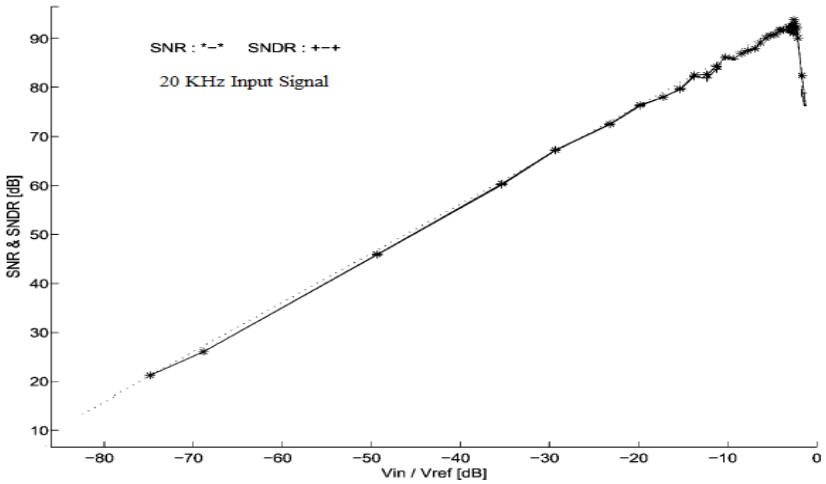

Figure 9: SNR and SNDR of the Proposed Design

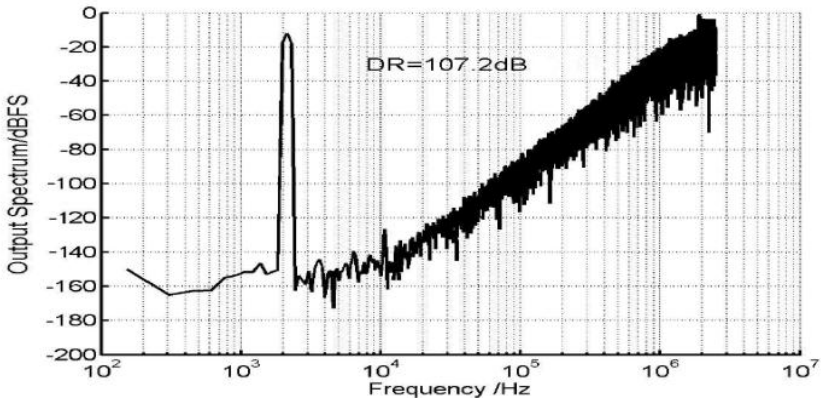

Figure 10: Dynamic Range (DR) of the Proposed Design

Table III: Measured Performance Summary

Technology	40nm CMOS Process
Power Supply	0.9V
Input Range	1.2 $V_{p\text{-}p,diff}$
Clock Frequency	12MHz
Oversampling Ratio	64
Signal Bandwidth	32 KHz
Dynamic Range	107.2 dB
Peak SNR	95.4 dB (@ Input=3KHz)
Peak SNDR	92.3 dB (@ Input=3KHz)
Power Consumption Modulator	180uW (Analog + Digital)
Figure of Merit (FOM) Modulator	172.49 @ 120dB (DR)
Power Consumption ADC	300uW (Analog + Digital)
Figure of Merit (FOM) ADC	157.48
Layout Active Area	0.312 mm^2

Table IV: Performance Comparison Of Low Voltage Delta-Sigma Modulators

Paper	Supply Voltage (v)	Process (nm)	DR (dB)	SNDR (dB)	BW (KHz)	Power (uW)	FOM
[2] (Peluso, 1998)	0.9	500	77	62	16	40	163
[3] (Sauerbrey, 2002)	0.7	180	75	67	8	80	155
[5] (Goes, 2006)	0.9	180	83	80	10	200	165
[6] (Pun, 2007)	0.5	180	76	74	25	300	155
[16] Won-Tak Choi Gil-Cho Ahn) 2014	1.1	45	81.8	76.8	5	850	---
[17] Xin Meng,Jinzhou Cao,Tao He) 2015	1.6	180	81.8	81.6	40	19200	165.2
This Work	0.9	40	107.2	92.3	32	300	172.49

CONCLUSION

A very low-power 4-th order ΔΣ ADC using 6-bit SAR type internal quantizer is implemented in a 40nm CMOS process. Input feed forward modulator architecture is used to reduce the voltage swings of the integrators. By reducing the integrator swings, more power-efficient OTA scan be used for low-power circuit design. An input feed-forward ΔΣ ADC using SAR type internal quantizer was realized. A 6-bit asynchronous SAR type quantizer incorporates analog adder without using extra op-amp and without increasing the clock frequency. Thus, this technique allows power and area reduction compare to conventional multi-bit feed-forward topology. The measured results validate the efficiency of the recommended design technique to achieve low-power and high-accuracy performance. The FOM comparison among the low voltage ΔΣ ADC modulators proves that the presented modulator has highly optimized performance.

REFERENCES

[1] J. C. Candy and G. C. Temes, Oversampling Delta-Sigma Data Converters: Theory, Design and Simulation. Piscataway, NJ: IEEE Press, 1992.

[2] V. Peluso, P. Vancorenland, A. M. Marques, M. S. J. Steyaert, andW. Sansen, "A 900-mV low-power ΔΣ A/D converter with 77-dBdynamic range," IEEE J. Solid-State Circuits, vol. 33, no. 12, pp.1887–1897, Dec. 1998.

[3] J. Sauerbrey, T. Tille, D. Schmitt-Landsiedel, and R. Thewes, "A0.7-V MOSFET-only switched-opamp ΔΣ modulator in standard digital CMOS technology," IEEE J. Solid-State Circuits, vol. 37, no.12, pp. 1662–1669, Dec. 2002.

[4] G.-C. Ahn, D.-Y. Chang, M. E. Brown, N. Ozaki, H. Youra, K. Yamamura,K. Hamashita, K. Takasuka, G. C. Temes, and U. Moon, "A0.6-V 82-dB delta-sigma audio ADC using switched-RC integrators,"IEEE J.

Solid-State Circuits, vol. 40, no. 12, pp. 2398–2407, Dec. 2005.

[5] J. Goes, B. Vaz, R. Monteiro, and N. Paulino, "A 0.9 V ΔΣ modulatorwith 80 dB SNDR and 83 dB DR using a single-phase technique," inIEEE ISSCC Dig. Tech. Papers, 2006, pp. 74–75.

[6] K.-P. Pun, S. Chatterjee, and P. R. Kinget, "A 0.5-V 74-dB SNDR25-kHz continuous-time delta-sigma modulator with a return-to-openDAC," IEEE J. Solid-State Circuits, vol. 42, no. 3, pp. 496–507, Mar.2007.

[7] M. Dessouky and A. Kaiser, "Very low-voltage digital-audioΔΣmodulatorwith 88-dB dynamic range using local switch bootstrapping,"IEEE J. Solid-State Circuits, vol. 36, no. 3, pp. 349–355, Mar. 2001.

[8] S. S. Bazarjani, M. Snelgrove, and T. MacElwee, "A 1 V switched-capacitorΔΣ modulator," in Proc. IEEE Symp. Low Power Electronics,Oct. 1995, pp. 70–71.

[9] L. Samid and Y. Manoli, "A Multibit Continuous Time Sigma DeltaModulator with Successive-Approximation Quantizer," in Proc. Int.Conf. Circuits and Systems, 2006, pp. 2965–2968.

[10] I. Galton, "Spectral shaping of circuit error in digital-to-analogconverters", Circuits and Systems II: Analog and digital signal processing, IEEE Transactions on, vol. 44, Issue 10, Oct. 1997, pp.808-817.

[11] L. Yao, M. Steyaert, and W. Sansen, "A 1-V 140- ..W 88-dB audiosigma-delta modulator in 90-nm CMOS," IEEE J. Solid-State Circuits,vol. 39, no. 11, pp. 1809–1818, Nov. 2004.

[12] R.Gregorian, Introduction to CMOS Op-Amps and Comparators.New York: Wiley, 1999.

[13] D. Senderowicz, S. F. Dreyer, J. H. Huggins, C. F. Rahim, and C.A. Laber, "A family of differential nMOS analog circuits for a PCMcodec filter chip," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp.1982–1023, Dec. 1982

[14] Chun-Cheng Liu, "A 10-bit 50-MS/s SAR ADC With a MonotonicCapacitor Switching Procedure*," Solid-State Circuits, IEEE Journal of*,vol. 45, Issue 4, April 2010, pp. 731-740.

[15] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*. Piscataway, NJ: *IEEE Press*, 2005

[16] Won-Tak Choi Gil-Cho Ahn , "A 1.1 V 81.8dB Delta-sigma ADC ,". *International journal of control and automation* vol.7, Issue 3, 2014, pp. 219-224.

[17] Xin Meng,Jinzhou Cao,Tao He, Yi Zhang and Gabor C. Temes "A 19.2-mW, 81.6-dB SNDR, 4-MHz Bandwidth Delta-Sigma Modulator With Shifted Loop Delays " *IEEE*, 2015, pp. 221-224.