International Journal of Applied Engineering Research ISSN 0973-4562 Volume 12, Number 24 (2017) pp. 14095-14100

The Differential Transimpedance Amplifier Design based 0.18 µm CMOS Technology

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Abstract

The transimpedance amplifier is recognized in a 0.18µm CMOS technology. The TIA applies a shunt-shunt feedback topology, differential TIA as it grasps a higher bandwidth rather than a conservative one. The TIA additionally has a variable gain to upsurge the bandwidth of the amplifier. The TIA has a concentrated gain of 70 dBΩ, bandwidth 3.1GHZ, bit rate 5Gb/s and input-referred current noise of 5 pA/√Hz. Eye jitter at bit rate 5Gb/sequal to 5ps (peak to peak)

Keywords: Preamplifier**,** Transimpedance amplifier , CMOS technology , Advanced design system

INTRODUCTION

Within an optical communication system, optoelectronic receiver, which entails of a photo detector and a transimpedance amplifier, is applied to transform the optical signals to electrical signals in the front end. Figure (1) indicates the system block illustration of optical fiber communication [1]. A tele- as well as data-communications are advanced promptly. Optic-fiber networks are extensively applied and the data speeds of the systems get higher over time. Consequently, ultra-high speed ICs for diverse systems is required. So far, still, almost all ICs at gigabit per second are made in GaAs and bipolar Silicon technologies with a higher expense. As the feature's size get reduced, CMOS technologies start to take an essential role in high performance in addition to high speed ICs. Currently, a feature size of 0.35-, 0.25-, along with 0.18-µm CMOS technologies are considered obtainable. The counterfeit unity present gain cut off frequency (f_T) of the above sub-micron CMOS technologies are 13.5-, 18.6-, and 49-GHz, correspondingly. Conventionally, a transistor could be wrought with a frequency of $f_T/10$. Accordingly, these submicron CMOS technologies could be applied in the ICs with upper frequencies of 1.35-, 1.86-, and 4.9-GHz, correspondingly. Moreover, 1-Hz frequency band could carry around 2 bit data, ensuing in the utmost bit rates of >2.5-, >3.5-, and ≈10 Gb/s for 3 sub-micron CMOS technologies [2].

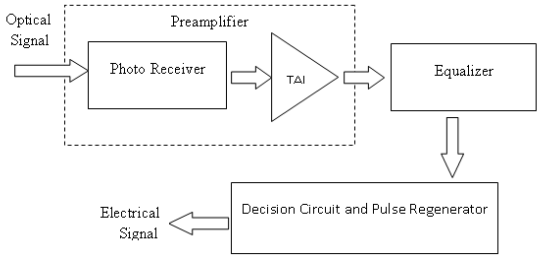


Figure 1: block diagram of optical fiber communication system

Further than the 4 amplifier forms, specifically voltage, transimpedance, transconductance, as well as current amplifiers [3]. In this research, a CMOS variable-gain fully difference Tran's impedance feedback amplifier is studied.

TRANSIMPEDANCE AMPLIFIER TOPOLOGIES:

The transimpedance amplifier alters the current created by the photodiode into an output voltage [4]. The design of this circuit includes several trade-offs among noise, bandwidth, gain, chip area and power dissipation. The simple topology of feedback transImpedance amplifier shown in figure (2), $V_{in} = V_{out}/-A$, where V_{in}, V_{out} are the input and output voltage of amplifier respectively and A the open loop voltage gain of core amplifier , we have

$$\frac{V_{out}/A}{R_{FB}} = -lin - (\frac{V_{out}}{A})C_{PD^S} \quad (1)$$

That is $$\frac{V_{out}}{I_{in}} = Z_T = -\frac{A}{1+A}\frac{R_{FB}}{1+\frac{R_{FB}C_{PD}}{1+A}s} \quad (2)$$

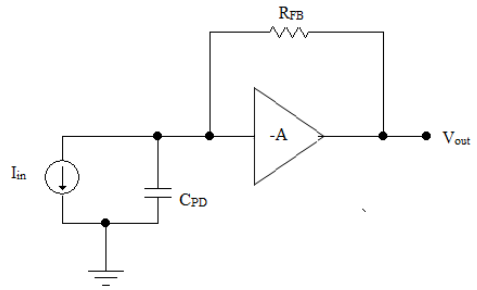


Figure 2: Feedback Transimpedance amplifier

Where I_{in} the input current of amplifier , C_{PD} is the capacitance of the photodiode , R_{FB} is the feedback resistance and Z_T is the transimedance gain . At low frequencies the transimpedance gain equal to :

$$Z_T = -\frac{A}{1+A} R_{FB} \tag{3}$$

Figure (3) indicates a diagram of the representative single-ended CMOS transimpedance preamplifier. The amplifier contains of a common-source stage and a source follower. The source follower isolates R_D from the loading effect of both R_{FB} and the input capacitance of the subsequent stage. In this study, the channel-length modulation and body outcome are deserted for simplicity. If the output impedance of the source follower ($1/g_{m2}$) ,is far less then, R_{FB} the open loop voltage gain of the amplifier is roughly equal to $g_{m1}R_D$ and the closed loop transimpedance gain is

$$Z_T = \frac{g_{m1} R_D}{1+g_{m1} R_D} R_{FB} \tag{4}$$

Where g_{m1}, g_{m2} are the transconductance of M_1 and M_2 correspondingly.

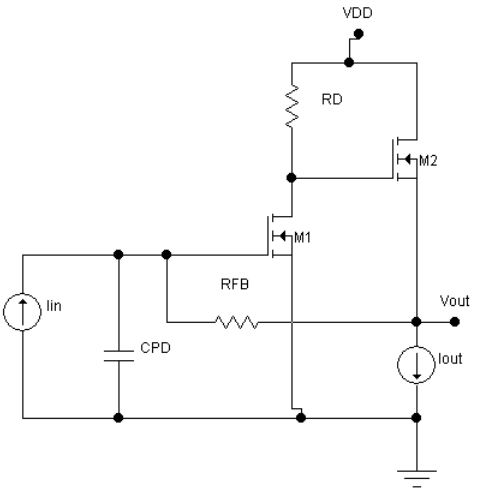


Figure 3: Single-ended CMOS feedback Transimpedance amplifier

From the principle of feedback system [4], the input of the feedback amplifier equal to:

$$R_{in} \approx \frac{R_{FB}}{1+A} \approx \frac{R_{FB}}{1+g_{m1} R_D} \tag{5}$$

While the output impedances at low frequencies is given by:

$$R_{out} \approx \frac{r_{dg2}}{1+A} \approx \frac{1/g_{m2}}{1+g_{m1} R_D} \tag{6}$$

In order to calculate the input-referred noise current of the TIA through the use of the topology of Figure (4). Observing M_1,R_D,and M_2 as the core voltage amplifier and neglecting channel length cadence and body, the output noise voltage as :

$$V^2_{n,out,core} = 4kTg_{m1}\gamma R^2_D + 4kTR_D + 4kT\frac{\gamma}{g_{m2}} \tag{7}$$

Where γ signifies the additional noise coefficient, equal to 2/3 for long channel devices and reaching as great as 2.5 in deep submicron technologies [5].

Where the last span signifies the gate-referred noise voltage of M_2.Dividing equation (7) by the square of the voltage gain yields the input-referred noise of the core:

$$\bar{V^2}_{n,in,core} = 4kT\frac{\gamma}{g_{m1}} + \frac{4kT}{g^2_{m1} R_D} + 4kT\frac{\gamma}{g_{m2} g^2_{m1} R^2_D} \tag{8}$$

The input noise current is

$$\bar{I^2}_{n,in} = \frac{4kT}{R_{fb}} + \frac{\bar{V^2}_{n,in,core}}{R^2_{fb}} \tag{9}$$

$$\bar{I^2}_{n,in} = \frac{4kT}{R_{fb}} + \frac{4kT}{R^2_{fb}}\left(\frac{\gamma}{g_{m1}} + \frac{1}{g^2_{m1}} + \frac{\gamma}{g_{m2} g^2_{m1} R^2_D}\right) \tag{10}$$

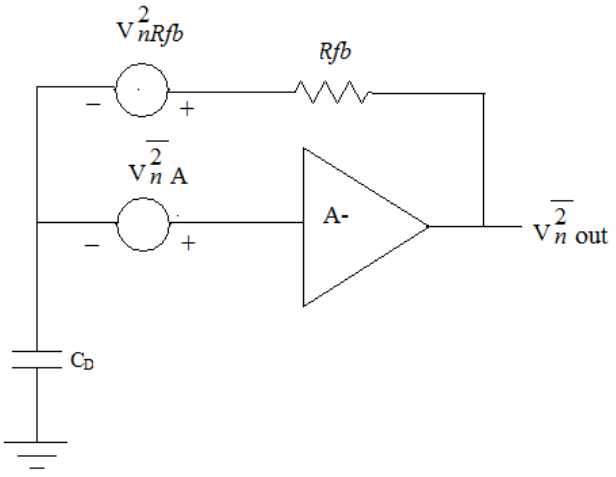


Figure 4: Show noise sources in feedback TIA

For a provided transimpedance gain, solitarily the noise donated by the core could be minimalizd This needs capitalizing on R_D and the Trans conductance of M_1 and M_2.

CIRCUIT DESIGN

Differential transimpedance amplifier: The scheme provided in this research is presented in Figure (5) through the use of double balanced photo diode and 3 stage differential transimpedance amplifier. The differential transimpedance amplifier is selected additionally due to its complementary results of the transimpedance amplifier stage which tolerates a differential interface to the following differential main amplifier stage, which is beneficial at great speed data rates. An additional significant benefit is that the differential configuration through the photo-receiver lessens the influence of bond wire inductance of ground and supply voltage by reducing concurrent switching currents. This is vital, as experience has indicated that single-ended amplifiers have a propensity to common-mode oscillation [6]. The circuit is intended to function at a bit-rate of 5-Gbit/s, while functioning from a supply voltage of 3.5 V. Figure (6) demonstrations the diagram of copiously differential transimpedance amplifier, The initial stage of the transimpedance amplifier is selected to be a completely differential mutual source with shunt feedback resistance and a resistive load. Its elementary purpose is to change the input current to an output voltage, while the second stage is a buffer stage with two-source follower granting isolation among the input and output of the amplifier, As for the third stage, It is an entirely differential output phase, This phase further rises the gain of the amplifier.

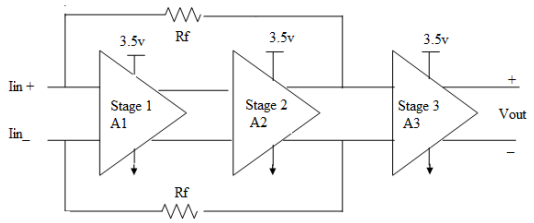


Figure 5: Circuit diagram of three stage transimpedance design with single power supply

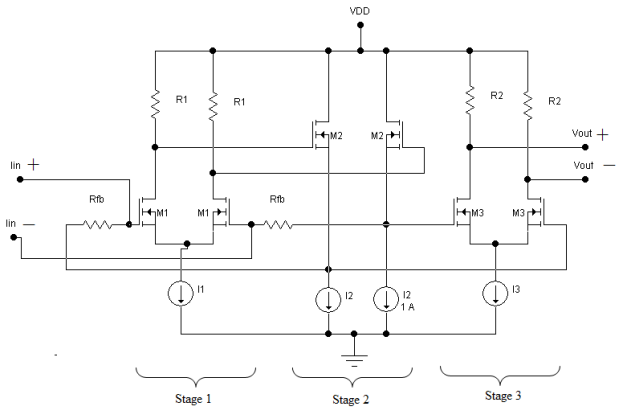


Figure 6: Differential transimpedance amplifier schematic

Variable Gain TIA: So as to evade drenching the amplifier while the high amplitude signal is being applied, the TIA is considered to have a variable gain. The gain, could be speckled by altering the rate of the feedback resistance, by employing a transistor PMOS type functioning in the linear mode in line with the feedback resistor R_{fB} as indicated in Figure (7). The channel of PMOS transistor linked to the input and source linked to the output. The bias voltage Vg is currently for instance base, when a signal is used, the source voltage of the transistor upsurges, therefore any alteration in Vds is reflected in an equivalent alteration in Vgs and the transistor would stay in linear region, even for bulky signals, consequently PMOS transistor is selected. In figure (7) when the gate voltage(Vg) of the transistor is augmented, the transistor is turned on and starts to conduct, dropping the value of the whole feedback resistance. On resistance of the transistor regulates the tuning range. The inclusive feedback value R_f is given by:

$$R_f = R_{fb} / R_{MRfb} \tag{11}$$

$$R_{MRfb} \cong \frac{1}{\mu_P C_{ox} (\frac{W}{L})_{MRfb} (|V_{gs}| - |V_T| - |V_{ds}|)} \tag{12}$$

Where μ_p mobility. C_{ox} is the oxide capacitance. V_T the threshold voltage. and $(\frac{W}{L})_{MRfb}$ the dimentions of the PMOS transistor .

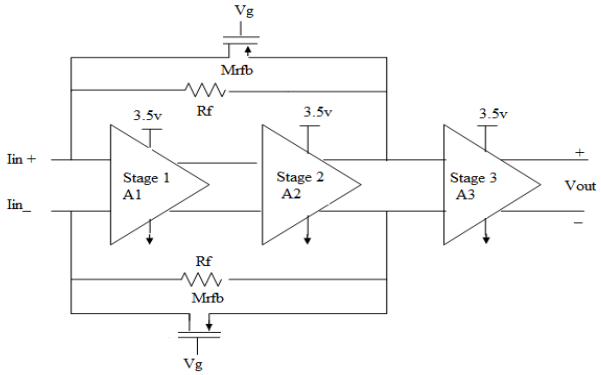
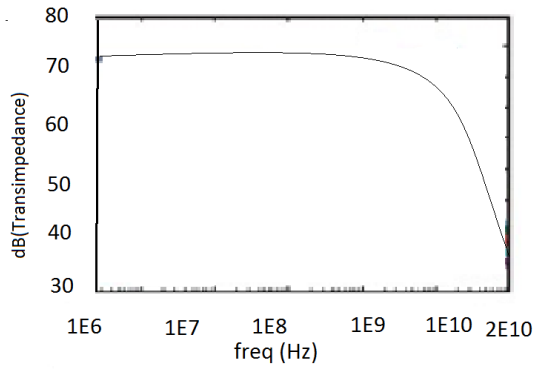
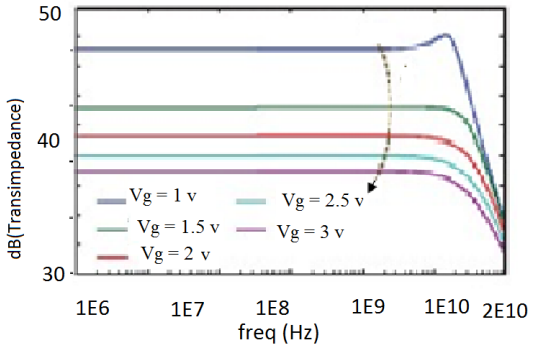


Figure 7: Implementation of Variable Gain TIA

Mockup Outcomes: The entirely differential transimpedance amplifier has been counterfeited through the use of BSIM 0.18 µm CMOS technology in ADS system. The frequency response of the closed-loop transimpedance feedback amplifier is indicated in figure (8). Figure (8) (a) indicates that the concentrated transimpedance gain is 73dbΩ with a bandwidth of 3.1 GHz and a bit rate of 5Gbps. When Vg voltage rises the transimpedance amplifier gain would drop and the bandwidth of the amplifier as indicated in figure(8) (b). This is for the reason that, the Vg voltage rises, the total resistance of the feedback network will drop. Figure (9) (a) demonstrates the average input referred noise current spectral density conforming to the concentrated gain is roughly 5 pA/√Hz, figure (9) (b) indicates that the Vg voltage is augmented, the input referred noise current will rise. This is due to the transistor M_{Rfb} is currently directing and contributing noise current that is directly referred to the input. Figure (10) indicates the stage response of transimpedance amplifier. Figure (11) (a), (b) and (c) show the simulation outcomes of eye diagrams at 2.5, 5 and 7 Gb/s, correspondingly. The data jitter is approximately 0 ps for 2.5 Gb/s, 2 ps (peak to peak) for 5 Gb/s and 8 ps (peak to peak) for 7 Gb/s.

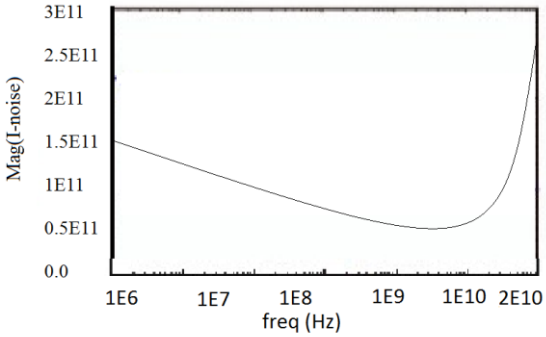


a)

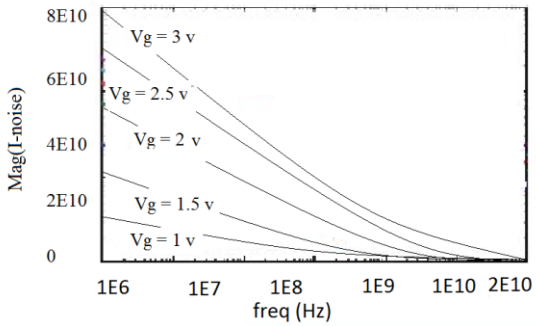


b)

Figure 8: Transimpedance amplifier gain (a) without variable gain(b) with variable gain (Vg is varied from 1 v to 3 v)



(a)



(b)

Figure 9: Input referred noise of Transimpedance amplifier (a) without variable gain (b) with variable gain (Vg is varied from 1 to 3 v)

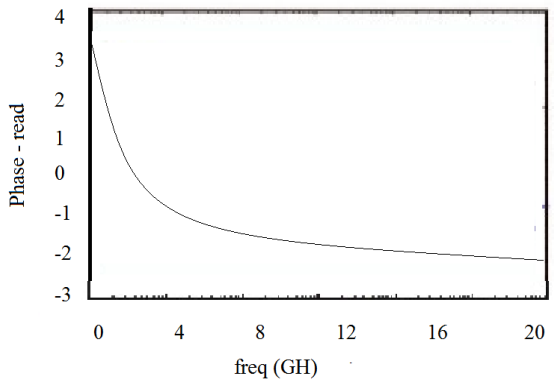


Figure 10: phase response of TIA

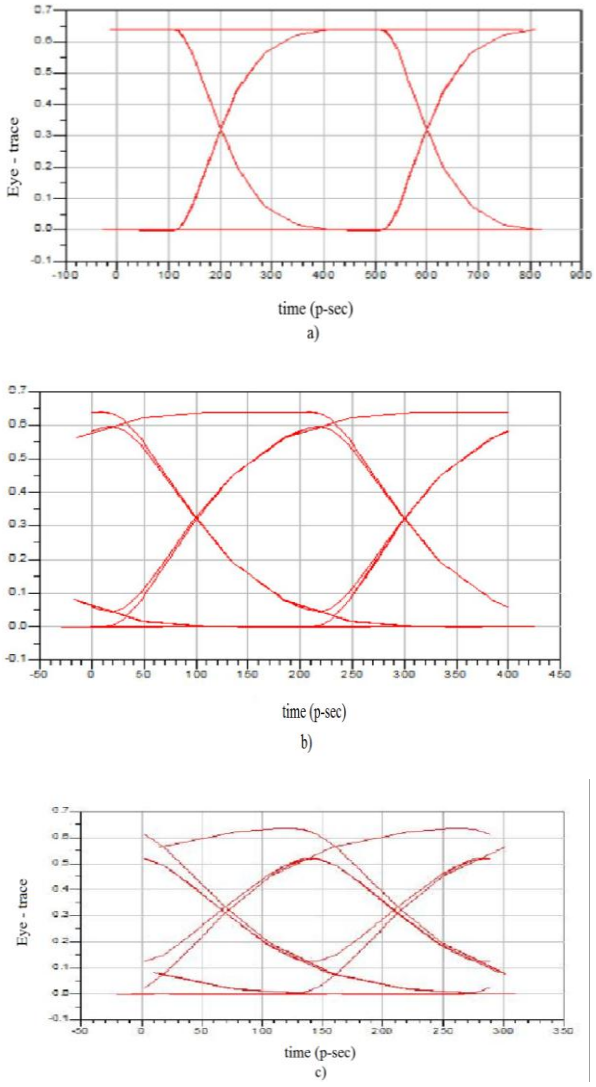


Figure 11: Eye diagrams of transimpedance amplifier for different data rates (a)2.5Gb/s (b) 5 Gb (c) 7 Gb/s

Table 1: Indicates the performance comparison 5Gb/s transimpedance amplifier in this research with some studies in the same data rate, Where attained in this research the gain higher than found in the [7], [8], and [9] references, and the noise in this paper less from the [8] reference.

Ref.	7	8	9	This work
CMOS technology	0.18 µm	0.18 µm	0.18 µm	0.18 µm
d.c gain (dBΩ)	66	58.7	55.75	70
Supply voltage (V)	1.7	1.7	1.7	3.5
Input Referred Nois	20	$13pA/\sqrt[2]{HZ}$	-------	$5pA/\sqrt[2]{HZ}$
Power dissipation	24mw	47mw	29.66mw	43.4mw

CONCLUSIONS

The differential TIA designed based on 0.18 µm CMOS technology through the use of RF large-signal model BSIM model in simulation , a maximum trans impedance gain of 73 dBΩ , trans impedance bandwidth of 3.1 GHZ and data rate 5Gb/s were attained. The average input referred noise current spectral density over the TIA bandwidth is 5 pA / √Hz . The TIA as well has a variable gain to increase the flexibility of the amplifier.

ACKNOWLEDGEMENT:

The authors are grateful to the Applied Science Private University, Amman, Jordan, for the full financial support grated to this research project

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