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The Design of Cascode, Shunt feedback Low Noise Amplifiers in 180nm Technology for WiMAX Applications

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Abstract

The proposed designed cascode common source, Shunt feedback LNA topology structures are a fully integrated at 5.9 GHz. The low noise, low power, high gain CMOS LNAS are designed for an WiMAX applications with TSMC 0.18µm RF CMOS process and are operated with a 1-V supply, the cascode LNA achieved the best performance with a simulated gain of 16dB and noise figure of 1.85dB. Similarly Shunt feedback LNA achieved forward gain of 20dB and noise figure of 2.34dB.The proposed structures has been simulated using cadence spectre RF.

Keywords: RF CMOS, VLSI Design, Low noise amplifier, Cascode , WiMAX, TSMC.

INTRODUCTION

The WiMAX is a new wireless wideband technology specified by IEEE 802.16e standards. Since last decade several CMOS LNA'S have been reported at 802,11/6,802.11/a and GSM. The network structures developed for existing internet is insufficient, such that so many developers are tried to improve this problem. The CMOS technology [1] is the best solution for low cost, for high integration processing and analog circuits to be mixed with [1] From fig (1), the low noise amplifier is one of the most crucial blocks in a receiver section of communication systems. Because of the sensitivity is mainly determined by the LNA performance with respect to mainly noise figure and gain.LNA is first stage of receiver such that it provides better input impedance matching. [1, 2]

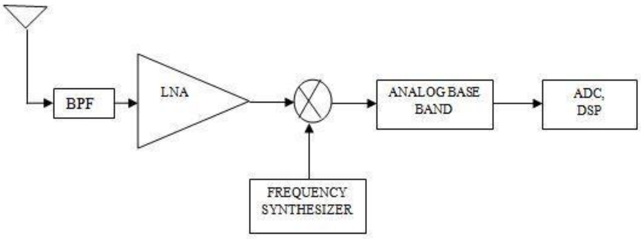

Figure.1: The basic receiver block diagram with LNA [1]

WiMAX is a communications technology which stands for Worldwide Interoperability for Microwave Access. It belongs to the IEEE 802.16 family of standards, which aim to provide wireless broadband access. There are two types of WiMAX systems: Fixed WiMAX and Mobile WiMAX. The fixed WiMAX system does not allow handoff between base stations. Mobile WiMAX on the other hand provides both mobile and fixed services. The WiMAX provide 75mbps data rate with coverage area 50km range by a metropolitan area network access scheme and also cope with NLOS(none line of sight) and LOS(line of sight) transmission conditions. It can also expand 3G, Cable modem, wired broad band access. [1, 2].

BASIC LNA REQUIREMENTS

1. Gain (10-20 dB) to amplify the received signal and to reduce the input referred noise of the subsequent stages.

2. Good linearity: Handling large undesired signals without much distortion.

3. Low noise for high sensitivity

4. Maximum power gain 50 Ω termination for proper operation and can route the LNA to the antenna which is located an unknown distance away without worrying about the length of the transmission line [1,7].

Basic Topologies

1. Wide band LNA input matching topologies (a) Resistive termination (b) Common gate (c) Resistive shunt feedback.

2. Narrow band LNA input matching topologies (a) Inductive degenerated (b) Resistive terminated [1, 7].

Cascode Common Source Amplifier

The most widely used topology for low noise amplifier design is the inductive source degeneration cascode common source amplifier show in the Fig.2 [5]. The cascode common source amplifier is also called as telescopic cascode amplifier because of the cascode transistor is the same type as the input transistor [6].

The cascode topology provide a higher gain, because of increase in the output impedance and it also gives a better isolation between the input and output ports. The higher reverse isolation provided by cascode common source amplifier [7].The suppression of the parasitic capacitances of the input transistor also improves the higher frequency operation of the amplifier, it can happen due to suppression of the parasitic capacitances of the input transistor.

Shunt Feedback Amplifier

The shunt feedback low noise amplifier is shown in the Fig. 3[5]. In order to achieve good linearity the shunt feedback topology is preferable. It provides a very good input and output matching for wide range of frequencies. The linearity of the amplifier improves the gain, which is achieved by feedback becomes less sensitive to the gain of the amplifier, resistors in series with a capacitor .The feedback element which are composed of a resistor in series with a capacitor, linearize the gain and increase the bandwidth of the amplifier. To increase the high frequency performance, an extra inductor can be placed in series with the capacitor and resistor [9].The feedback is also suited for the CMOS low noise amplifiers, since the input impedance of MOSFETs is large and mostly capacitive, which means that the input impedance can be controlled and set by the feedback. Finally, the high self resonance frequency of inductors to achieve a wideband, high impedance drain load by a post processing technique [1].

Circuit Design Procedure

The performance specifications requirement for a WiMAX receiver according to IEEE 802.16 is given in table.1.Similorly the table 2 represents the design requirements of LNA specifications.

Table 1: WiMAX receiver requirements and specifications

Parameter	**WiMAX specifications**
Radio Technology	MIMO-SOFDMA
Range	30 miles(50km)
Speed	70Mbps
Frequency range	2 to 64GHz
Receiver maximum input levelon channel reception tolerance	≥30dBm
Rx max. input level on-channeldamage tolerance	≥0dBm
2nd adjacent channel rejection	≥23dBm
1st adjacent channel rejection	≥4dBm
Noise Figure	≤7dB

Table 2: LNA requirements

Parameter	**Typical Values**
Technology	180nm
Frequency	5.9GHz
Power Dissipation	< 4 m W
Gain	> 20 dB
Noise Figure	<3 dB
Linearity	<-10dBm
Input and Output Matching	< -10dB
S_{11}	<-10dB
S_{12}	<-10dB
S_{22}	<-10dB

Calculation and analysis of LNAS

The LNA topologies were designed and analyzed in a standard 180 nm technology in CMOS process. The extraction of all device parameters, simulations was done using Virtuoso Schematic Composer and Spectre Simulator from Cadence Design System. The measurements in the plots were considered at 5.9 GHz. The LNAS were designed to operate at the frequency band of 5.725 GHz to 5.925 GHz [12].

Cascode Common Source Amplifier

In schematic of the designed cascode common source amplifier is shown in Fig. 2. The input impedance of the cascode common source low noise amplifier circuit will be capacitive due to the gate source capacitance Cgs. A lossless degenerating inductor Ls is added to the source of the cascode transistor M_1 to reduce the noise and improve the power gain in the circuit. The input impedance of the LNA can be computed based on (1) [4] with the value of source inductance Ls. The width of the cascode transistor M_2 was set equal to the width of the input transistor to take advantage of the reduced junction capacitance in the layout. The output matching network, composed of the drain inductor, L $_d$ and the output capacitors, C_1 and C_2, can be designed.

The final simulation design of the cascode common source LNA with device sizes and bias voltages shown in Fig. 2. [12]. From Figure.2 we can say that input impedance behaves like a series RLC circuit, due to the addition of L $_g$ in the

Circuit [5], [6].

$$Z_{in} = s(L_g + L_s) + \frac{1}{SC_{gs}} + \frac{g_m L_s}{C_{gs}} \qquad (1)$$

matching occurs when,

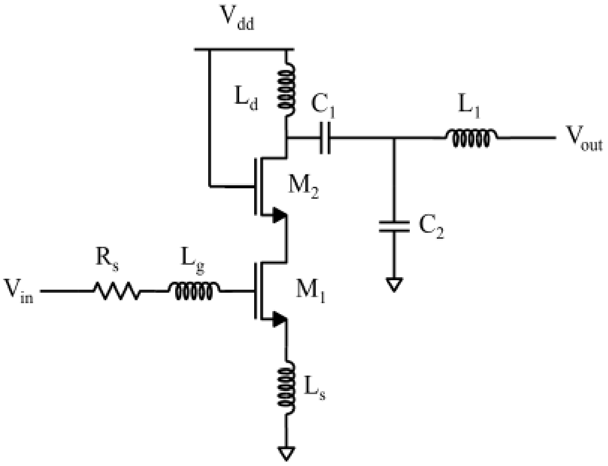

Figure 2: Inductive degenerated CS low noise amplifier

$$Z_{in}(j\omega_o) = R, \omega_o^2 = \frac{1}{(L_g + L_s)C_{gs}}, R_s = \frac{g_m L_s}{C_{gs}} = \omega_T L_s$$

L_s can be selected by: $L_S = \frac{R_s}{\omega_T}$ if this value is too small to be practical, a capacitor can be inserted in shunt with Cgs to artificially reduce ω_T [5, 6].

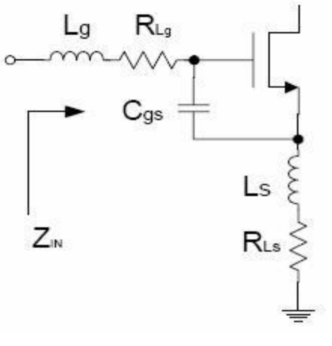

Figure 3: Non-idealizes of input impedance.

$$Z_{in} = s(L_g + L_s) + \frac{1}{SC_{gs}} + \omega_T L_s + \frac{1}{\frac{s}{\omega_T RL_s}} + R_{Lg} + RL_s + R_g + R_{gNQS}$$

Where

$$R_{gNQS} = \frac{1}{5g_m} \qquad (2)$$

$$R_S = \frac{R_{poly\,sh} w}{12N^2 L}$$

$$Z_{in}(j\omega_o) = \omega_T L_s + R_{Lg} + R_g + R_{Ls} + R_{gNQS} \qquad (3)$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s)\frac{1}{\omega_T RL_s} C_{gs}}} \qquad (4)$$

Inductance loss R $_{Lg}$: offset Z $_{in}$; R_{LS}: offset Z $_{in}$ and ω_0; Gate resistance R $_g$: offset Z $_{in}$; NQS gate resistance R g: NQS: offset Z in; Q-boosting [5][12].

Equivalent input network

From the source, the amplifier input (ignoring C_{gd}) is equivalent at resonance; the complete circuit is as in Fig.4 [5, 12].

Noise Analysis: From Fig.4, The output noise current due to R_s and R $_g$ is simply calculated by multiplying the voltage noise sources by g_m [4].

The calculation of output noise current due to drain noise is more involved, i_d^2 flows partly into the source of the device, and it activates the g_m, i_d^2 Output noise current [8].

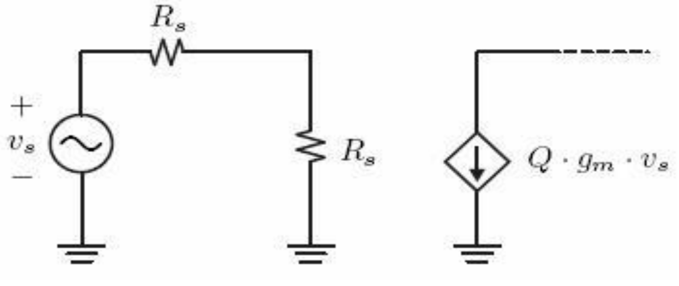

Figure 4: Complete circuit at Resonance

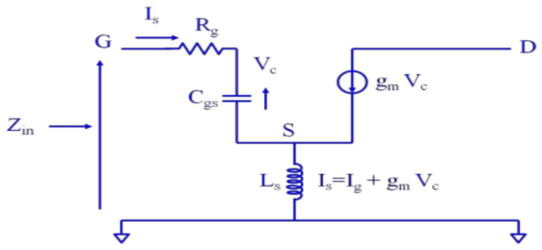

Figure 5: The source degeneration

Equivalent mode Input impedance

$$Z_{in}=\frac{V_g}{I_g}=\frac{I_g+V_c+j\omega I_s L_s}{I_g}\quad Z_{in}=\frac{L_s g_m}{C_{gs}} \qquad (5)$$

Where Z_{in} may be say 50ohms.

In most LNA designs the value of Ls is picked and the values of gm and C_{gs} are calculated to give the required Z_{in}.

Degeneration Inductor L_S

The value of this inductor is fairly arbitrary but is ultimately limited on the maximum size of inductance allowed by the technology.

$$\omega_T=\frac{g_m}{C_{g_s}}=\frac{R_s}{L_s}=\frac{50\Omega}{1nH}=50GHz \qquad (6)$$

Optimal Q of Inductor

The Optimal Q is given by the relation

$$Q_L=\sqrt{1+\frac{1}{p}} \qquad (7)$$

Where $p=\frac{\delta\alpha^2}{5\lambda}$

The parameters for p are dependent on the CMOS technology but typically α is assumed to be 0.8 -1 (take to be 0.9), δ is set between 2 - 3 (normally 2), λ is 2 - 3 times the value of δ (normally 4) by substituting these values

Where $p=\frac{2(0.9)^2}{5x4}\quad Q_L=\sqrt{1+\frac{1}{0.162}}=2.67$

Evaluation of L g

The relation to calculate the gate inductance is,

$$L_g=\frac{Q_L R_s}{\omega_o}-L_s \qquad (8)$$

Where ω_O = centre frequency

2π.5.9G = 3.7E10 rad/sec

$$Lg=\frac{2.67x50}{3.7e^{10}}-1nH=2.6nH$$

To Find Cgs (Gate-Source Capacitance)

The formulae is used for find gate to source capacitance is,

$$C_{gs}=\frac{1}{\omega_o^2(L_{gs}+L_s)} \qquad (9)$$

$$C_{gs}=\frac{1}{(3.7E^{10})^2(2.6nH+1nH)}=0.205pF$$

To Find Width of transistor

The width of the transistor is calculated by the,

$$w=\frac{3C_{gs}}{2C_{ox}L_{\min}} \qquad (10)$$

$$=\frac{3x0.0205pF}{2x3.419E^{-2}x0.6E^{-0.6}}=158.7\mu m$$

L min = $0.6E^{-0.6}$m; T ox = 1.01 $E^{-0.8}$m

ε ox = ε ox ε o

Where ε s = dielectric constant for silicon = 3.9 and

ε o = dielectric constant for free space = 8.854^{-14}F/cm

$$\text{Cox}=\frac{\varepsilon_{ox}}{T_{ox}}=\frac{3.9x8.854E^{-14}}{1.01E^{-6}}=3.419E^{-3}\ \text{pF}/\mu\text{m}^2 \qquad (11)$$

To Calculate g_m ;

The transconductance of the transistor is $g_m=\omega_T c_{gs}$

= 50GHz x 0.205pF = 0.01025A/V (12)

To find V Effective

$$\text{Veff}=(\text{Vgs-VT})=\frac{g_m L_m}{\mu_n c_{ox} w} \qquad (13)$$

μ_n = device mobility = 433cm/V

$$V_{eff}= \frac{0.01025x0.6E^{-6}}{433x3.419E^{-3}pF/\mu m^2x158.7\mu m}$$

$V_{eff} = 0.25\mu V$

$V_T = 0.7v$

$$V_{eff} = (V_{gs} - V_T) \qquad (14)$$

$$V_{gs} = V_{eff} + V_T \qquad (15)$$

$V_{gs} = 0.25 + 0.7$

$V_{gs} = 0.95V$ ~ 1V to the gate

Bias Current I_D

It is defined as the following

$$I_D = g_m.V_{eff} = 0.01025A/V \text{ x } 0.25V = 2.565mA \qquad (16)$$

Estimated Optimum Noise Figure NF_{op}

$$1+\frac{2\gamma}{\alpha}(\frac{\omega_o}{\omega_T})\ (\sqrt{p}\ |c|\ \sqrt{p}\ \sqrt{(1+p)})\,) \qquad (17)$$

$|c| = 0.4$

$$NF_{opts} = 1+\frac{4}{0.9}(\frac{3.7E^{10}}{50G})\sqrt{0.16}|0.4|\sqrt{0.16}\sqrt{1+0.16}$$

$NF_{opt} = 4.2 = 10 \log (4.2) = 6.3dB$

Shunt Feedback Amplifier

The design of shunt feedback low noise amplifier is shown in Fig. 6, the value of the feedback resistor which sets the power gain is given in (2) [4], where R_f, Z_o, and S_{21} are the values of the feedback resistor, output impedance, and the transducer gain.

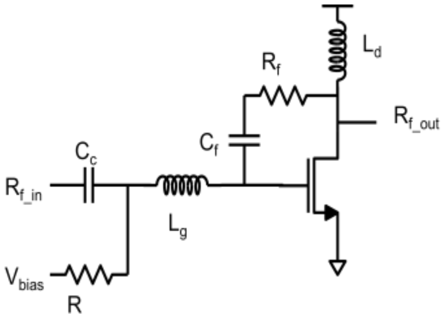

Figure 6: Schematic of shunt feedback amplifier

A small inductor was placed in the gate of the transistor to aid input matching. To tune out the junction capacitances in the drain of the transistor a load inductor was placed in the drain of the transistor. The value of the feedback capacitor, which is used for biasing purposes, was set large enough to not have a significant effect on feedback [12].

$$R_f = Z_o(1+|S_{21}|). \qquad (18)$$

The feedback resistance value is varied the parameters Noise figure minimum, maximum gain (g_{max}) and Parameter (S_{11}), (S22) of the feedback amplifier is changed as shown is table below [1].

Table 3: Feedback resistance versus variation in parameters.

Feedback Resistance	Gmax	NFmin	Input/output Return loss(max)	
500Ω	10.5	3.6	-14.2	-14.6
600Ω	11.1	3.5	-12.7	-12.6
700Ω	11.6	3.4	-11.5	-10.8
800Ω	12	3.3	10.7	-9.6

Layouts of Cascode and Shunt feedback LNAS.

The Schematic and layout design of cascode common source LNA [11] and shunt feedback LNA shown in fig .7, 8,9,10.

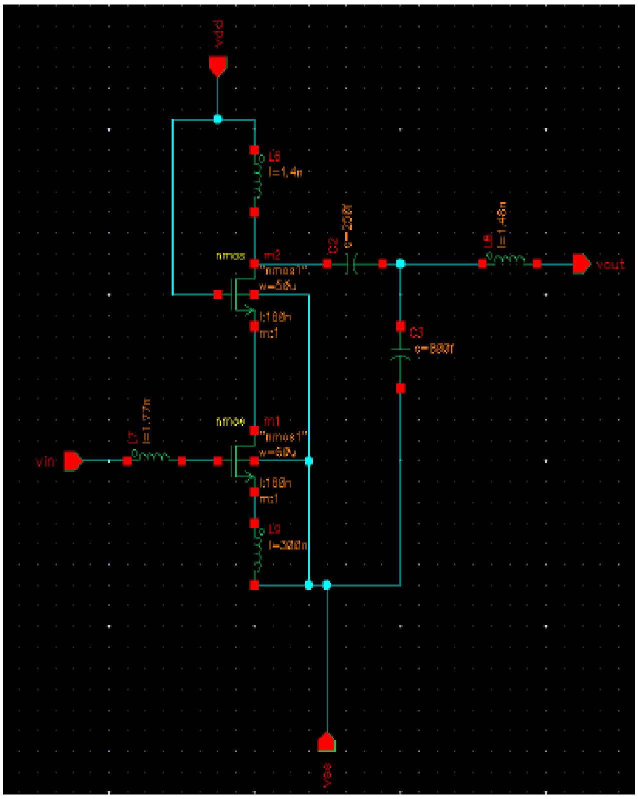

Figure 7: Schematic design of cascode common source LNA.

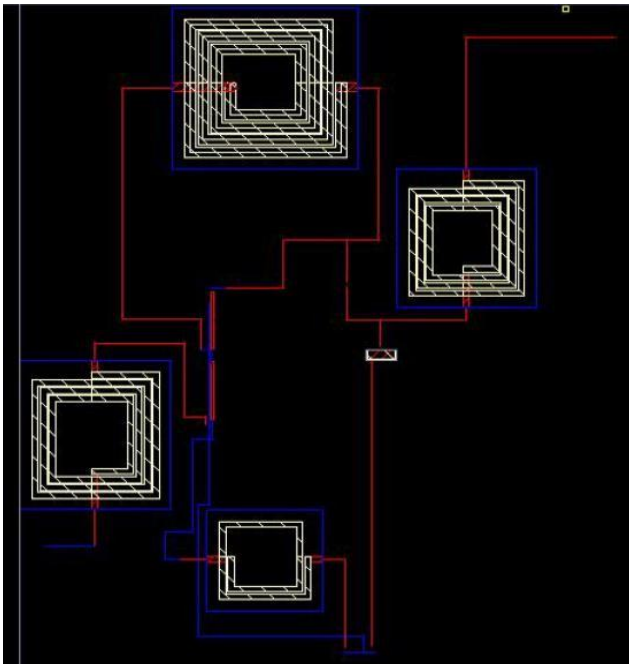

Figure 8: Layout of cascode common source LNA

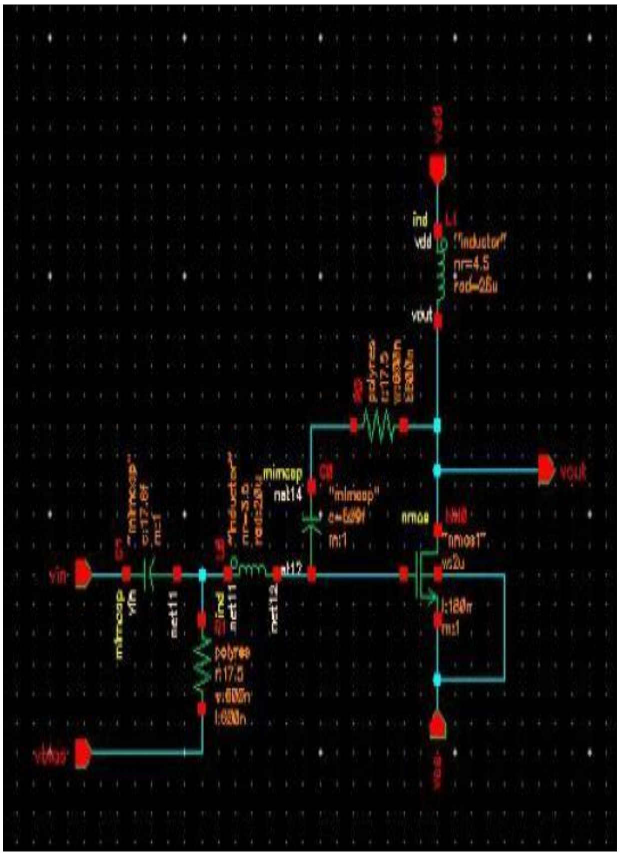

Figure 9: Simulation design of shunt feedback LNA setup to analyze

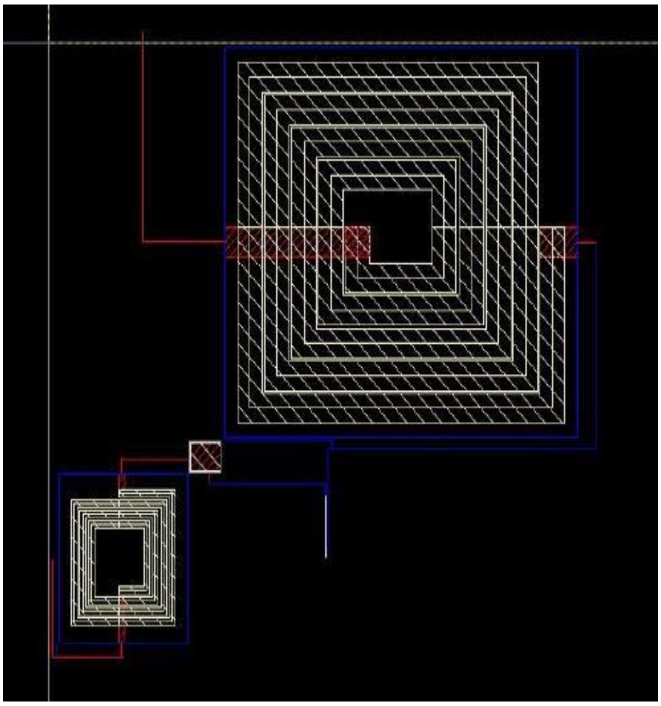

Figure 10: Shunt feedback LNA Layout.

SIMULATION RESULTS

Forward Gain (S_{21})

The shunt feedback amplifier achieved highest gain with 20 dB and the cascode common source amplifier achieved gain with 15.7 dB at 5.9 GHz. In order to compensate noise contribution of next stages in the receiver chain, it should have a LNA with power gain (S_{21}) more than 15 dB. And also can be shown on the plot of the power gain, the shunt feedback amplifier has provide a relatively wideband characteristic compared to the cascode amplifiers. The linearization effect of feedback gives the shunt feedback LNA its wideband characteristics compared to the narrowband characteristics of the cascode common source LNA is shown in Fig. 11.

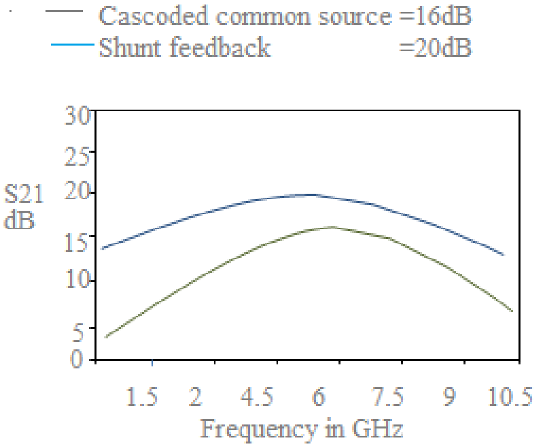

Figure 11: Forward gain (S_{21})

Noise Figure (NF)

The noise figure is shown in Fig. 12, the extracted noise figures of the LNA topologies are 1.85 dB for the cascode common-source and 2.63 dB for the shunt feedback amplifier. All the LNA topologies achieved a noise figure below 3 dB, because it is specifications for single ended LNA according to 802.16 WiMAX standards.

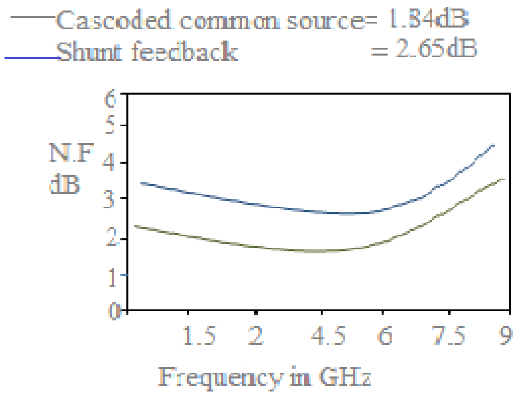

Figure12: Noise Figure (N.F)

Input Matching (S_{11})

The input matching of the designed LNA should be less than –10 dB while maintaining lowest noise figure. In the designed cascode common source LNA has -9.5dB and shunt feedback LNA has -11.2dB is achieved at 5.9GHz as shown in fig.13.

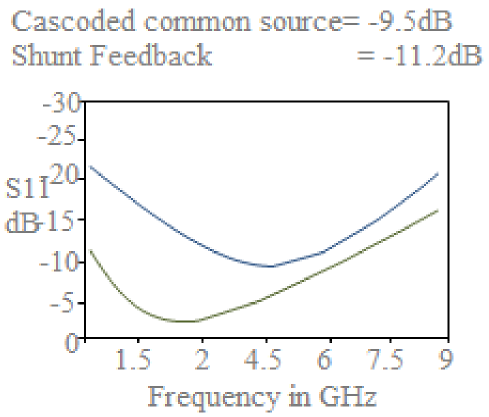

Figure 13: S11 Parameter

Output Matching (S_{22})

If the LNAs are having very low output impedance it achieves the required output matching without any output filter network at the output, but output matching network does not change the DC bias of the active device. The shunt feedback LNA has -22.8dB is achieved at 5.9 GHz and Cascode common source achieved -14.4dB as shown in Fig. 14.

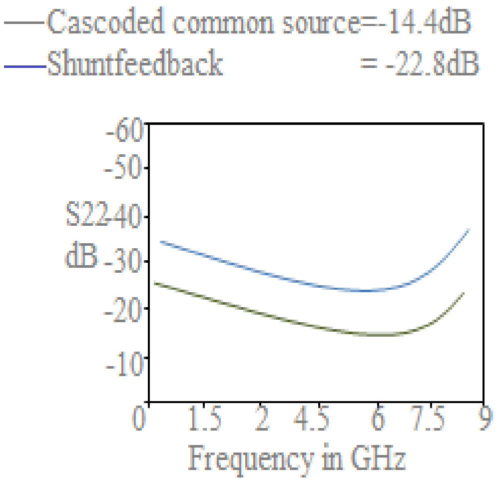

Figure 14: output matching parameter (S_{22})

Reverse Isolation (S_{12})

The reverse isolation is very important parameter to ensure better stability. Since the cascode stage eliminates the Miller capacitance, it is chosen to provide better isolation. The shunt feedback LNA achieved the best reverse isolation with -32.5dB at the frequency of 5.9GHz as shown in Fig. 15.

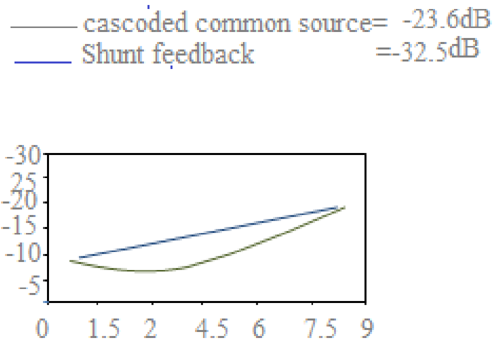

Figure 15: Reverse isolation (S_{12})

Stability Factor

The stability of an amplifier is a very important consideration in a design of an LNA and can be determined from the S parameters, the matching networks, and the terminations [10]. The stability factor, `K' is calculated over the frequency band 5.725GHz to 5.925 GHz by using the equation .10.

$$K = \frac{1+|S_{11}S_{22}-S_{12}S_{21}|-|S_{11}{}^{2}|-|S_{22}{}^{2}|}{2|S_{11}S_{21}|} \tag{10}$$

The two amplifiers are unconditionally stable with stability factor greater than 1 at the frequency of 5.9GHz is shown in fig .16.

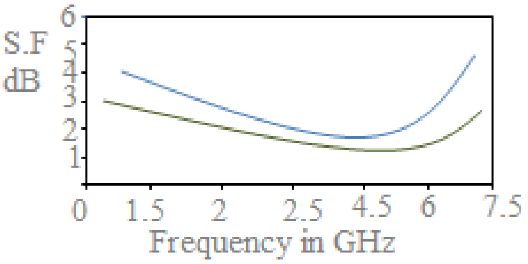

Figure 16: Stability factor

Linearity (IIP3)

The linearity due to feedback gave the shunt feedback amplifier the best linearity among the two amplifiers with an IIP3 of - 5.07dBm at the frequency of 5.9 GHz. The amplifier's linearity was determined by using the input referred third-order intercept point (IIP3). Fig. 17, the two amplifiers achieved the target IIP3 of -10dBm.

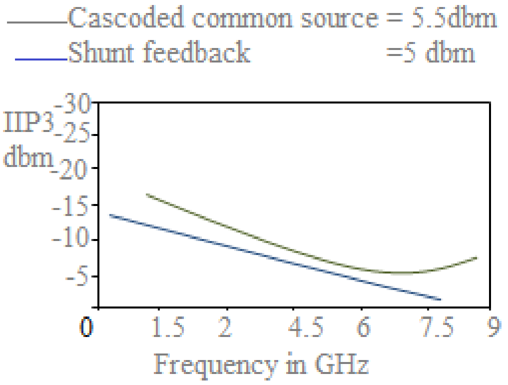

Figure 17: Third order intercept point (IIP3)

CONCLUSION

The designs of low-noise amplifiers are implemented for a WiMAX receiver. The amplifiers were implemented in a standard 180nm CMOS process using 1v as supply voltage, frequency range of 5.725 GHz to 5.925 GHz. The input matching using inductive degeneration cascade CS design achieved the lowest noise figure compared to other amplifier, due to the noise optimization in the implementation of the input. The cascode common source is also performed the lowest power dissipation because it contains only one current branch. By changing the value of the feedback resistor the shunt feedback amplifier achieved the highest gain. The shunt feedback LNA highly linearity performance makes its choice in the implementation of a wideband receiver LNAS, but it has a slightly high noise figure compared to the cascode common source LNA.

Table 4: Comparison of parameters of LNA

Ref	**Circuit Designs**	**V_{DD} [v]**	**f_c[GHz]**	**Gain [dB]**	**NF [dB]**	**P_{DC} [mW]**
[4]	Fold Amp	1	5.9	12.8	1.99	48.28
[11]	Cur Reus Amp	1.5	5	13	5.7	4.8
[12]	Distributive Amplifier	1.8	9	12.5	2.9	21.6
[12]	Com Gate	1.8	10	15	4.4	12
[12]	Differential Amplifier	1.4	5	12	5.2	22
P.W	**C.CS Amp**	**1**	**5.9**	**16**	**1.85**	**19.31**
	Shun Feed Amp	**1**	**5.9**	**20**	**2.65**	**56.8**

Ref	**Circuit Designs**	**S11 [dB]**	**S22 [dB]**	**S12 [dB]**	**IIP3 [dBm]**
[4]	Fold Amp	-12.3	-8.98	-25.9	-6.2
[11]	Cur Reuse Amp	-10.3	-14.5	-45.8	-5.6
[12]	Distributive Amplifier	-12	-8	-25	-5.9
[12]	Com Gate	-9	-12.4	-24	5.1
[12]	Differential Amplifier	-10.4	-14.7	-47.5	6.7
P.W	**C. CS Amp**	**-9.5**	**-14.4**	**-23.6**	**-5.5**
	Shunt Feed Amp	**-11.2**	**-22.8**	**-32.5**	**-5**

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