International Journal of Applied Engineering Research ISSN 0973-4562 Volume 13, Number 12 (2018) pp. 10580-10587

Realization of NOMA Scheme using Interleaved Division Multiple Access for 5G

Dr. S. Syed Ameer Abbas
Professor, Department of Electronics and Communication Engineering
Mepco Schlenk Engineering College, Sivakasi- 626005, India.

S. Priyadarsini
PG Scholar, Department of Electronics and Communication Engineering
Mepco Schlenk Engineering College, Sivakasi- 626005, India.

Abstract

Mobile communications has become one of the most developed technologies in the last two decades. Strong demand to increase system capacity is still growing dramatically. Non-orthogonal multiple access (NOMA) is a promising candidate for the future fifth generation (5G) systems because of its ability to provide greater spectral efficiency. Interleave division multiple access (IDMA) is one of the NOMA techniques that can support multiple access for a large number of users in the same bandwidth. This paper deals with IDMA to achieve high data rate with less complex transceiver design using VLSI implementation. The IDMA scheme basics scheme and IDMA multi-user detection concept used in the system is presented.

Keywords: Interleaved Division Multiple Access (IDMA), Non-Orthogonal Multiple Access (NOMA), 5G algorithm, Transmitter design, receiver design.

INTRODUCTION

Non-orthogonal multiple access (NOMA) is a key technology for the next generation of wireless networks because it has an ability to provide greater spectral efficiency and support a large number of users. Interleave Division Multiple Access (IDMA) is one of the NOMA techniques which is considered to be one promising technology for the fifth generation (5G) systems. IDMA is a special form of Code Division Multiple Access (CDMA) where the receiver differentiates each station (STA) by their unique interleaving patterns instead of unique spreading codes. This leads to a low complexity receiver which grows linearly with the number of parallel stations (STAs) [1]. IDMA has been previously proposed for cellular networks as an upgrade to the 3rd generation wideband CDMA system. In [2], the authors proposed a single carrier multi-layer IDMA system for 3GPP long term evolution (LTE) systems. This system features direct enhancement of throughput and reliability from the previous CDMA based system. IDMA has several other advantages over uplink multiple access schemes such as orthogonal frequency division multiple access (OFDMA) and CDMA. These include higher spectral efficiency and insensitivity to clipping distortion [3]. In addition, because all users utilize all subcarriers simultaneously, there is no need for scheduling avoiding air overhead [4]. IDMA has an ability to employ different modulations such as Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), and other higher order modulations that are necessary for next generation communications [5]. This paper deals with IDMA to achieve high data rate with less complex transceiver design. The various NOMA techniques were discussed in section II. The transmitter and receiver designs of IDMA were presented in section III and IV. Finally the simulation results and conclusion were discussed in section V and VI.

NOMA TECHNIQUES

Non-orthogonal multiple access (NOMA) is one of the most promising radio access techniques in next-generation communications. Compared to orthogonal frequency division multiple access (OFDMA), which is the current de facto standard orthogonal multiple access (OMA) technique, NOMA offers a set of desirable potential benefits, such as enhanced spectrum efficiency, reduced latency with high reliability, and massive connectivity. The baseline idea of NOMA is to serve multiple users using the same resource in terms of time, frequency, and space. The available NOMA techniques can broadly be divided into two major categories, i.e., power-domain NOMA and code-domain NOMA. Code-domain NOMA can further be classified into several multiple access techniques that rely on low-density spreading and sparse code multiple access. Other closely related multiple access schemes in this context are lattice-partition multiple access, multi-user shared access, and pattern-division multiple access. Recent studies demonstrate that NOMA has the potential to be applied in various fifth generation (5G) communication scenarios, including Machine-to-Machine (M2M) communications and the Internet-of-Things (IoT). Moreover, there are some existing evidence of performance improvement when NOMA is integrated with various effective wireless communications techniques, such as cooperative communications, multiple-input multiple-output (MIMO), beam forming, space–time coding, network coding, full-duplex, etc. Since the principle of NOMA allows multiple users to be superimposed on the same resource, this leads to interference for such systems. Consequently, existing resource

management and interference mitigation techniques, especially for ultra-dense networks, need to be revisited due to the incorporation of additional interference this new technology brings. For the similar reason, beam forming and the resultant other problems (e.g., precoding) in massive-MIMO systems introduce additional challenges and need to be solved in order to achieve full utilization of these technologies. From the perspective of physical layer, existing channel coding, modulation and estimation related problems need to be revised as well. Some of the NOMA schemes includes Pattern Division Multiple Access(PDMA), Resource Spread Multiple Access (RSMA), Interleaved Division Multiple Access (IDMA), Sparse Code Multiple Access (SCMA), NOMA by Power Domain. The PDMA pattern defines the mapping of transmitted data to a resource group that can consist of time, frequency, and spatial resources or any combination of these resources. The pattern is introduced to differentiate signals of users sharing the same resources, and the pattern is designed with disparate diversity order and sparsity. SCMA can be considered as a combination of CDMA, Code Division Multiple Access and OFDMA, Orthogonal Frequency Division Multiple Access. In SCMA, different incoming data streams to be transmitted are directly mapped to code-words of different multi-dimensional codebooks, where each code-word represents a spread transmission layer. In this way the multiple data streams can share the same time-frequency resources of the signal. Resource spread multiple access (RSMA) relies on a combination of a low-rate channel coding scheme and a user-specific scrambling, Without the joint decoding process at the receiver side. RSMA has the potential to allow grant-free transmission and asynchronous multiple access. NOMA, non-orthogonal multiple access is to have signals that possess significant differences in power levels. NOMA non-orthogonality is intentionally introduced then as the signal is received demultiplexing is obtained as a result of the power difference between the two users. To extract the signal, successive interference cancellation is used within the receiver. Interleaver division multiple access (IDMA) is a technique that relies on different interleavers to separate signals from different users in a multiuser spread-spectrum communication system. IDMA is a special form of Code Division Multiple Access (CDMA) where the receiver differentiates each station (STA) by their unique interleaving patterns instead of unique spreading codes.This include advantages of higher spectral efficiency and insensitivity to clipping distortion Among various NOMA schemes IDMA is believed to have higher advantages.

A.IDMA OVER CDMA

CDMA is a spread spectrum technique that utilizes the entire spectrum. The users in the channel are identified by unique pseudorandom numbers that enhance the voice and data capacity, there by accommodating more number of users at any given time instant. However the serious limitation of CDMA is the multiple access interference due to the superimposition of different users sharing a common transmission medium. IDMA scheme is to mitigate the effects of MAI wherein the problem is overcome by assigning unique interleavers for each user. This is in contrast to the allocation of different frequency bands, different time slots and different spreading sequence in the FDMA, TDMA and CDMA systems respectively. All the users use a common spreading sequence which is dispersed to produce an uncorrelated sequence resulting in a simple and efficient chip-by-chip detection scheme. The IDMA system is visualized as a special case of CDMA systems if the interleaving index is assumed as the code sequence to identify the users. The IDMA offers the combined advantages of CDMA system along with various other features such as

(i) Rate and power adaptation: The IDMA system offers rate and power adaptation in downlink due to its multi-code feature. The scheme supports varied data rates in contrast to the other coding techniques. Furthermore the modulation scheme is fixed for all the users with same channel coding.

(ii) Frequency-selective fading: The IDMA performance is tested under realistic channel conditions such as SUI and LTE which are prone to frequency selective fading. The IDMA scheme offers improved BER performance even at low SNR.

(iii) Complexity: The receiver complexity is less in the case of an IDMA system as proposed by Wang and Poor. The receiver system employs a low rate decoder with turbo processing. This cancels out the interference effects such as multi-antenna interference, multi-user interference, multi-layer interference and inter symbol interference etc. The complexity is proportional to the number of layers, antennas, users, iterations and channel taps.

(iv) Resource allocation: The IDMA scheme exploits the same interleavers and hence the resource allocation is made simple.

(v) Low delay: In comparison with the conventional DS-CDMA, the block size can be controlled due to chip-by-chip interleaving. Knowledge of the a priori layer information is desirable for cancelling the effects of multilayer interference.

Therefore, the IDMA schemes are prevalent in the downlink communication system where base station processing is executed at the transmitter end. Some of the advantages of DS-CDMA such as the unity reuse factor, soft handover, resilience to interference are available with IDMA and hence IDMA can be considered as a special case of DS-CDMA. Thus IDMA systems can be called as an upgraded or improved CDMA.

IDMA TRANSMITTER

The transmitter structure of an IDMA system with multiple users is shown in Figure 1.

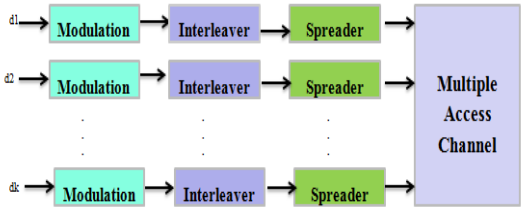

Figure 1. IDMA Transmitter block diagram

The input data sequence of user is modulated using Binary Phase Shift Key technique. Binary Phase Shift Keying (BPSK) is a two phase modulation scheme, where the 0's and 1's in a binary message are represented by two different symbols in the carrier signal. The input bit binary 0 is represented by +1 and input bit binary 1 is represented by -1.

Then resultant modulated bits are permutated by an random interleaver. Users are solely distinguished by their random interleavers. Random interleaver scrambles the data of different users with different pattern shown in Figure 2 Patterns of interleaving of data for the users are generated randomly. Due to the interleaving of data, burst errors of the channel are randomized at the receiver side and can be easily detected and corrected. For proper decoding of the sequence of interleaver, the receiver must have all the relevant information regarding pattern of interleaving at transmitter side. Therefore, in order to operate IDMA scheme properly, base station has to forward the information of interleaving at the receiver side of the system.

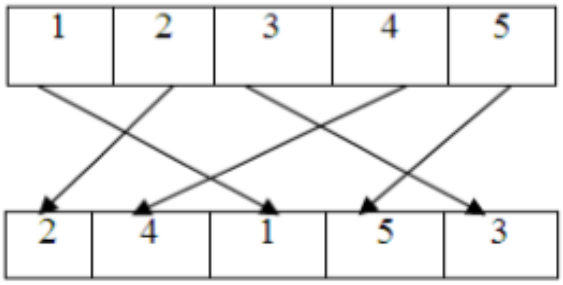

Figure 2. Random permutations in interleaver

The interleave output is given to the input of spreader. The spreader block replicates the interleaved output multiple times to increase the signal to noise ratio. The resulting signal is transmitted by using different antennas to transmit the signal to the channel. The channel adds all the data transmitted from the transmitters and project them towards the IDMA receivers.

A. BPSK MODULATOR

Binary Phase Shift Keying (BPSK) is a two phase modulation scheme, where the 0's and 1's in a binary message are represented by two different phase states in the carrier signal -1 for binary 1 and +1 for binary 0.In digital modulation techniques, a set of basis functions are chosen for a particular modulation scheme. Generally, the basis functions are orthogonal to each other. Basis functions can be derived using Gram Schmidt orthogonalization procedure. Every users' data at the IDMA transmitter is BPSK modulated. The Architecture for the BPSK modulator is shown in Figure 3. The Eight bit user data is given as the input to the BPSK modulator where each single bit is modulated into two real and two imaginary bits resulting four modulated bits for each bit of the user input. In the BPSK modulator each bit enters the BPSK modulation block where it gets modulated as shown in table 1.

Table 1: BPSK Modulation

Input bit	Real bits	Imaginary bits	Resultant bits
0	01	01	0101
1	11	10	1110

As a result from each BPSK modulation block inside BPSK modulator 4 bits are taken as modulated bits for each bit in the users' data. Hence as a whole for the 8 bit user data total of 16 bits are obtained as real bits and another 16 bits are obtained as imaginary bits which is projected to interleaver to permute the user data.

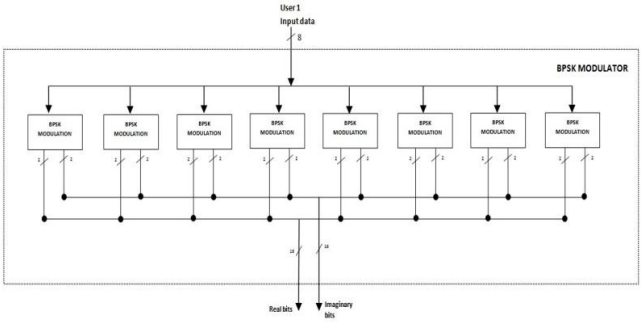

Figure 3. BPSK Modulator Architecture

B. INTERLEAVER

Interleavers are designed and used in the context of characteristics of the errors that might occur when the message bits are transmitted through a noisy channel. Random interleaver scrambles the data of different users with different pattern. Patterns of interleaving of data for the users are generated randomly. Due to the interleaving of data, burst errors of the channel are randomized at the receiver side and can be easily detected and corrected. For proper decoding of the sequence of interleaver, the receiver must have all the relevant information regarding pattern of interleaving at transmitter side. Therefore, in order to operate IDMA scheme properly, base station has to forward the information of interleaving at the receiver side of the system. Figure 4 shows the architecture for the interleaver at the transmitter side.

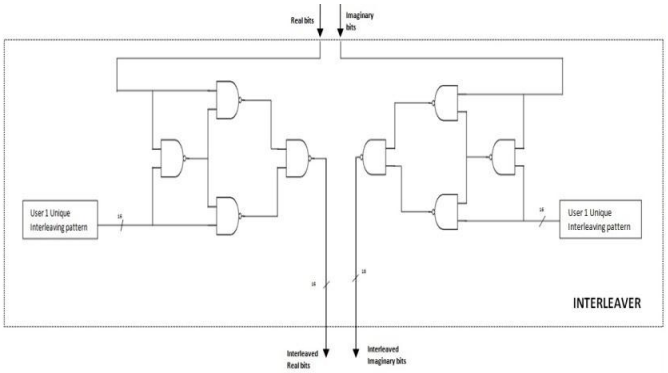

Figure 4. Interleaver Architecture

The modulated 16 real bits and 16 imaginary bits from BPSK modulator is interleaved using random interleaver. In Random interleaver user data is permutated in a random pattern based on the unique interleaving sequence in the block. Users are solely distinguished by their random interleavers. Interleaved 16 real bits and 16 imaginary bits are obtained as the output from the interleaver block and this output is given as input for the spreader.

C. SPREADER

In many communications environments it is desirable to spread the signal across as much of the allocated frequency spectrum as possible. This is usually done for one of three reasons: to enhance security of the communications channel. Figure 5 and 6 shows the architecture for the spreader.

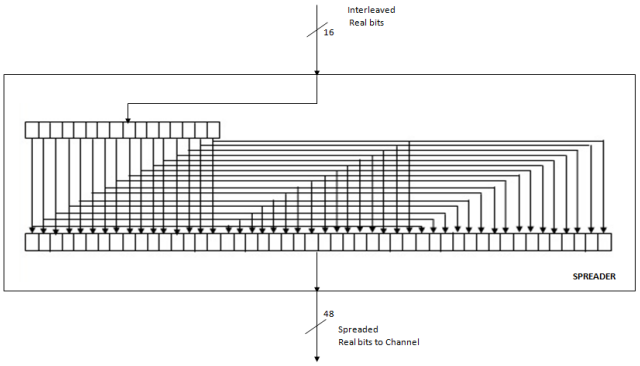

Figure 5. Spreader Architecture for real bits

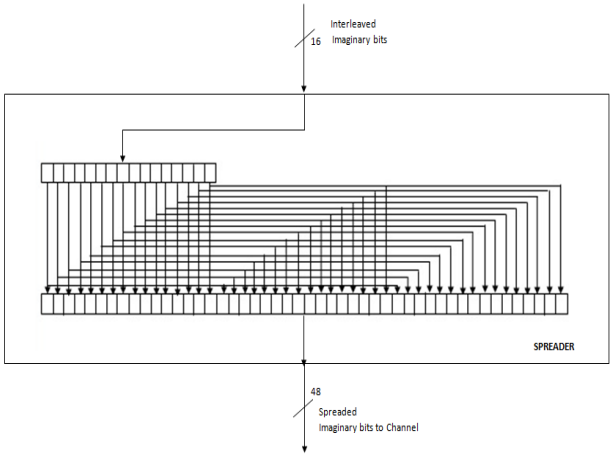

Figure 6. Spreader Architecture for imaginary bits

The interleaved data bits are passed to spreader where the data bits are replicated multiple times by the factor of three to have higher signal to noise ratio. In the spreader block 16 bits real data are spread into 48 bits and 16 bit imaginary data are also spread into 48 bits resulting total of 96 bits from the spreader. These 96 bits are now projected towards the channel as single user's data from the IDMA transmitter side.

IDMA RECEIVER

The IDMA receiver consists of multiuser detection, despreader, deinterleaver, and demodulator. Each block in the receiver is used to retrieve back the original data sent by every user. The Figure 7 shows the IDMA receiver structure.

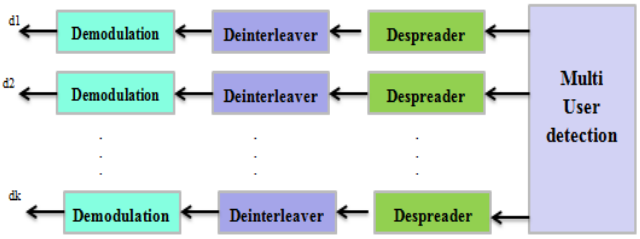

Figure 7. IDMA Receiver block diagram

The multiuser detection module is used to separate individual user's modulated interleaved and spreaded data from the combination of other user's data and assign it to respective receiver module to decode back the original data.The identified individual user's data is then given as input to the despreader where inverse operation of spreader is done. The duplicated data is removed and the interleaved data is obtained as the result. Then its output is given as the input to deinterleaver where interleaving patterns used at the transmitter is available and it is used to deinterleave the data to get back the modulated output. The resultant output from the deinterleaver is given as input to the BPSK demodulator where inverse operation of modulator is done to get back the original data of the user.

A. MULTIUSER DETECTION (MUD)

The processing in MUD need not be a successive detect and subtract process (called Successive Interference Canceller-SIC) and there are algorithms of MUD in which the optimized signals can be detected in few stages. The signals can be detected all together (N signals in one time). The detected signals are considered as estimate signals, now if one signal is to be detected in particular, the remaining N-1 estimated signals can be used to refine the estimate of this particular one (subtract the N-1 and detect again). The idea of minimum square error is used in such processing. This is sometimes called Parallel Interference canceller-PIC. This type of MUD can be optimum detection, in which the detection results in zero errors. In the initial detection stage of parallel interference canceller, the data symbols of all active users are detected in parallel by a Single User Detection technique. Then, the obtained interference is subtracted from the received signal and data detection is performed. Figure 8 shows the architecture for the multiuser detection module

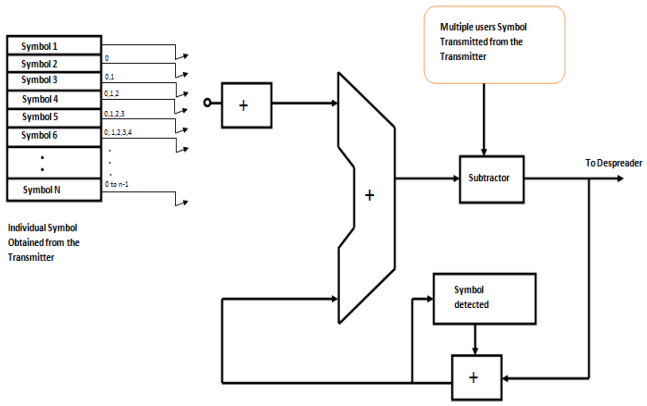

Figure 8. Multiuser detection block diagram

In the multiuser detection from the combined data each user's data is retrieved back and assigned to the corresponding receiver. The 48 bits of spread real data and 48 bit of imaginary spread data is obtained.

B. DESPREADER

From the user detection module individual user's data is retrieved back from the other user's data. This block takes the retrieved user's spread version of real and imaginary bits as input. Figure 9 and 10 shows despreader architecture for real and imaginary bits respectively.

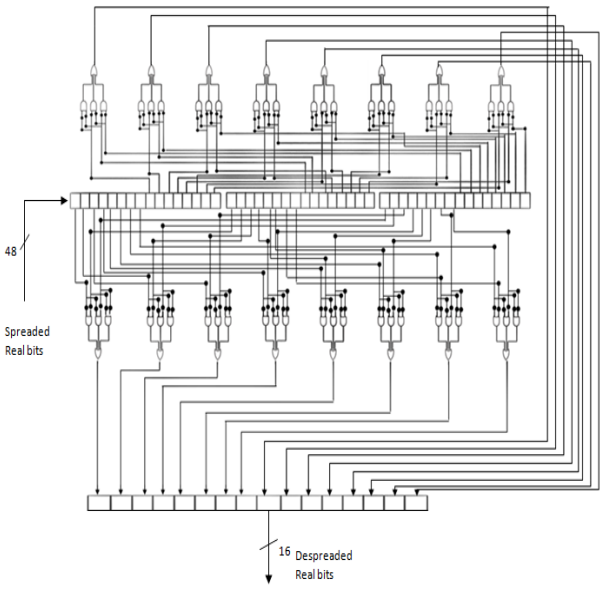

Figure 9. Despreader Architecture for Real bits

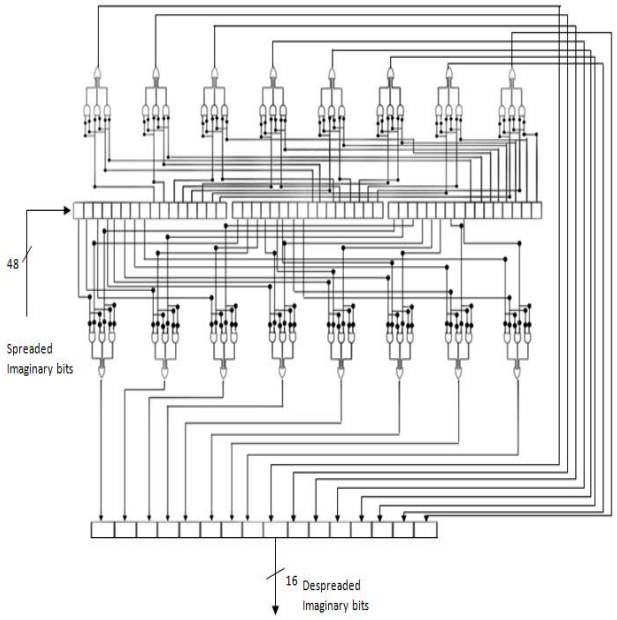

Figure 10. Despreader Architecture for imaginary bits

Since the user's data at the spreader is multiplied by the factor of three it must be despread to get back 16 original bits. This can be done in a way as follows: For each bit another two replicated bits are obtained at the spreader. These three bits compared and majority of these bits is obtained so as to get back the single original bit. This majority operation is done by the digital circuit as shown in Figure 11 and the truth table for the majority circuit is listed in table 2.

Table 2. Truth table for Majority Circuits

A	B	C	MAJORITY
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

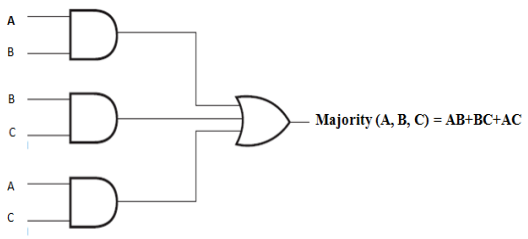

Figure 11. Majority Circuit

C. DEINTERLEAVER

For proper decoding of the sequence at deinterleaver, the receiver must have all the relevant information regarding pattern of interleaving at transmitter side. Therefore, in order to operate IDMA scheme properly, base station has to forward the information of interleaving at the receiver side of the system. Figure 12 shows the architecture for the deinterleaver at the receiver side.

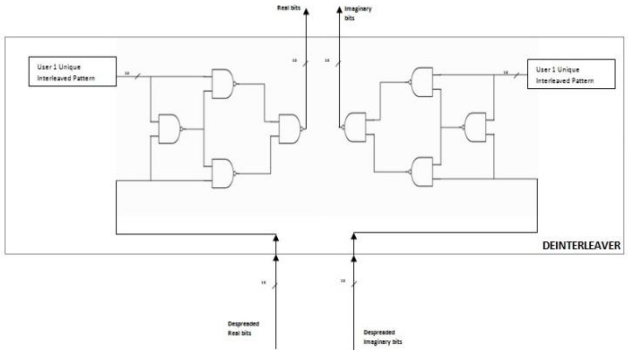

Figure 12. Deinterleaver Architecture

The despread 16 real bits and 16 imaginary bits from despreader is deinterleaved once again using random interleaver. In Random interleaver user data is permutated in a random pattern based on the same unique interleaving sequence used at the transmitter side. So that users are solely distinguished from other users. Deinterleaved 16 real bits and 16 imaginary bits are obtained as the output from the deinterleaver block so as to get back the same modulated output at the transmitter side and this output is given as input for the BPSK demodulator.

D. BPSK DEMODULATOR

The Architecture for the BPSK modulator is shown in Figure 13. The user data is 16 real bits and 16 imaginary bits are given as the input to the BPSK demodulator where 16 real and imaginary bits are split into 8 groups each consisting of 2 real bits and 2 imaginary bits. Each group of bits is given to BPSK demodulation block to get back single demodulated bit from 2 real and 2 imaginary bits. In BPSK demodulation block the demodulation is done based on the table 3 to get back the single demodulated bit

Table 3. BPSK Demodulation

Input Real bits	Input Imaginary bits	Input to the Demodulator Block	Resultant bits
01	01	0101	0
11	10	1110	1

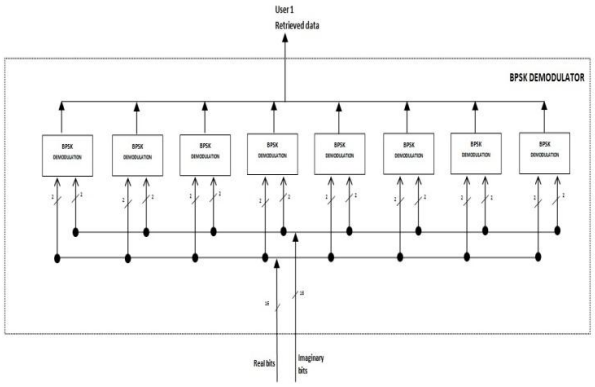

Figure 13. BPSK Demodulator Architecture

As a result from each BPSK demodulation block inside BPSK demodulator single bit is taken as demodulated bit. Hence as a whole for the 16 real bits and 16 imaginary bits of deinterleaved data from the previous block total of 8 bit original user data is retrieved from the demodulator. Hence the original data is retrieved in IDMA receiver side.

RESULTS AND DISCUSSION

Verilog codes are written for the transmitter and receiver structures of Interleaved division Multiple Access based on the architectures discussed in the previous chapter and simulated using Modelsim Altera Starter edition. The same structures are also implemented in the FPGA. The RTL schematics for each block, The FPGA editor for transceiver and Hardware utilization to implement the IDMA structure with four users is analyzed in this section.

A. RTL VIEW

Design at RTL level is a typical practice in modern digital design. One of the significance of the plan ahead tool is that it provides elaboration capabilities to compile RTL source files in the project. Figure 14 shows RTL view of transmitter and Figure 15 shows the RTL view of Receiver.

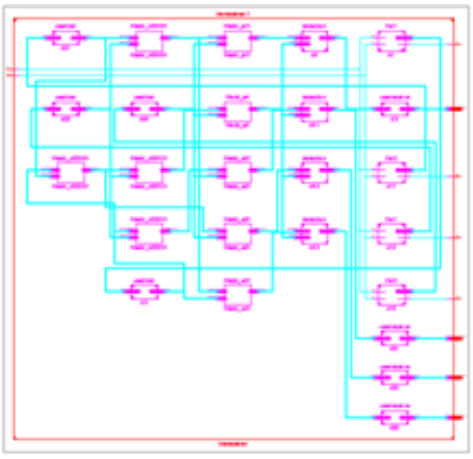

Figure 14. RTL view of IDMA Transmitter

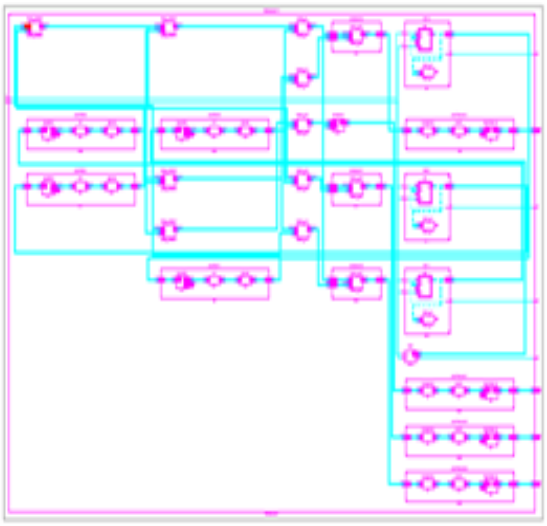

Figure 15. RTL view of IDMA Receiver

B. FPGA EDITOR

Lower level representations and ultimately actual wiring can be deriving from FPGA editor view. FPGA editor view represents the routing connection between logical blocks. FPGA editor view of transceiver is shown in Figure 16 and 17 respectively.

Figure 16. IDMA Transmitter editor view

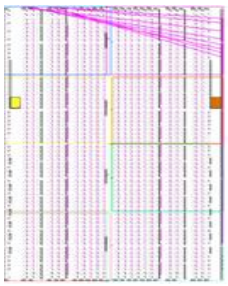

Figure. 17. IDMA Receiver editor view

C. SCHEMATIC

The Schematic of the Entire IDMA architecture with transmitter and receiver of four user is shown in Figure 18.

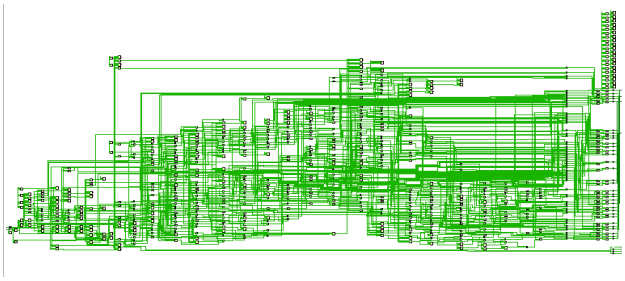

Figure 18. Schematic of IDMA Transceiver

D. DESIGN SUMMARY OF IDMA TRANSCEIVER

Design summary of transceiver is shown in table 4. Total resources utilization for the implementation is 38% of IO, 20% Slice LUT and has a maximum delay of 5.385 ns.

Table 4. Design summary of IDMA transceiver

Slice Logic Utilization	Used	
	Transmitter	Receiver
Number of Slice Registers	141	32
Number used as Flip Flops	110	32
Number used as AND/OR logics	31	36
Number of Slice LUTs	97	29
Number used as logic	56	56
Number of Multipliers	17	20
Number of Subtractors	1	4
Number of Adders	38	25

CONCLUSION AND FUTURE WORK

The Transceiver for a NOMA scheme, Interleaved Division Multiple Access was realized. Architectures for every module in the IDMA transmitter and receiver are drafted. Verilog codes are written for the transmitter and receiver structures of IDMA based on the architectures and simulated using Modelsim Altera Starter edition. The same structures are also implemented in the FPGA. The RTL schematics for each block using plan ahead tool is obtained, The FPGA editor for transceiver and Hardware utilization to implement the IDMA was discussed. The results obtained are analyzed with respect to number of Look up Table (LUT) and it is observed that transceiver utilizes 38% of IO resources, 20% Slice LUT resources and has a maximum delay of 5.385 ns.

The use of random interleaver can cause higher latency in the system, thus replacing the random interleavers with other low latency interleavers can be the future work for the proposed system.

REFERENCE

[1] L. Ping, “Interleave-division multiple access and chip-by-chip iterative multi-user detection,” IEEE Commun. Mag., vol. 43, no. 6, pp. S19–S23, Jun. 2005.

[2] P.A. Hoeher and X. Wen, “Multi-Layer Interleave-Division Multiple Access for 3GPP Long Term Evolution,” in Proc. IEEE Int. Conf. on Commun. (ICC), Glassgow, Scotland, pp. 5508–5513, Jun. 2007.

[3] D. Hao and P.A. Hoeher, “Iterative Estimation and Cancellation of Clipping Noise for Multi-Layer IDMA Systems,” in Proc. 7th Int. ITG Conf. on Sour. and Chan. Cod. (SCC), Ulm, Germany, pp. 1–

6, Jan. 2008.

[4] K. Kusume, G. Bauch and W. Utschick, "IDMA vs. CDMA: Analysis and Comparison of Two Multiple Access Schemes," IEEE Trans. Wireless Commun., vol. 11, no. 1, pp. 78–87, Jan. 2012.

[5] T.T.T. Nguyen, L. Lanante, Y. Nagao, and H. Ochi, "Low Complexity Higher Order QAM Modulation for IDMA system," in Proc. IEEE Wireless Commun. and Net. Conf. Work. (WCNCW), New Orleans, USA, pp. 129–134, Mar. 2015.