International Journal of Applied Engineering Research ISSN 0973-4562 Volume 13, Number 7 (2018) pp. 4911-4914

Design and Analysis of 4-BIT SRAM using Sleepy-Stack with Keeper and Dram Using Microwind

M.Bhavani[1]*, B.Purnima[2], B.Sruthi[3], J.Saisree[4] and CH. Manasa[5]

[1]Assistant Professor, Department of Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India.

[2,3,4,5] Department of Electronics and Communication Engineering, Bapatla Women's Engineering College, Bapatla, India.

Abstract

As the technology increases the amalgamated compactness of transistor also increases. There is a demand for portable devices like mobiles, notebooks and laptops etc. For this compactness design, feature estimate is diminished by the enhanced innovation. Reduced feature size devices require low power for their activity. Diminished power supply lessens the edge voltage. Low limit gadgets have better performance yet sub-edge leakage current paramount in such a deep submicron regime. Henceforth reducing this leakage is a noteworthy incitement for architects. To explain this numerous fieldworkers have proposed divergent thoughts. In this paper we proposed 4-bit static RAM cell using sleepy-stack keeper approach and also we implemented the 4-bit DRAM. The schematic of RAMs has been developed using DSCH and its layout has been created using Micro wind

Key-words: Sub-threshold leakage, Deep submicron regime, SRAM, DRAM.

INTRODUCTION

Initially all processors and computers were made up of CPU with only one hard disk which has the speed of 80M-120MHZ which is very slower to give data to CPU in time. That is the reason they placed the RAM in between CPU and ROM which works with speed near to CPU speed. Later on CPU is updated with multitask processor then it needs high speed access memory that time RAM is divided into SRAM and DRAM. With the quick development of present day correspondences and signal processing system, handheld remote PCs and buyer gadgets are winding up progressively prevalent[1]. A computer uses RAM to temporarily hold instructions and data for CPU processing tasks. In networking equipment, memory is used to buffer information. The demand for static random access memory (SRAM) is expanding with extensive utilization of SRAM in versatile items, System On-Chip (SoC) and high-performance VLSI circuits. SRAM is critical segment utilized for the cache memory. Dynamic random-access memory (DRAM) is a type of storage that is widely used as the main memory[2].

BASIC 6T SRAM

It is a type of semi conductor. It can store each bit by the use of bistable latching circuitry. When the memory is not powered, the data will be lost in the SRAM. In the SRAM it does not periodically refreshed and it is more expensive. It is typically used for CPU cache. SRAM cell is made of 6 MOSFETs[3]. Each bit in an SRAM is stored on 4 transistors(M1,M2,M3,M4) that are from two cross coupled inverters. It has two stable states that are 0 & 1.

HOLD operation

Write Line is disabled, no reading and writing is possible

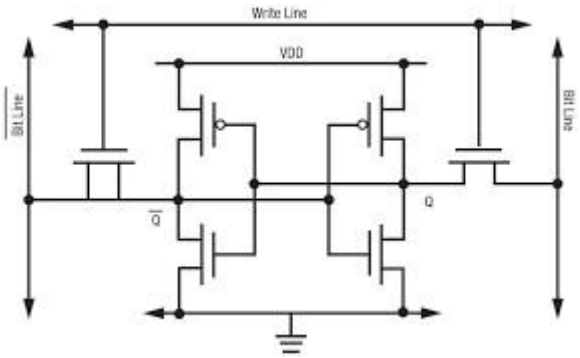

Figure 1. Basic 6T static RAM

READ operation

Reading starts with preloading the Bitlines to 1. Now the Writline gets activated. If Q is 1 then BL gets pulled to one and $\overline{BL}$ towerds zero. A sense amplifier senses which line hast he higher voltage[4].

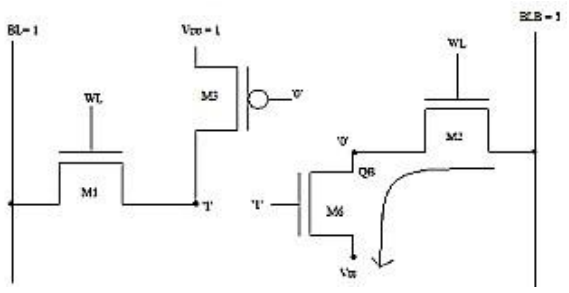

Figure 2.:Read equivalent SRAM circuit

WRITE operation

Setting the Bitline to 1 (BL = 1, $\overline{BL}$ = 0) then enabling the write line will write a one. The input-drivers have to be much stronger than the transistors.

SLEEPY STACK APPROACH

The sleepy stack approach has a structure combining the stack and sleep approaches by dividing every transistor into two half width and placing a sleepy transistor in parallel with one of the divided transistor. Sleep transistors are placed in parallel to the divided transistor closest to V_{dd} for pull up and in parallel to the divided transistor closest to GND for pull down[5]. The sleepy stack approach can have advantages of both the stack approach and the sleep approach. During the active mode, the sleepy stack approach results in lower delay than the stack approach because sleep transistors placed in parallel reduce resistance and already on[6].

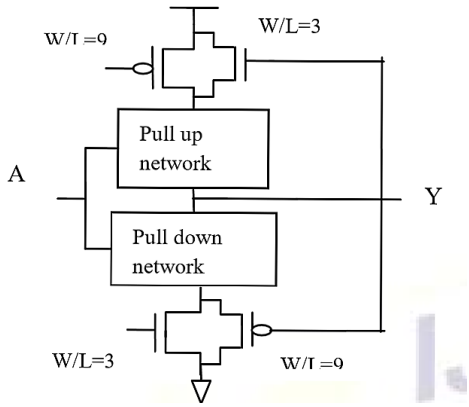

Figure 3. sleepy approach

PROPOSED WORK

The leakage reduction of the sleepy stack structure occurs in two ways. One is Leakage power is suppressed by high voltage transistors which are applied to the sleep transistors and the transistors parallel to the sleep transistors.[7] Another is Stacked and turned off transistors induce the stack effect.

According to forecast technology parameter, supply voltage VDD for 50nm and 90nm technology is taken as 0.5v,1.0v respectively.

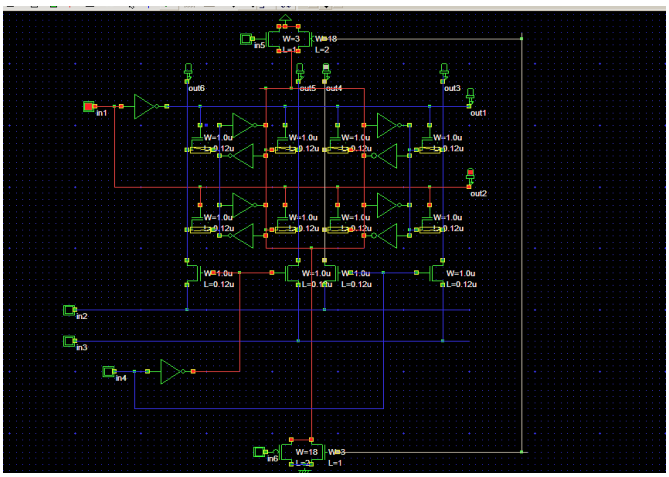

Figure 4. The 4-bit SRAM using sleepy stack with keeper

The correspondence layout design of 4-bit SRAM with sleepy stack is shown below.

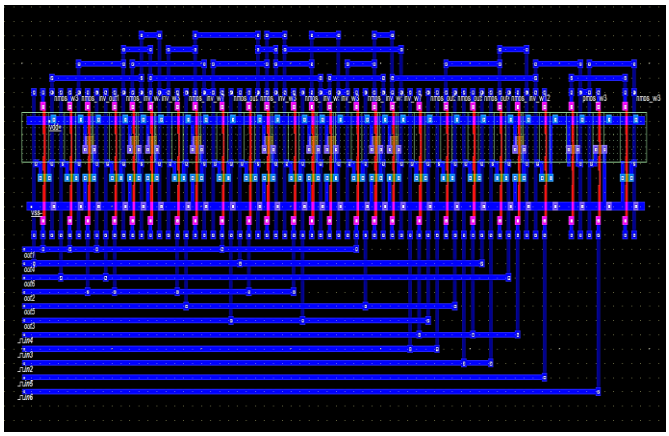

Figure5: layout design of 4-bit SRAM with sleepy stack

CIRCUIT SIMULATION & TABLE

Here the 4-bit SRAM cell is designed using a sleepy stack with keeper technique and the waveforms shows the operations at different technologies. In this we can observed that if we increase the technology then the power consumption also increases[8].

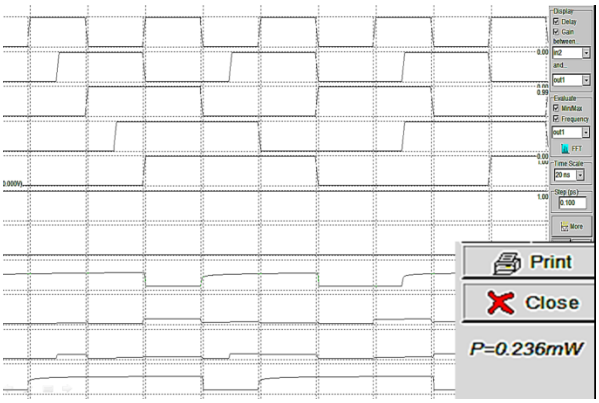

Figure 6.:Waveforms of 4-bit SRAM cell at 90nm technology.

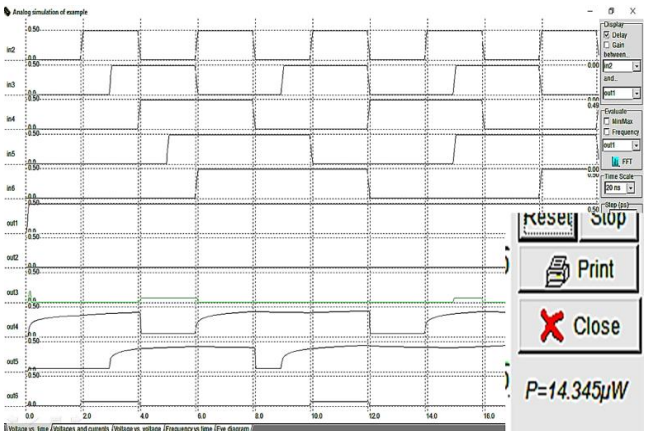

Figure 7. Waveforms of 4-bit SRAM cell at 50nm technology.

Table1: Area and power analysis of 4-bit SRAM

SRAM design	Area	Power consumption
1-bit SRAM	$113\mu m^2$	$0.112\mu w$
SSK 6T	$143\mu m^2$	$83.02\mu w$
4-bit SRAM	$270\mu m^2$	2.3mw
50 nm	$360\mu m^2$	$14.3\mu w$
90nm	$360\mu m^2$	0.23mw

BASIC DRAM

Dynamic random access memory (DRAM) is a type of random access memory stores each bit of information in a different capacitor inside an incorporated circuit. The capacitor can be either charged or discharged, these two states are taken to represent the two values of a bit, conventionally called '0' and '1'.Since capacitors is charged, the information eventually fades unless the capacitor charge is refreshed periodically. Because of this refresh requirement, it is a dynamic memory as opposite to SRAM and other static memory. The main memory(the "RAM") in personal computers is dynamic RAM (DRAM)[9].It is also used in the laptop and work station computers as well as video game.

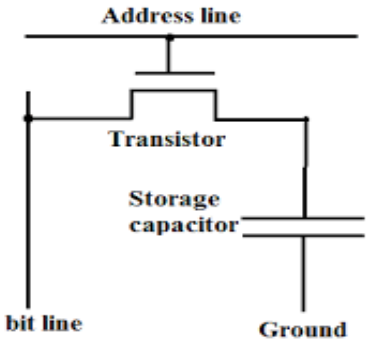

Figure 8. 1T DRAM cell

WRITE operation

Writing operation works with both bitlines to charge or uncharged capacitors.

READ operation

In Read operation, the voltage of a bit line is discharged to the ground through the transistor where the gate is charged with the high voltage[10]. The Read operation is non-destructive since the voltage stored at the node is maintained during the read operation.

PROPOSED WORK

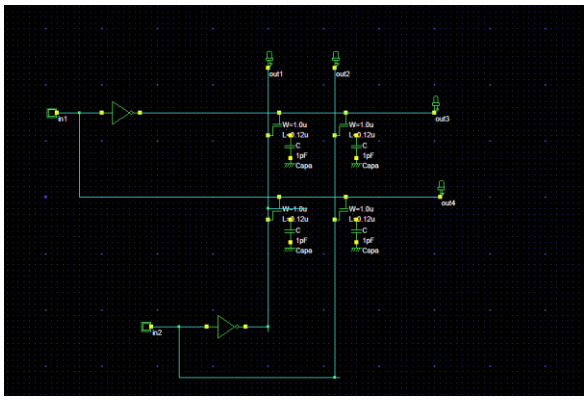

Figure 9. 4-bit DRAM schematic

The correspondence layout of the 4-bit DRAM cell is implemented on microwind tool. the figure shown below

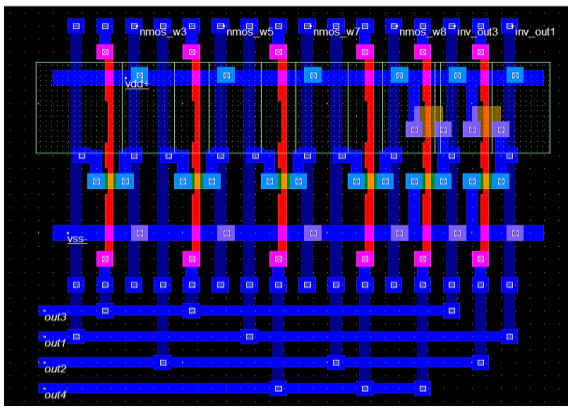

Figure 10. Layout of 4-bit DRAM

CIRCUIT SIMULATION & TABLE

MICROWIND software is used for this approach to analyse the leakage power dissipation. The waveforms of the DRAM cell is shown below.

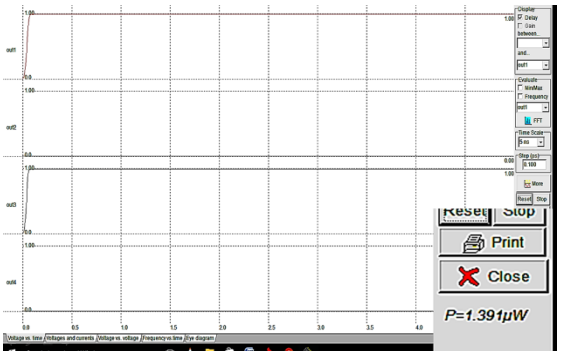

Figure 12: waveforms of DRAM at 90nm technology.

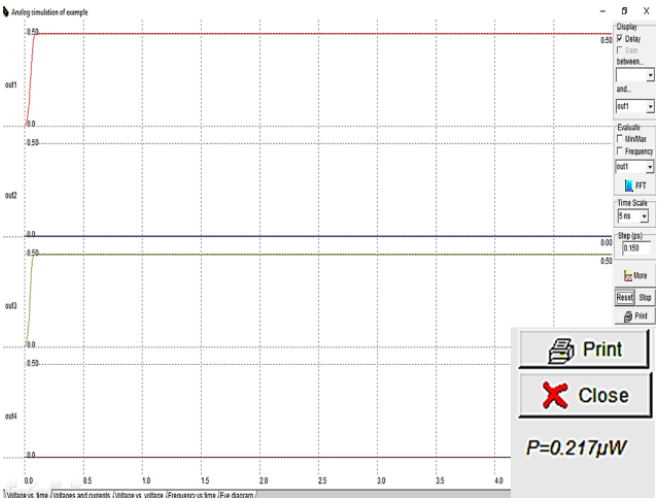

Figure 11: waveforms of DRAM at 50nm technology

In this we observed that if we increase the technology then the power consumption also increases.

Table 2: Area and power analysis of 4-bit DRAM

DRAM design	Area	Power consumption
1-bit DRAM	$53\mu m^2$	2.06mw
4-bit DRAM	$88\mu m^2$	$0.21\mu w$
50 nm	$88\mu m^2$	$0.15\mu w$
90nm	$88\mu m^2$	$1.39\mu w$

CONCULSION

In this paper we can observe that by using sleepy stack with keeper technique we can reduce the power consumption in static random access memory and also we implemented the dynamic random memory of 4-bit. Both schematics are designed in DSCH tool and layout implemented in MICROWIND tool. And also here we can observe that by reducing the technology we can save the power dissipation here we give the comparisons between 50nm and 90nm technology.

REFERENCES

[1] J. Park, "Sleepy Stack: a New Approach to Low Power VLSI and Memory," Ph.D.Dissertation, School of Electrical and Computer Engineering, 2005.

[2] J.C. Park, V. J. Mooney III and P. Pfeiffenberger, "Sleepy Stack Reduction of Leakage Power," Proceeding of the International Workshop on Power and Timing Modeling, pp. 148-158, September 2004.

[3] International Technology Roadmap for Semiconductors(ITRS05).http://www.itrs.net/Links/2005ITRS/Design2005.pdf.

[4] PetluruVenkataRamasandeep,M.Vinay Kumar, "Design and Development of 4 Bit SRAM Architecture by using Static Power Reduction Techniques"

[5] HinaMalviya, SudhaNayar, C M Roy, "A New Approach for Leakage Power reduction Techniques in deep submicron Technologies in CMOS Circuit for VLSI Applications," IJARCSSE, Vol. 3, Issue 5, May 2013.

[6] C.M.R. Prabhu and Ajay Kumar Singh, "A proposed SRAM cell for low power consumption during write operation", Faculty of Engineering and Technology, Multimedia University, Melaka, Malaysia.

[7] Ramnath Venkatraman, Olga Kobozeva, Franklin L. Duan, Arvind Kamath, S. T. Sabbagh,Miguel A. Vilchis-Cruz, Member, Jhon Jhy Liaw, Jyh-Cheng You, and Subramanian Ramesh , "The Design, Analysis, and Development of Highly Manufacturable 6-T SRAM Bitcells for SoC Applications", IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 52, NO. 2, FEBRUARY 2005.

[8] S. Y. Kulkarni, "Design and Verification of Low Power 64bit SRAM System using 8T SRAM:Back-End Approach" , IJEIT, Volume 1, Issue 6, June 2012.

[9] Akashe, S. ,Mudgal, A. , Singh, S.B. "Analysis of power in 3T DRAM and 4T DRAM Cell design for different technology" Information and Communication Technologies IEEE journal, Publication Year 2012.

[10] Sung-Mo Kang and Yusuf Lebelebici, "CMOS Integrated Circuits" Third edition; Tata McGraw-Hill; New Delhi.