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AC and DC caracteristics of simulated Doped Graphene Field Effect Transistor (GFET) Frequency Multipliyer

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Abstract

The presented work demonstrates the simulation of Graphene Transistor. Graphene filed effect transistor can be operated at high-frequency. The material parameters for device simulation have been extracted from the recently published literature. The device carrier transport calculations are performed with semiclassical Boltzmann transport models along with Poisson equations. The current-voltage characteristics analyzed and performance of the device is evaluated. Device parameters of the graphene radio frequency transistor have been extracted. The equivalent circuit has been built with passive components by using general purpose PSpice circuit simulator. Then the equivalent circuit performance is analyzed for a given input frequency.

Keywords: GFET, Semiconductor devices, modeling, Simulation, etc.

1. INTRODUCTION

Doped Graphene Filed Effect Transistor (GFET) improves career transport phenomenon [23].This is prorperty enables to utilize such marterials for development of high-performance application devices such as RF mobile unit, satellite communication and military applications [11, 14, 34]. GFET amplifier perform well on encoding and decoding for a high frequency signal [32, 45]. Graphene FET have four contacts such as drain, source, top gate and bottom substrate and each terminal has specific operational functionality. Works [36, 41].

GFET operaions are similar to FET (Field Effect Transistors).Gate controls the electron flow through channel with respect to bottom substrate [10, 30].This dertermines the nature of oerpation in the GFET reuslting in enhancement mode. GFET frequency amplifiers transport high electron density at low power which is major advantgae compared to to High Electron Mobility Transistor (HEMT) [1, 12].

Graphene is a single crystalline two-dimensional material formed by mechanical exfoliation methods from graphite. It occupies sp_2 hybridization of 0.34 nm thick carbon atoms [42]. Lattice structure is formed by these carbon atoms [22]. The pure condcuting nautre of the Grpahene is doped to develop new type of electronic devices [35]. Since oped graphene behaves like a semicondcutor [1].

There is need to occupy narrow bandgap in the graphene sheet. doped graphene bandgap is engineered by improving defect in the graphene. Graphene occupies narrow bandgap between conduction and valance band. The ambipolar behavior of GFET operates on high electron mobility transport [2, 20].

The device simualtions are perfomed using ATLAS deisgn tool.Well-designed GFET on TCAD Silvaco by extracting material parameters [1-3, 48]. GFET mirrior with MOSFET are replaced in silicon substrate with hexagonal silicon carbide material [13, 17, 33]. This results in quantum confinement channel by high dielectric material like hafnium dioxide (HfO_2) as gate capacitance [5]. Simulation of GFET with shorter channel length improves large career transport current thorugh doped graphene channel. Larger the current, Less requirement of gate voltage, high transconductance and high output voltage improves performance of GFET is depends on their DC analysis [16]. GFET device parameters are well extracted in small signal equivalent circuit on circuit simulator tool. A lower intrensic gate capacitance are imforms to take place GFET into the high frequency application [25]. This GFET device were tested in 10 MHz input frequency, its ransmitted at a maximum of 26 MHz. GFET improves performace of frequency multiplier output. Later on it will used in band pass filter and frequency seperation units [19].

2. DESIGN METHODOLOGY

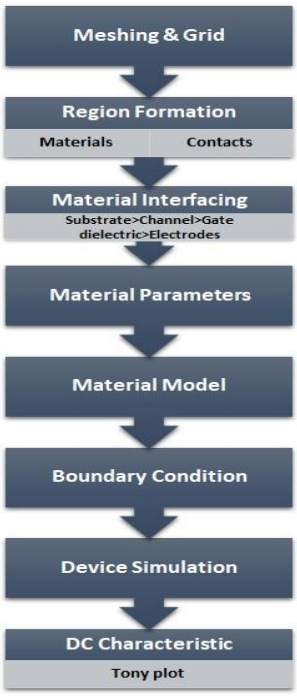

Figure 1: Computational modeling steps for GFET modeling

GFET device is structured and defined with Atlsa device simulator. Computational work starts from meshing, griding,

region formation, interfacing, Contacts identifications, material interface, material parameters, material model, boundary condition, Numerical method, Device simulation, DC caracteristics and ploting, etc. as shown in Figure 1 Silvaco/Atlas TCAD tool provies user friendly computional facility [15, 48]. The material constants like doped graphene bandgap, , dielectric values has been extracted from published research papers [27]. The GFET device is modeled by extracting device parameteres such as material constant, gate length, length of oxide thickness and channel width, etc. [4]. in nanometer scale. This is applicable for high career mobility transport also and depeneds on shorter channel length. [22, 37, 41].

3. MATERIALS AND METHODS

The selection of material reflects the device performance and includes doped graphene parameters such as energy band gap, permittivity, affinity, a material mobility of doped graphene extracted from research articles mention Table 1. There are various types of graphene bandgap opening such as substrate induced band gap opening, chemical substitution doping, hybrids, quantum confinement nanoribbon GNR (zig-zag and armchair), Graphene Nano-mesh, etc. [8]. 0.25eV energy bandgap is utilized from recently published research papers [1-2]. GFET device modeled by metal oxide semiconductor FET. For the exploration of high electron and hole mobility through at 200nm GNT channel length depends on quantum confinement of the device. It requires high dielectric gate material hafnium dioxide (HfO_2).

Table 1: Doped graphene channel material parameter

Parameter	Doped graphene
Energy Band Gap	0.25 eV
Concentration (nc300 / nv300)	2.5 x e^{20}
Mobility	12000 cm/(V-s)

4. DEVICE MODEL

The role of material interface is for binding every layer to become a device. This operates for DC (Direct Current) parameters. Doped graphene channel is modeled with electrodes and six Carbon atom in a Si-C hexagonal structure. The carbon lattice layers are formed through covalently and establish strong carbon-carbon bonds [22]. The semiclassical Boltzmann transport model are used to confine channel width [26]. Contribution of electrons and holes for current conduction from source to drain happens simultaneously [6, 46]. The parameters used in the simulations are listed in Table 2 based on the extraction from different research papers. The 2D structure of GFET device modelled with mentioned parameters in Table 2 is shown in Figure 2 [38].

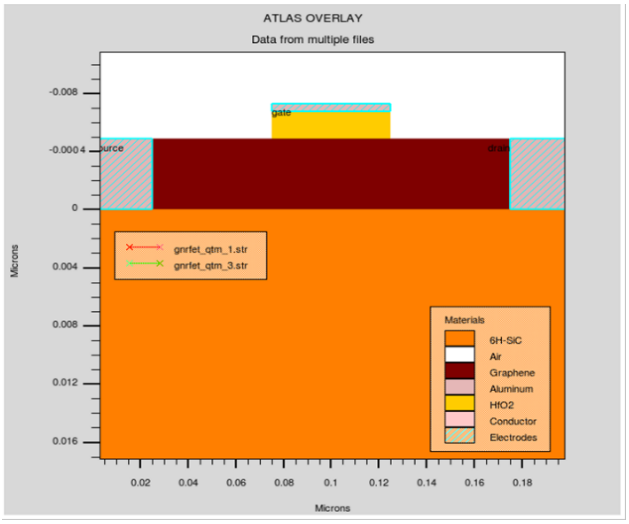

Figure 2: 2D-simulated GFET device.

Table 2: GFET device structure parameter

Parameter	Data (nm)
Channel Thickness	0.453
Channel Length	150
Device Length	200
Gate Dielectric Thickness	6.4

5. RESULTS AND DISCUSSION

5.1. DC Analysis

GFET operates under positive as well as negative gate voltage. This shows ambipolar behavior of GFET observed using Silvaco Atlas simulator [31, 48]. Also gate to substrate conductance, gate capacitance, parallel intrinsic capacitance, and parallel conductance were extracted through simulations etc. Dirac point at 1V dc gate bias voltage is shown in Figure 3. The confinement of channel gate length purely depends on the gate capacitance. This is also called as quantum capacitance. The gate Quantum conductance is extracted between the substrate and the gate terminal. The measured substrate to gate parallel conductance is for applied gate voltage between -0.2 V to 0.75 V respectively [3].

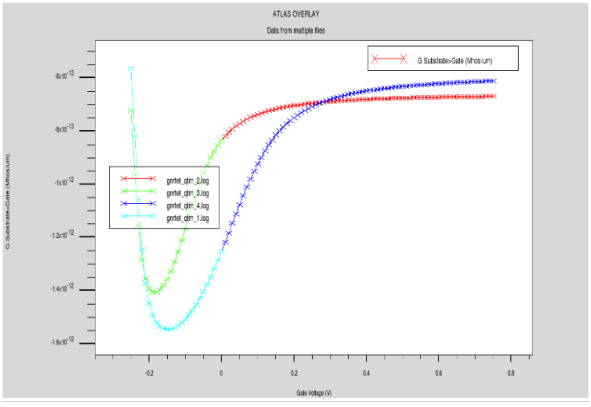

Figure 3: Gate conductance at confined channel region.

5.2. Gate Capacitance:

At radio frequency transistor operates with three gate capacitances [41]. They are electrostatic capacitance, gate dielectric capacitance and quantum capacitance. This is extracted from the DC analysis and output transfer characteristics [5, 9]. The smaller GFET with thinner gate oxide results in increased quantum mechanical effects [18, 37]. These are observed as shifts in threshold voltage and gate capacitance [28]. And were observed by varying gate voltage from -0.25 V_{DC} to +0.75 $V_{DC.}$ Shown in figure 4.

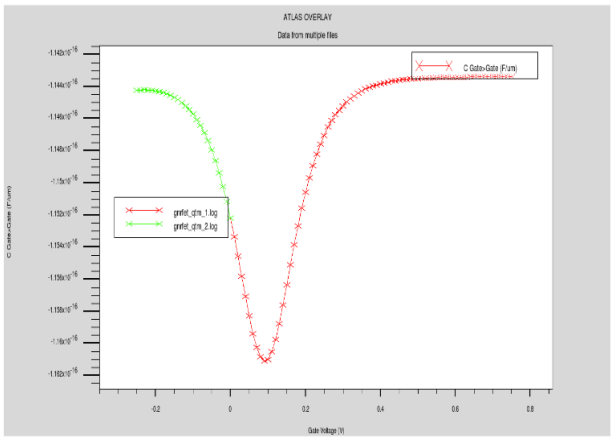

Figure 4: Gate dielectric capacitance

5.3. Gate to source capacitance

The gate to source capacitance is 4.61 x $10^{\wedge -17}$ which is from grpah as shown in Figure 5. Here gate to source capacitance achieved desired to peek at 0.1 V_{DC} with -0.2 V_{DC} to +0.75 V_{DC} voltage gate biased. This denotes the high-frequency incoming signal allowed by source terminal [47].

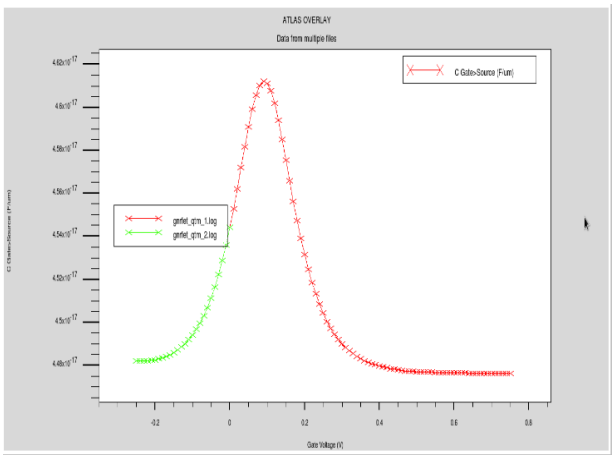

Figure 5: Parallel intrinsic capacitance

5.4. Ambipolar behaviour of GFET

Gate to substrate Capacitance extracted from the Figure 4 is more accurate at Dirac point for the multiplier circuit operation [3, 19, 31]. In the Figure 6 Dirac point measured while gate bias is from -0.2 V_{DC} to +0.75 V_{DC}. This is exactly at the +0.1V gate voltage. Graphene parallel parallels to the device from the substrate to gate conductance measured as referrred in [28, 35].

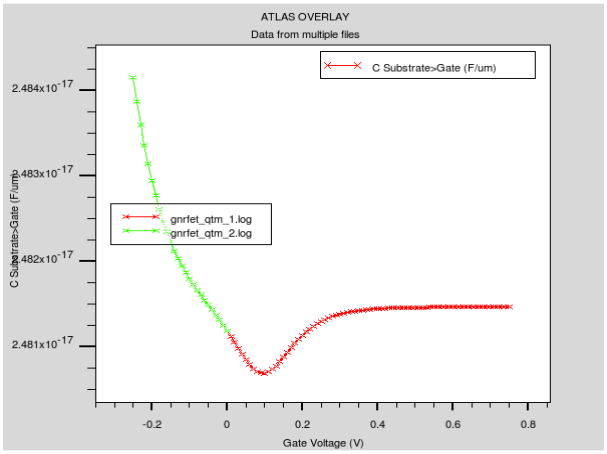

Figure 6: Parallel (substrate-Top gate) conductance

5.5. Transfer curve

The transfer characteristics for 50-nm gate shown in Figure 7. The single-channel GFET is simulated for a drain to source voltage (V_{DS}) of $1V_{DC}$. The transistor's threshold voltage V_{th} is defined for $1V_{DS}$ and a drain current of 10^{-7} A w/L flows and the effective gate-source voltage is related to the applied gate-source voltage V_{GS}. As to be expected from the 0.25 eV bandgap of the channel. The transistors show excellent switch-off, and on-off ratio of 1.5 x 10^6 for a $1V_{GS}$ gate voltage swing (from $V_{GS'eff}$ = 0.25 V_{DC} to +0.75 V_{DC}). The trans-conductance peaks at an effective gate voltage is around 0.68 V_{GS}.

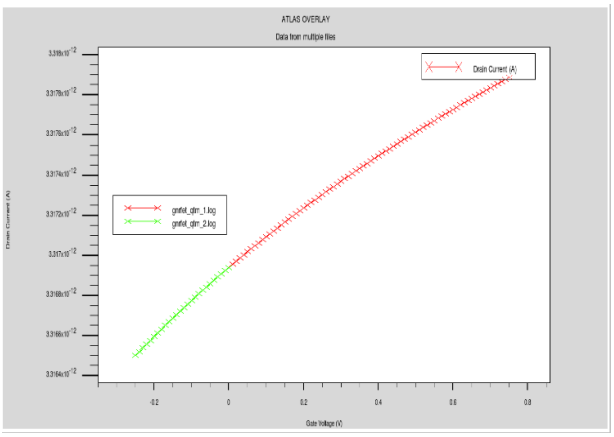

Figure 7: Transfer characteristics and

5.6 Output Characteristics

The output characteristics of transistor's operation and saturated drain current I_d is shown in Figure 8. The low drain conductance is 1.66 x e^{-06} at a drain to source voltage (V_{DS}) = $1V_{DC}$ and $V_{GS'eff}$ = 0.5 V_{DC} [46]. The good current saturation is caused by the semiconducting nature of the doped graphene channel. In addition to the high ON-OFF ratio, an important improvement in operation of GFETs in comparison to large-area graphene channels. The large are Graphene channels from a weak saturation and a large drain conductance [10, 30].

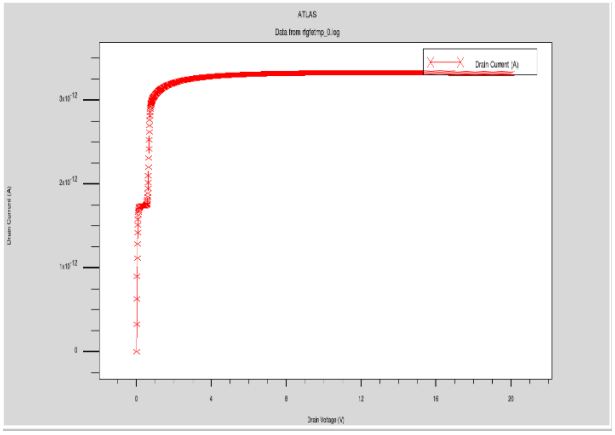

Figure 8: Output characteristics

5.7. Intrinsic parameters

As given in the Figure 10 radio frequency intrinsic parameters were extracted from the doped graphene transistor device simulator [43, 44]. These results are used to estimate the performance using the amplifier as a frequency multiplier circuit as shown in Figure 9 and 10 [29].

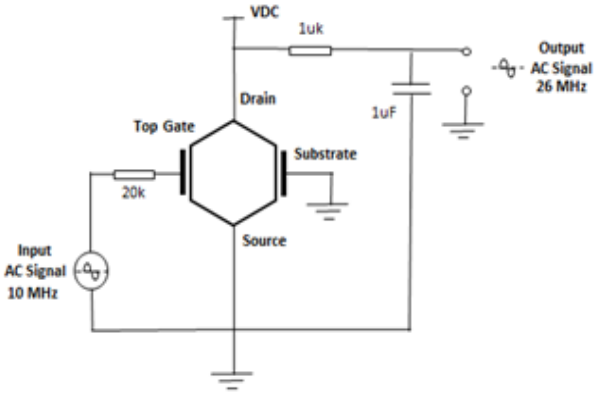

Figure 9: GFET frequency multiplier

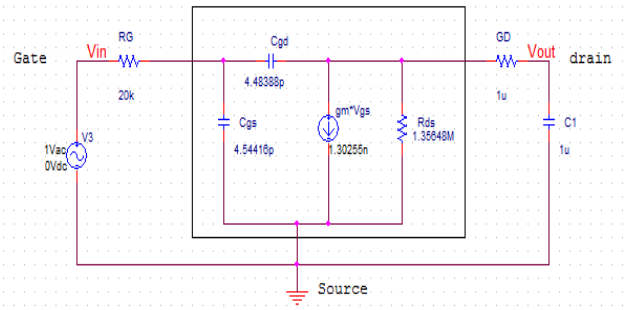

Figure 10: Equvalent circuit of GFET RF transistor

For the requirement of amplifier biasing, a voltage divider gate and drain resistors are include for separating all alternating current (AC) analysis data from the input and output circuit [9, 17, 29] as shown in Figure 11.The intrinsic parameter used in the simulation is given in Table 3 [7].

Table 3: Intrinsic GFET device parameters

Intrinsic elements	DC parameters
Gate to drain Capacitance	4.48388 e^{-17}
Gate to source Capacitance	4.54416 e^{-17}
Drain to source Resistance	1.35648 e^{+13}
Trans-conductance	1.30255 e^{+13}

Band stop frequency depends on Gate to Drain Capacitance (C_{GD}). This should be as small as possible, since the cut-off frequency will be high. Figure 7 shows the bode plot of the transistor's operation when it works as a low-pass filter.

This filter, only passes low frequency from. On the other hand, [16, 47]. The frequency of the transistor amplifier always results in generation of HF signals. [23]. The cut-off frequency is between 10MHz to 30MHz. High transmission bandwidth, Ultra low power and low complexity communication circuit are to be developed based on these results[24, 38].

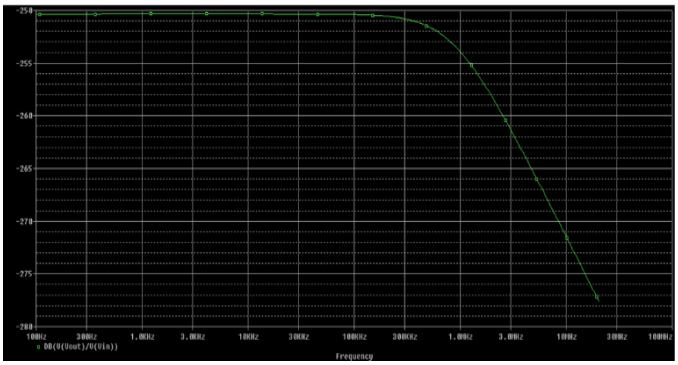

Figure 11: Bode plot shows highest cut-off frequency at maximum current gain -275.5 dB/ decade

6. CONCLUSION

The simulated results agree with standard observations found in the literature with regard to GFET with doped materials for channel. These simulations are to be tested with fabricated devices in the near future.

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