International Journal of Applied Engineering Research ISSN 0973-4562 Volume 14, Number 6 (2019) pp. 1275-1279

Implementation of Variable Duty Cycle Ring Oscillator for Unique Identification

N.Sivasankari [(1)], B.Balambiga [(2)] and P.Indumathi [(3)]

[(1)]Assistant Professor, Department of Electronics and Communication Engineering Mepco Schlenk college of Engineering, Sivakasi-626005, Tamilnadu, India.

[(2)] Department of Electronics and Communication Engineering , Mepco Schlenk college of Engineering, Sivakasi-626005, Tamilnadu, India.

[(3)] Department of Electronics and Communication Engineering , Mepco Schlenk college of Engineering, Sivakasi-626005, Tamilnadu, India.

Abstract

Different duty cycle ring oscillator is presented in this paper. This paper aims to drive a ring oscillator with different duty cycle without the knowledge of external persons, other than manufacturer. First we propose a dependence of duty cycle variation by changing different width and length ratio, and dependence of variation of power supply voltage. The simulation results confirm that duty cycle of CMOS inverters show the additional overhead with power supply and width to length ratio. This property can be used for authenticating one person in the common organization who is having the correct power supply value and W/L ratio. The simulation results using TANNER EDA for 0.125 μm CMOS shows a good agreement with analysis results. In addition in this paper the mathematical justification for duty cycle variation is explained. We present the parameters W/L and supply voltage to identify a person by producing different random number.

Key words: Asymmetric duty cycle, Ring oscillator, random number generation.

I. INTRODUCTION

Hardware solutions are useful for the recognition of integrated circuits, authentication generation in cryptographic architectures and protocols. All these different applications take advantage of the capacity of hardware devices to store or generate a only one of its kind, secure and unpredictable key in order to avoid hacker attacks or unlicensed use of hardware designs. Rather than creating many software's, it is more advantage and beneficial to implement a simple hardware with equivalent security. Same input applied to different ring oscillators with different $\left(\delta = \frac{W}{L}\right)$ ratio should result in unforeseeable responses with each other. This feature makes the devices suitable for security applications and they have become a main primitive in hardware security implementations. First, their randomness is assured by the process variability. Secondly, they are low cost as they do not suppose any overhead to the process fabrication. And thirdly, the security and attack resistance are guaranteed because any counterfeit attempt results in the device functionality destruction.

Ring oscillators [4] are used in many applications such as phase locked loop, random number generation etc., with a symmetric duty cycle. But this concept is slightly varied in [1] to produce asymmetric duty cycle to generate random waveform. The same concept is applied in [2] to produce Physical Unclonable Function (PUF) which will protect the circuit under different temperatures and environmental conditions. In [3] ring oscillator with high performance in terms of avoidance of phase noise is proposed, with the cost of additional MOS transistor for biasing. The authors of [5] made analysis on CMOS ring oscillator with thyristor structure. The authors of [6] propose new solution based on loop gain of ring and new frequency equations were described.

In this paper we propose

1. Authentication of persons without applying any additional circuitry.
2. Mathematical study of inverter and its behaviour as a function of power supply, inter-capacitance and W/L ratio.
3. Implementation analysis of power supply with transient analysis and W/L ratio with transient analysis
4. we enhance the uncertainty of the Ring oscillator and we provide more potential challenges for the same number of ring oscillators.

II. PROPOSED METHOD

Conventional Ring oscillators measure the output frequency and they determine relationships among them. Instead of measuring frequency, we design a ring oscillator based on measuring differences in the duty cycle of different signals. We introduce a methodology to design a ring oscillator with configurable duty cycle , which are not clocks of 50% duty cycle.

The whole system for application is shown in figure 1. It finds applications in authentication of concerned organization users. The users chip specification is known only to the manufacturer. During the issue of chip, the corresponding specifications for identification (V_{DD},φ) are provided. By again applying the same specification set (V_{DD},φ) the same

pattern is expected to be repeated. If the user is able to reproduce the pattern as specified by the manufacturer, then he is identified as authorized user.

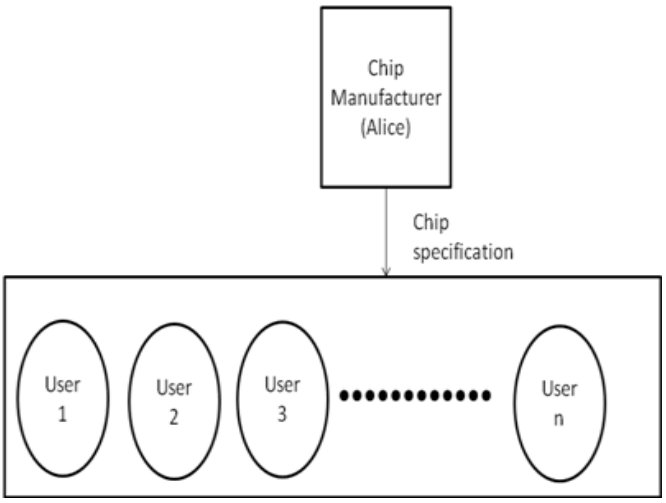

Figure 1: Issue of chip specification

The chip specification is given at the circuit manufacture level. In manufacturing, all the circuits have been implemented as CMOS. The specification in dimension of CMOS and power supply given to them are unique for each and individual user. The basic element in CMOS circuits is inverter. Let us see the design of inverter in its dimension level and how it affects the performance to distinguish each persons.

A. CMOS Inverter:

As per figure 2, the components present in CMOS inverter circuit are PMOS and NMOS.

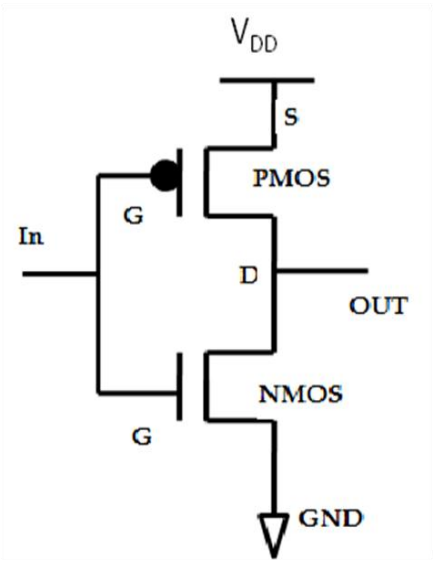

Figure 2: CMOS inverter

According to this model, the equation which is used to rule the source-drain current of an individual transistor is:

$$I_{ds} = \frac{Q_{ch}}{L/v} = \mu C_{ox} \frac{W}{L}(V_{gs} - V_t - V_{ds}/2)V_{ds} \text{ ----(1)}$$

Where Qch=charge inside the channel,

L=channel length, v=average velocity of carriers,

μ=electron/hole mobility constant, C_{ox}=capacitance per unit area of gate oxide, W=channel width,

V_t =transistor threshold voltage, V_{gs}=gate-source voltage, V_{ds}=drain source voltage.

Equation (1) is divided into three different regions depending on their input voltages:

$$I_{ds} = \begin{cases} 0, V_{gs} < V_t, Off \\ \frac{\beta}{2}(V_{gs} - V_t - V_{ds}/2)V_{ds}, V_{ds} < V_{DSAT}, Linear \\ \frac{\beta}{2}(V_{gs} - V_t)^2, V_{ds} > V_{DSAT}, Saturation \end{cases} \text{ ------- (2)}$$

Where V_{DSAT} splits ohmic node from saturation mode and $\beta = \mu C_{ox} W/L$ .The load capacitance should be known to set the propagation delay of an inverter. The load capacitance of each inverter is highly influenced by the gate capacitance of the next inverter since the inverters of ring oscillators are liable in a loop configuration. Thus other important parameter to determine the propagation delay of CMOS inverters within ring oscillators is their gate capacitance which is defined as:

$$C_g = C_{ox}(W_n + W_p)L \text{ ----------(3)}$$

We define the propagation delay fall time t_{pdf} as the time lapsed to change a node voltage from V_{DD} to $V_{DD}/2$.

$$t_{pdf} = \frac{V_{DD}C_l}{\beta_n(V_{DD} - V_t)^2} \text{ ……(4)}$$

We also define the propagation delay rise time t_{pdr} as the time lapsed to change a node voltage from 0 to $V_{DD}/2$.

$$t_{pdr} = \frac{V_{DD}C_l}{\beta_p(V_{DD} - V_t)^2} \text{ .....(5)}$$

Where β_p is the result of replacing μ by electron mobility μ_p .From (4) and (5) thus we can conclude that the propagation delay fall and rise depends on the bias voltage of an inverter, the load capacitance and the transistor size ratio from equations (4) and (5) the rise and fall times are the functions of V_{DD}, C_l, and W/L ratio.

$$t_{pd}(V_{DD}, C_l, W/L) \text{ ……(6)}$$

The above equation (6) implies that the propagation delay for rise and fall time is a function of factors like bias voltage, capacitance, and width to length ratio of the CMOS transistor. By changing these parameters, different responses can be obtained.

B. Duty cycle as a function of W/L ratio:

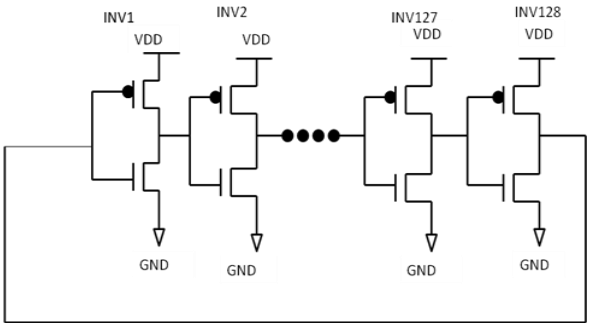

Figure 3: Ring oscillators with symmetric dimension

The traditional ring oscillator structure is shown in figure 3.Now let us see the dependence of duty cycle with respect to width to length ratio. Using the developed equations in the previous section we can study the ring oscillator as the chain of various CMOS inverters. The ring oscillator period T can be determined as the addition of all inverter propagation delays:

$$T = 2 * \sum t_{pdi} \ldots\ldots(7)$$

This work is mainly focused on controlling the duty cycle of every stage output instead of the output frequency. Thus, the period can be divided into t_{high} and t_{low}. t_{high} -the output is higher than $V_{DD}/2$—and t_{low}—the output is lower than $V_{DD}/2$.Therefore (7) is redefined as:

$$T = t_{low} + t_{high} \ldots\ldots(8)$$

A more specific analysis of the terms of the ring oscillator when they have combined is given below:

$$t_{highN} = t_{pdrN} + \sum_{1}^{\frac{N-1}{2}} (t_{pdf_{2i}} + t_{pdr_{2i-1}}) \ldots\ldots\ldots\ldots\ldots(9)$$

$$t_{lowN} = t_{pdfN} + \sum_{1}^{\frac{N-1}{2}} (t_{pdf_{2i-1}} + t_{pdr_{2i}}) \qquad \ldots\ldots\ldots\ldots..(10)$$

The particularization of the dependency in (6) for the ring oscillator nodes results in:

$$t_{pdfi+1}\left(V_{DDi+1}, C_{l(i+1)}, \left(\frac{W_{ni}}{L_{ni}}\right)\right) \quad \ldots\ldots\ldots (11)$$

The duty cycle of a digital signal is defined as the ratio between t_{highi} and its period T.

$$d_i = \frac{t_{highi}}{T} \ldots\ldots\ldots\ldots\ldots\ldots . (12)$$

All ring oscillators designs make use of inverters that are exactly the same, then all t_{pdri} and t_{pdfi} are equal and the duty cycle for each node N is determined from (9),(10),(12) by:

$$d_N = \frac{1}{2} + \frac{(t_{pdr} - t_{pdf})}{2N(t_{pdr} + t_{pdf})} \ldots\ldots\ldots\ldots\ldots\ldots(13)$$

t_{pdri} is the result of the aggregation of β,(3) and(4) and consequently its dependency with respect to Wi is:

$$t_{pdri} = \alpha_p\left(\frac{W_{ni+1} + W_{pi+1}}{W_{ni}}\right) \ldots\ldots \quad (14)$$

If we bring β,(3) and (4)together, then we can define t_{pdfi} for each inverter with respect to the transistor widths W_i. This definition remains as:

$$t_{pdfi} = \alpha_n\left(\frac{W_{ni+1} + W_{pi+1}}{W_{pi}}\right) \ldots\ldots(15)$$

Substituting (15) and (14) in (13),we get

$$d_N = \frac{1}{2} + \frac{1}{2N} \frac{\left(\alpha_p\left(\frac{W_{ni+1} + W_{pi+1}}{W_{ni}}\right) - \alpha_n\left(\frac{W_{ni+1} + W_{pi+1}}{W_{pi}}\right)\right)}{\left(\alpha_p\left(\frac{W_{ni+1} + W_{pi+1}}{W_{ni}}\right) + \alpha_n\left(\frac{W_{ni+1} + W_{pi+1}}{W_{pi}}\right)\right)} \quad (16)$$

equation (14) can be rewritten as

$$t_{pdri} = \alpha_p\left(\frac{W_{ni+1}}{W_{ni}} + \frac{W_{pi+1}}{W_{ni}}\right) \ldots\ldots\ldots\ldots\ldots \quad (17)$$

and substituting the relation

$\gamma = W_p/W_n$ $t_{pdri} = \alpha_p(1+\gamma)$ ----------(18)

similiarly $t_{pdfi} = \alpha_n(1+\frac{1}{\gamma})$ …… (19)

by substituting (18) ,(19) in (13),we get,

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\left(\alpha_p(1+\gamma) - \alpha_n(\frac{1}{\gamma}+1)\right)}{\left(\alpha_p(1+\gamma) + \alpha_n(\frac{1}{\gamma}+1)\right)}\right) \ldots\ldots.(20)$$

Further simplification yields ,

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\lambda(1+\gamma) - (\frac{1+\gamma}{\gamma})}{\lambda(1+\gamma) + (\frac{1+\gamma}{\gamma})}\right) \ldots\ldots..(21)$$

Let $\lambda = \alpha_p / \alpha_n$

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\frac{\lambda\gamma + \lambda\gamma^2 - 1 - \gamma}{\gamma}}{\frac{\lambda\gamma + \lambda\gamma^2 - 1 + \gamma}{\gamma}}\right) \ldots\ldots.(22)$$

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\gamma(\lambda-1) + \lambda\gamma^2 - 1}{\gamma(\lambda+1) + \lambda\gamma^2 + 1}\right) \ldots.(23)$$

The width of odd and even inverters are varied as per

$W_{po} = W_{ne} = \phi W_{pe} = \phi W_{no}$ .Thus $\phi = \frac{W_{po}}{W_{pe}} = \frac{W_{ne}}{W_{no}}$

By substituting the φ relations in equations (14) and (15),we get

$$t_{pdri} = \alpha_p(\gamma + \phi) \quad \text{.....(24)}$$

$$t_{pdfi} = \alpha_n(\gamma + \phi) \quad \text{.....(25)}$$

Substituting (24)and (25) in (13),

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\alpha_p(\gamma+\phi) - \alpha_n(\gamma+\phi)}{\alpha_p(\gamma+\phi) + \alpha_n(\gamma+\phi)}\right)$$

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\alpha_p - \alpha_n}{\alpha_p + \alpha_n}\right) \quad \text{.....(27)}$$

C. Duty cycle as a function of power supply:

The second method for obtaining the variable duty cycle is based on changing the bias voltage V_{DD} of each inverter as shown in Fig 4. Here, the width and length of the CMOS are not changed and are set to be in fixed value. The voltage is varied from 1V to the saturation level of the transistor. Duty cycle is varied as per the power distribution as shown in equation 28.

$$\text{Duty cycle} = \frac{P_{avg}}{P_{peak}} \quad \text{..... (28)}$$

D. Duty cycle as a function of capacitance:

As per equation 6, one of factor affecting the duty cycle is capacitance. But with the chain of inverters, propagation delay is not a function of inter-node capacitance. Substituting (4) and (5) in equation(13),we get, By simplifying,

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\beta_n(V_{DD} - V_t)^2 - \beta_p(V_{DD} - V_t)^2}{\beta_n(V_{DD} - V_t)^2 + \beta_p(V_{DD} - V_t)^2}\right) \quad \text{.....(31)}$$

$$d_N = \frac{1}{2} + \frac{1}{2N}\left(\frac{\beta_n - \beta_p}{\beta_n + \beta_p}\right) \quad \text{...(32)}$$

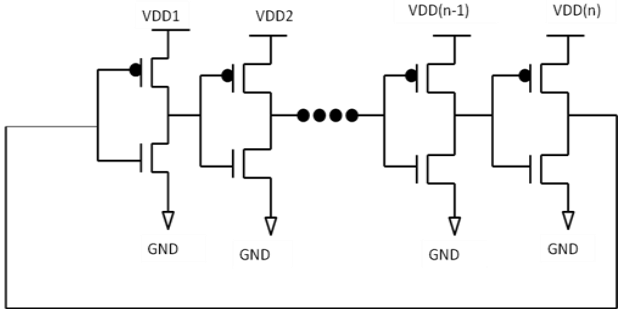

Figure 4: Various bias voltages applied to each inverter

From the equation 32, the duty cycle does not depend on internode capacitance.

The ring oscillator can be placed vertically as given in figure 5, to produce unique waveform for identification. The order and φ values are different for each user. It is shown in figure

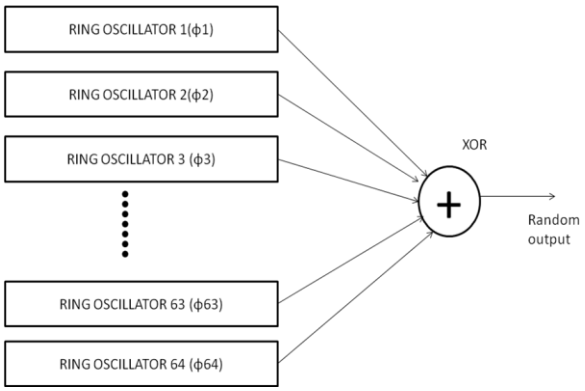

Figure 5: User chip circuit

III. RESULTS AND DISCUSSION

The experiments are conducted with different supply voltages. In each oscillator 128 inverters have been connected, the voltages at different nodes have been taken and the peak voltage among them is calculated. Value of ϕ is sets as 3. The variation in duty cycle, calculated as per equation (28) is shown in table 1.

Table 1: Bias voltage Vs Duty cycle

Average voltage	Peak voltage	Bias voltage	Duty cycle
0.437	0.7209	1	0.61
0.75	1.4	2	0.54
0.978	1.874	3	0.52
1.5	2.9	4	0.52
3.1	4.5	5	0.68
3.79	4.7	6	0.81

The inter node capacitance value is measured, and the variations in duty cycle with respect to capacitance is taken and tabulated in table 2.

Table 2: Capacitance Vs Duty cycle

V_{DD}(V)	Capacitance	T_{high}(ns)	Total Period(ns)	Duty Cycle
2.3	2pf	102	200	0.51
	3pf	102	200	0.51
	4pf	102	200	0.51
3.5	2pf	104	200	0.52
	3pf	104	200	0.52
	4pf	104	200	0.52
4.7	2pf	108	200	0.54
	3pf	108	200	0.54
	4pf	108	200	0.54

From the table 2, it is observed that duty cycle is not a function of capacitance. It is slightly varied with respect to bias voltage. φ value is fixed as 3 for all the measurements in table 2.

The value of φ is changed by keeping V_{DD} constant, and duty cycle is measured.

Table 3: W/L(φ) ratio Vs Duty cycle

φ	T_{high}(ns)	Total Period(ns)	Duty Cycle
3	102	200	0.51
4	102	200	0.51
5	102	200	0.51
7	103	200	0.515
9	105	200	0.525
15	108	200	0.54
20	109	200	0.545

From table 3, it is inferred that duty cycle is highly varied with respect to width to length ratio φ, compared to bias voltage and capacitance dependence. Hence more random waveforms with different duty cycle can be generated by changing the value of φ.

In our experiment, it is assumed that 64 users are enrolled. Hence 64 times ring oscillator is instantiated with different φ value, with the depth of 128.They are combined with XOR gate to produce the unique required waveform. From the analysis of table 1,2 and 3 we set φ=7,V_{DD}=5V.The random waveforms are shown in figure 6,7 and 8.

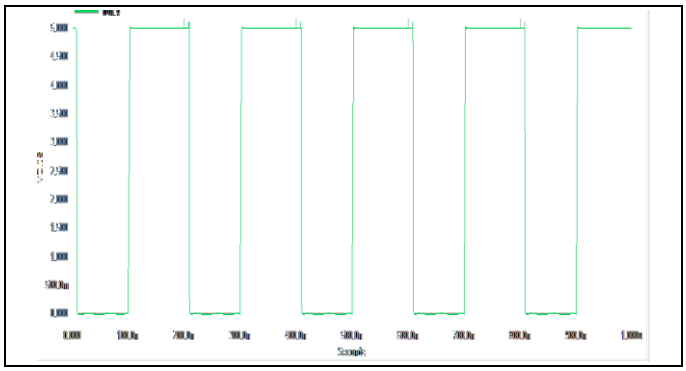

Figure 6: Duty cycle for W/L =7

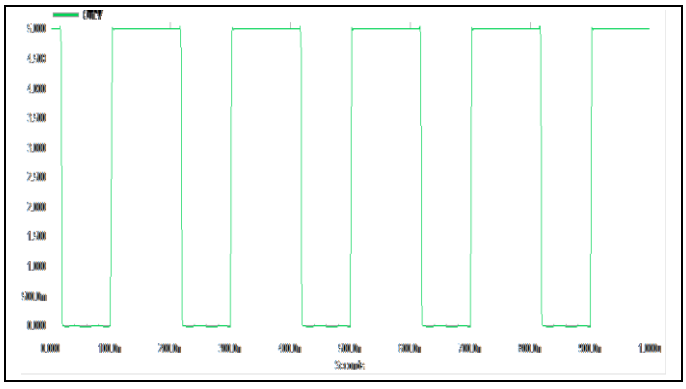

Figure 7: Duty cycle for W/L =15

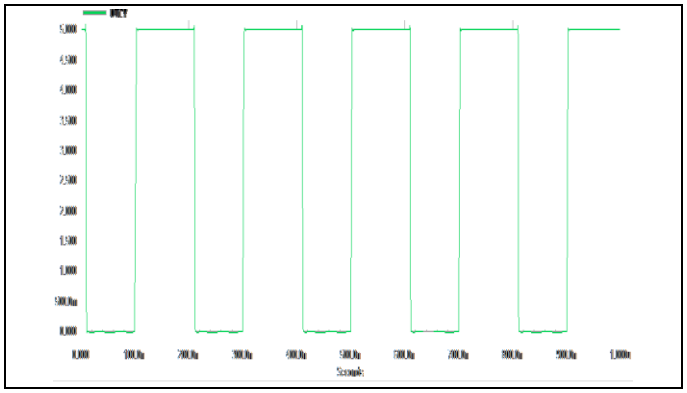

Figure 8: Duty cycle for W/L =20

IV. CONCLUSION

In this paper, the implementation of variable duty cycle ring oscillator chip is proposed by two methods. Duty cycle variation is done by transistor sizing and bias voltage.The idea used in this paper, for transistor sizing is,v arying the width to length ratio(aspect ratio)of NMOS and PMOS transistor is utilized to produce random waveforms for identification. In transistor sizing,the length of the PMOS and NMOS are kept as same whereas the width is changed so that the current varying parameters won't affect the performance more.

REFERENCES

[1]. Javier Agustin and Marisa Lopez-Vallejo,"An In-Depth Analysis Of Ring Oscillators:Expoliting Their Configurable Duty –Cycle",IEEE Trans.Circuits and Systems,Vol.62,No.10,Oct.2015

[2]. Javier Agustin and Marisa Lopez- Vallejo,"A Temperature-Independent PUF with a Configurable duty cycle of CMOS Ring Oscillators",IEEE,2016.

[3]. Yusuf Jameh Bozorg and Mohammad Jafar Taghizadeh Marvast , "Designing a New Ring Oscillator For High Performance Applications In 65nm CMOS Technology" Indian Journal of Fundamental and Applied Life Sciences, *Vol. 4 (S4), pp. 1978-1984,2014.*

[4]. V. Sikarwar, N. Yadav and S. Akashe, "Design and analysis of CMOS ring oscillator using 45 nm technology," *2013 3rd IEEE International Advance Computing Conference (IACC)*, Ghaziabad, 2013, pp. 1491-1495.doi: 10.1109/IAdCC.2013.6514447.

[5]. Balaji Ramakrishna S, Shivananda Yalpi, Nithin Kumar L, Ravindra H.B, Chaina Ram,"Design and Performance Analysis of Low Frequency CMOS Ring Oscillator using 90nm Technology", *IEEE* International Conference,May 20-21,2016.

[6]. P.M.Farahabadi, H.Miar-Naimi and A.Ebrahimzadeh," A New solution to analysis of CMOS Ring Oscillators", Iranian Journal, Vol. 5, No. 1, March 2009.