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Performance Analysis of UPFC Embedded With Three Level Cascaded H Bridge Inverter with SPWM Technique and Anfis Controller

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Abstract

Hybridization of the computational and control techniques has gained great importance in the last few years. One such an effort is made to combine the Fuzzy Logic Systems and the Neural Network Sytsems. Neural Networks possess advantages in the area of Learning, Classifying and Optimization, where as Fuzzy systems are dominant in areas such as reasoning on a degree. Both the techniques have gained individual importance in the real world simulations. Both of them are grouped in a manner where one of them is used as pre-processor and the other as post processor. A trial and error approach is used to solve the problem. The performance improvement of UPFC with reference to the Transient Stability and Dynamic Stability Enhancement incorporating a combination of ANN and Fuzzy Logic controller called the ANFIS Controller is analysed. The UPFC is embedded with a 3 level Cascaded H Bridge Inverter. The Response time taken by UPFC with ANFIS Controller is very less. Cascaded H Bridge Inverters offer high level of Voltage Support, Low Switching Stress and Good Modularity. The system response to the reference commands or the correction commands is very faster. This aspect is shown by calculating the times like settling time in all the four cases of faults like LG, LL, LLG, LLL and also even when the loads are changed from normal to highly Inductive and highly capacity. The ANFIS Controller based UPFC helps the Power System Network to restore normalcy in a Very Less Time. UPFC is connected to the IEEE 5 bus system between the buses 3 and 4 for checking its capabilities. The performance of UPFC with ANFIS Controller Based UPFC has a better performance rate than PI, FUZZY LOGIC Controller based UPFC. The Simulations are carried using MATLAB Software.

Keywords: AC Transmission, FACTS, UPFC, IEEE-5 BUS System, Shunt Line Faults, Power Flow Control, Cascaded H Bridge (CHB) Inverters, SPWM, Fuzzy, ANN, ANFIS Controllers, Rise Time, Settling Time.

I. INTRODUCTION

The Unified Power Flow Controllers were basically proposed for real time control and dynamic compensation of the ac transmission system parameters and for obtaining more flexibility in solving the problems faced by the utilities. An earnest effort towards achieving the above goals is made here especially to improve the sensitivity of the device, the quality of output of the device, the response time of the device and also the controllability of the device by making the device to act like a self thinking machine. The Unified Power Flow Controller has two converters, one a shunt converter (converter 1), connected in shunt with the transmission network and other a series converter (converter 2) , connected in series with the Transmission Network These two converters are connected to each other by a common DC link capacitor. The presence of a common DC link enables the transfer of real and reactive power to flow between the two converters thereby enabling the absorption and injection of voltages and currents from and to the transmission network respectively. Each of the converters can independently generate and absorb real and reactive power at their respective ac terminals. The basic function of the Shunt converter (converter 1) is to supply the real power it can also supply or absorb reactive power. The series converter (Converter 2) provides the main function of the UPFC by injecting an ac voltage of requisite magnitude Vpq ($0 \leq Vpq \leq Vpqmax$) and phase angle δ ($0 \leq \delta \leq \delta$ max) at power frequency in series with the transmission line voltage.

II. UPFC FUNDAMENTAL CONFIGURATION

Terminal Voltage Regulation is done with UPFCs wherein the required voltage of change required on the Transmission line say, ΔV (Vinj) , is injected either in-phase or in anti-phase mode with the existing voltage Vo on the Transmission line.

Series Capacitive Compensation is done where the required value of voltage say, Vinj, is injected in Quadrature with the Line Current.

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Phase Shifting or Transmission Angle Regulation is done by injecting a voltage of Vinj in an angular relationship with Vo to get the required Phase Shift (Advanced or Retarded) in the Line output voltage without change in the Magnitude of the Line output voltage.

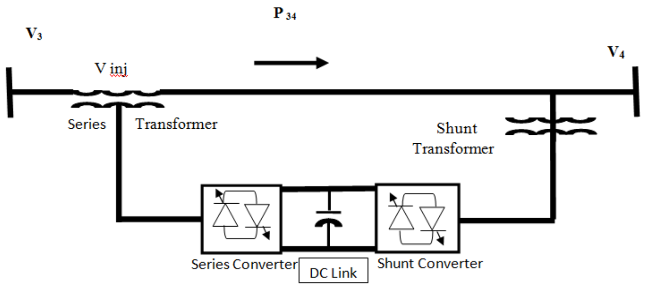

Fig.1. Three Level CHB Based UPFC for IEEE-5 Bus System

In the explanation that follows, the importance of using the ANFIS Controller in UPFC to enhance the Controlling Capabilities of UPFC are clearly explained. The UPFC incorporating a 3 Level CHB Inverter and an ANFIS Controller is tested for its improved performance on a Standard IEEE –5 Bus System. The UPFC is connected in the system between Bus number 3 and 4. The test conditions include (i) under voltage compensation (due to Increase in Inductive Load), (ii) over voltage compensation (due to Light load conditions or due to Capacitive Over Loadings), (iii) Transient Stability Enhancement Capabilities when the IEEE-5 Bus system is subjected to different Shunt Faults like LG,LL,LLG and LLL Faults at Bus No. 4. The immediate changes in the network conditions, more importantly, at the point of connection of the UPFC are detected and Appropriate Corrective Actions are initiated by the ANFIS Controllers. The UPFC Simulated in this paper mainly consists of a 3 level Cascaded H Bridge Inverter. The Sinusoidal Pulse Width Modulation Technique (SPWM) is used .The Advantage with the CHB Inverters is made use of in improving the Performance of the UPFC there by improving the protection levels offered to the Power System Network when the Power System is subjected to certain adverse and abnormal Conditions. One of the most widely used software MATLAB is used for simulating the said test conditions.

III. THE CASCADED H BRIDGE INVERTER

One of the outcomes of the research on the attempt to improving the output voltage of an inverter through Modifying Network/Circuit configurations of an Inverter is the Cascaded H Bridge (CHB) Inverter. The low switching voltage stress and modularity has made the Multi Level Inverters (MLIs) gain more attention. The user desired Multi Level voltage is obtained by using different and separate voltage sources like Batteries, Fuel cells, Solar Photo Voltaic (PV) Cells, Capacitors etc., The major advantages with Multi Level Inverters are their minimum harmonic distortions in the output voltage, Low electromagnetic emissions, high output to input power ratios i.e., high efficiency and more importantly their high voltage withstanding and operating capability and modularity. The multi level inverters have found great applications in the areas of Drive Controls, Uninterruptible Power Suppliers and Static Volt Ampere Reactive Generators (SVG).In general MLIs are divided in to three categories as Diode Clamped, Flying Capacitor and Cascaded Bridge Inverters. One of the advantages of MLIs over the Two Level Inverter is that they reduce the Common Mode Voltage causing the breaking leakage Current in Multi Drive Systems of High Power Ratings (Greater Than 250KW) based Vehicles.

The Circuit Topology of Cascaded H Bridge Inverter

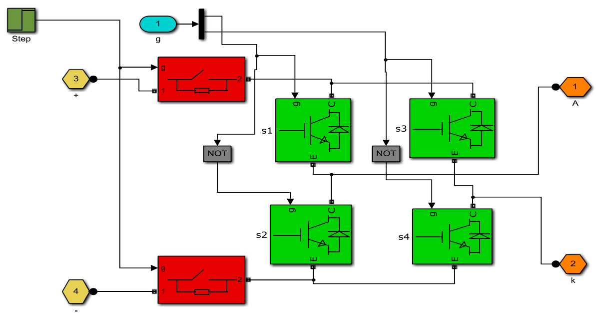

Fig.2. Basic Circuit of a CHB Inverter used in this Simulation

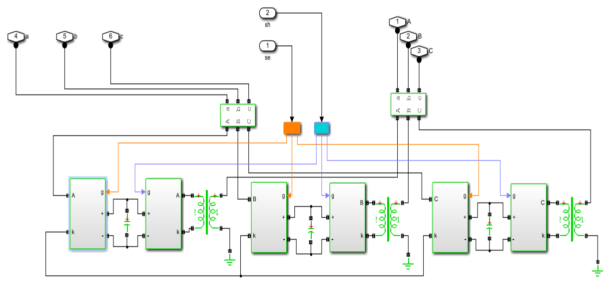

Fig.3. The 3 Level Cascaded H Bridge Inverter used in this Simulation

IV. THE CONTROL SYSTEM

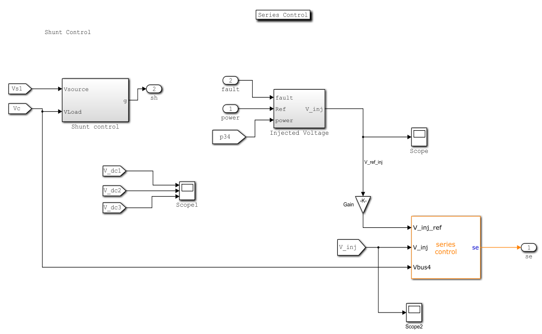

Fig.4. The Central Control System Comprising of the Series and Shunt Controllers including the SPWM Based Pulse Generator

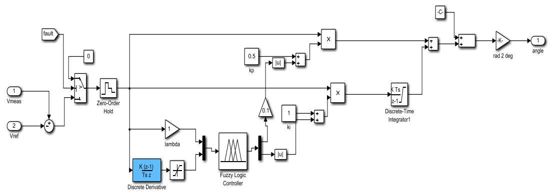

Fig.5. The ANFIS based Shunt Controller

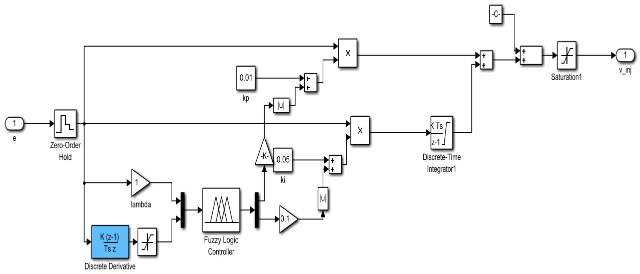

Fig.6. The ANFIS based Series Voltage Injection Controller

IV (a). THE ANFIS CONTROLLER

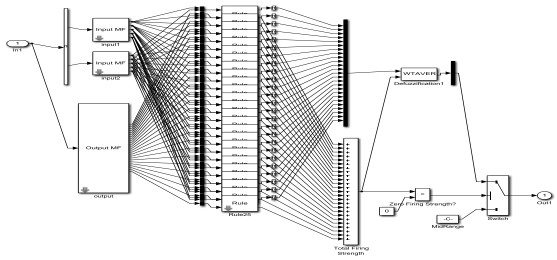

Fig.7. The Internal Structure of the ANFIS Controller

As can be seen from the figures 5,6 and 7 the ANFIS controller is a hybridised controller structure which uses the rules of the fuzzy logic systems and the Artificial Neural Network schemas based learning rules to solve the targeted problem of correction the voltage and powers transferred through the line 3-4. The strength of the fuzzy logic system i.e., the "fuzzy if- then rule" frame is used and appropriate membership functions are designed to map the output and the input system pairs. The (FIS) fuzzy inference systems is a combination of "the rule base, a data base, a decision making unit , a fuzzification interface and a defuzzification interface ", this FIS is grouped with the "adaptive network schemas which is a multilayer feed forward network " to obtain an Adaptive Network Based Fuzzy Inference System, The nodes of the network function perform a specific task , on the incoming signals ,defined as the node function thus making the core controlling system an effective self learning system.The ANFIS controller designed here takes the voltage on the line , power levels (both active and reactive) and their corresponding reference values as inputs and processes to generate the phase angles required to fire the power switches in the converters with appropriate values. This phase angle thus calculated is fed as input to the sinusoidal PWM based pulse generator block, detailed in the figure 8 below, for producing a train of pulses in synchronization with the voltage and current parameters on the line.

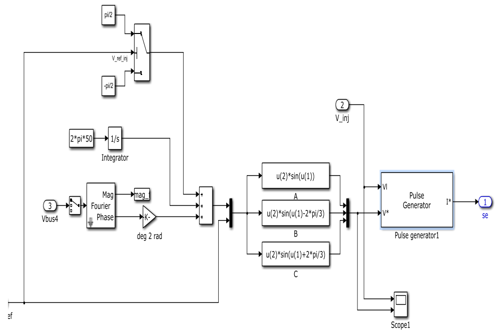

Fig.8. The Sinusoidal PWM Based Pulse Generator.

V. SIMULATED RESULTS AND DISCSSIONS

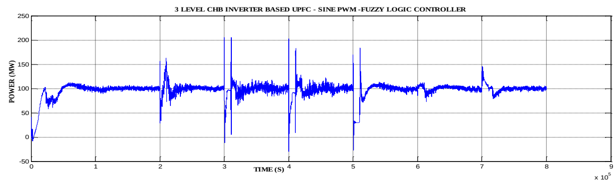

Fig.9(a). The Complete Power Transferred through the Line 3-4 under different test conditions using ANFIS Controller

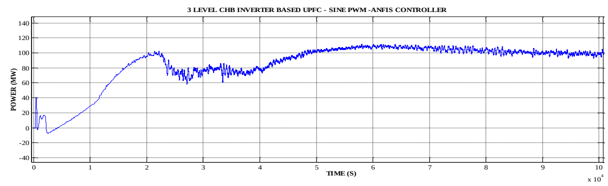

Fig 9(b) The Initial Power Swing of the Generator

Figure 9 (a) indicates the Power transferred through the line 3-4 during the entire test period of the ANFIS Controller based UPFC and figure 9 (b) details the time taken by the power wave in the line 3-4 to reach the targeted power value of 250MW from the initial start up conditions. It can be seen that the time taken to reach the 250MW stable margin is only 3s.

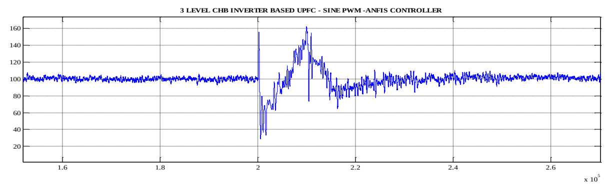

Fig.10. Power transferred through the line during LG Fault with an ANFIS Controller

An LG fault is created near bus number 4 in the line 3-4 .the duration of the fault is 0.5s and the time taken by the system to restore the 250MW rated value is only 1second.

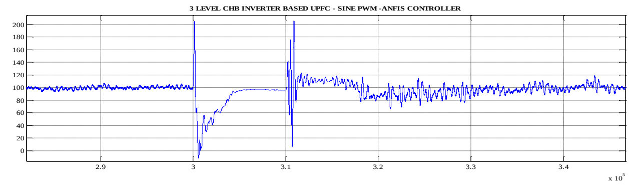

Fig.11. Power transferred through the line during LL Fault with an ANFIS Controller

In figure 11, an LL fault is created between the phases "a-b" to test the capability of the controller in supporting the transmission system to restore to its normalcy .The ANFIS controller based UPFC helps the system to regain normalcy within a span of 0.8s.

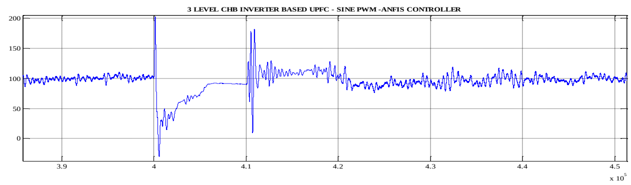

Fig.12. Power transferred through the line during LLG Fault with an ANFIS Controller

Figure 12 details the situation where the line 3-4 is subjected to a LLG fault i.e., between "phase a - phase b-ground" for a duration of 0.5 s the time taken by the system to restore normalcy / rated power of 250MW is 0.7s.

Very similar to the conditions stated above , to test the capabilities of the ANFIS controller based UPFC , a LLL fault is created between the phases "a-b-c" for a duration of 0.5 s.It can be observed from figure 13 below that the time taken by the system to regain original state of power transfer is 0.9 s.

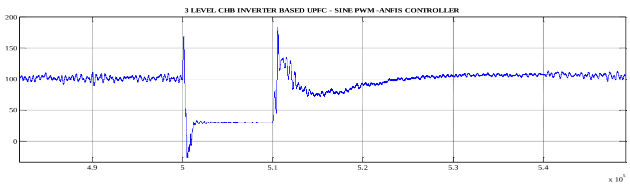

Fig.13. Power Transferred Through the line during LLL Fault with an ANFIS Controller

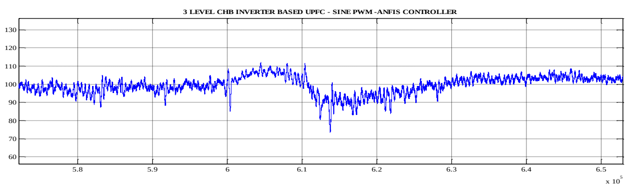

Fig.14. Power Transferred Through the line during Sag i.e., INDUCTIVE LOADING, with an ANFIS Controller

Figure 14 illustrates the capacity of the UPFC to support the transmission network in times of inductive overloading wherein an extra of 45MW of inductive load is added to the line 3-4 at bus number 4.As soon as the load is initiated/attached to the bus 4 the system undergoes a sudden decrease of voltage i.e., sag and the power transferred thereby suddenly decreases.The ANFIS controller based UPFC senses the change in values and initiates for corrective action in such a way that the voltage generated by the series converter with an appropriate phase angle which the alleviates the voltages to the rated values and restores the system power transferred to normalcy. The time taken by the system to reach the rated values from the voltage sag conditions is only 1 second.

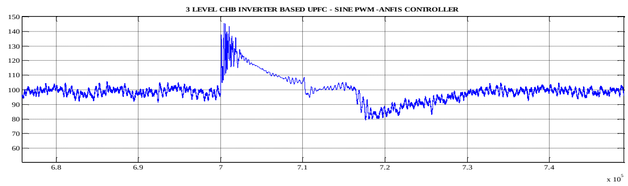

Fig.15. Control of Power Transferred through the line during voltage swell i.e., capacitive overloading with an ANFIS Controller

A contradicting condition to the one specified in figure14 is now explained with reference to figure15. A capacitive load of 45MVAR is added to the bus number 4 in line 3-4 .The sudden switching of an extra load of 45MVAR capacitive makes the voltage levels and the power levels to rise suddenly. This incremental change is sensed by the ANFIS controller based UPFC and corrective action of voltage absorption or reactive power compensation is initiated and the system voltage levels and power levels are restored to normalcy within a period of 0.9s.

RESULTS TABULATION

Table 1

S.No	Type of Disturbance	Duration of Disturbance in Seconds	Settling Time in Seconds ANFIS CONTROLLER
1	Voltage Sag	0.5 (30 to 30.5)	1.0
2	Voltage Swell	0.5 (35 to 35.5)	0.9
3	Line to Ground Fault	0.5 (10 to 10.5)	0.8
4	Line to Line Fault	0.5 (15 to 15.5)	0.9
5	Line to Line to Ground Fault	0.5 (20 to 20.5)	0.7
6	Three Phase Faults	0.5 (25 to 25.5)	0.9

VI. CONCLUSIONS

It can be concluded that the UPFC embedded with an ANFIS controller has a faster response rate. This Phenomenon can be observed from the fact that the Settling Time for restoration of normalcy during the occurrence of different kinds of disturbances, like Voltage Sag, Voltage Swell or Faults like LG, LL, LLG, and LLL as depicted in the Table 1 , is less.

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APPENDIX

IEEE-5 Bus System

NUMBER OF LINES = 7
NUMBER OF BUSES = 5

In all these BUS DATA's type-3 indicates slack bus, type-2 indicates PQ / load bus, type-1 indicates PV / generator bus.

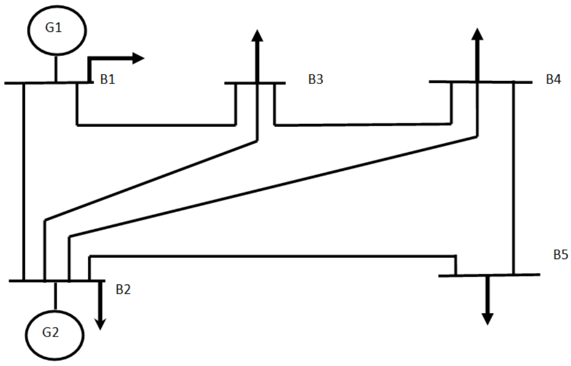

Figure: Single Line Diagram of the IEEE 5 Bus System

LINE DATA

SB	EB	R (p.u)	X (p.u)	Ys	Tap
1	2	0.02	0.06	0.03	1
1	3	0.08	0.24	0.025	1
2	3	0.06	0.18	0.02	1
2	4	0.06	0.18	0.02	1
2	5	0.04	0.12	0.015	1
3	4	0.01	0.03	0.01	1
4	5	0.08	0.24	0.025	1

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