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Interfacing Of PS/2 Mouse and VGA Monitor Using FPGA

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Abstract:
In this paper VGA (Video Graphics Array) monitor and PS/2(Personal System) Mouse are interfaced with BASYS3 FPGA board for moving objects like square and ball. VHDL (very High Speed Integrated circuit Hardware Description Language) language is used to design and develop for interfacing PS/2 mouse and VGA monitor. FPGA (Field Programmable Gate Array) switches are used to choose to draw a square and ball shape in the VGA monitor. Mouse left click, right click and movement of mouse are used to move the objects square and ball either in left, right, bottom and top positions in the VGA monitor. 8 bit data output of mouse are displayed using FPGA LEDs. Mouse left click, right click and movement of mouse are shown on FPGA board using 8 FPGA LEDs. Xilinx Vivado 2015.2 tool is used to interface PS/2 mouse and VGA monitor interface. We can use this prototype for detecting robot movement in two dimensional axes, developing any game by using shapes like square and ball.

Keywords: FPGA, VHDL, PS/2 Mouse, VGA, Square, Ball

I. INTRODUCTION

Research and development for a specific task are increasing day by day nowadays. Video processing is gaining importance in many fields such as ATM machines, video conferencing, and video surveillance systems [1]. Previously, video processing required high computational work with computers and standard processors but to meet the demand of smaller size equipment with less power consumption specialized hardware equipment are evolved such as digital signal processing kits(DSP) or field programmable gate arrays(FPGA)[2].

The applications developed using FPGA's have shown noteworthy speedups compared with software and DSP based approaches for several video processing applications. FPGA based systems have better expandability, provides an impacted size, have higher performance and also achieve low power consumption. FPGA also have other advantages over these platforms, these advantages are: high clock frequency, high operations per second, code portability, code libraries reusability, low cost, parallel processing, capability of interfacing with high or lower interfaces, security, and Intellectual property (IP) retention. Only the emerging of FPGA technology made VGA controller design accessible and suitable for study, experimentation, and research [3]. Video Graphics Array (VGA) is a high-resolution video standard used mostly for computer monitors, where ability to transmit a sharp, detailed image is essential [4]. Video graphics array controller is used as a logic circuit which control the VGA interface.

In this paper FPGA is used as the core of hardware circuit, which is responsible for the VGA display, we are showing interface of PS/2 mouse and VGA monitor with Artix7 FPGA Board and the movement of mouse are shown by using circle and ball shapes on the VGA screen. VGA controller can be developed by using VHDL(HARDWARE DISCRIPTION LANGUAGE) based in IEEE standards to ensure the portability with any manufacturer.

II. DESIGN AND DEVELOPMENT FOR INTERFACING PS/2 MOUSE WITH VGA USING FPGA

VHDL language is used to design different modules for interfacing of PS/2 mouse and VGA with Artix7 FPGA board [5]. 7LEDs are used to display the movement of PS/2 mouse. VGA monitor is used to display movement of ball and square when mouse is either clicked or scrolled. Detailed discussion of used PS/2 mouse is given below.

2.1 PS/2 MOUSE

PS/2 mouse is commonly used input device to connect the computer as pointing device. The main is to interface PS/2 mouse with Artix-7 Basys3 FPGA. Here in this project we designed a bidirectional mouse interface, where FPGA controls all the functions, from taking the commands from mouse to providing the information of protocol functioning using LEDs. We have displayed left scrolling, right scrolling and button clicks on the onboard FPGA.

2.1.1 OPERATION OF MOUSE

The mouse when moved it outputs a clock and data signals; Each time when it is moved, it sends three data packets to host, in which each data packet is of 11-bits. This 11-bit data packet contains a '0' start bit, 8 data bit, an odd parity bit, and terminated with a '1' stop bit. Each transmission contains of total 33 bits.

In these 11-bit packet, the 8-bit byte in this case Y7 down to Y0 & X7 down to X0 these corresponds to the Y and X velocity of the mouse, so if you move the mouse back and forth in the horizontal direction you will get an X-velocity measurement and if you move it up and down you get a Y-velocity measured. Fig.2.1 represents operation of mouse in 33-but data format.

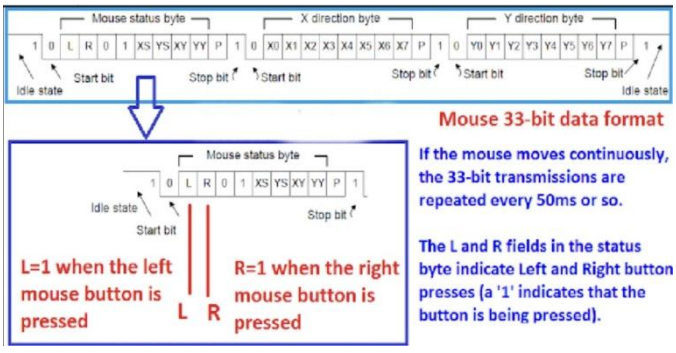

Figure 2.1: Operation of mouse in 33-bit data format

There can be signed numbers depending upon which direction you are moving, which is determined by these two signed bits XS and YS.
If we move our mouse fast then you get an overflow bit set in status byte which are XV(overflow bit for X) and YV(overflow bit for Y).
Finally the two bits R and L will tell you which button we are pressing, if we are pressing the right button then R=1, and if we are pressing the left button then L=1.

2.2 **INTERFACING PS/2 MOUSE WITH FPGA**

On board Microcontroller(PIC24FJ124) allows Basys 3 FPGA to have USB HID hist capability. Once the FPGA is programmed, which can interface the FPGA with a mouse connected to the USB type-A connector (J2).

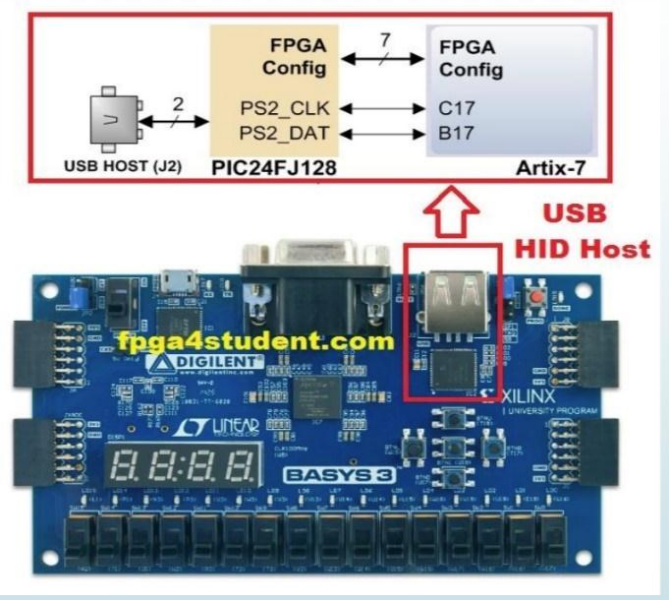

Figure 2.2: FPGA diagram for mouse interface

The microcontrollers PS2_CLK and PS2_DAT signals are used to implement a PS/2 interface for communication with a mouse. PS/2 device always generates the clock signal. If the host wants to sends data, it must first put the clock and data lines in a "Request to sends" state. Timing diagram for mouse interface with FPGA board is shown in Fig2.3.

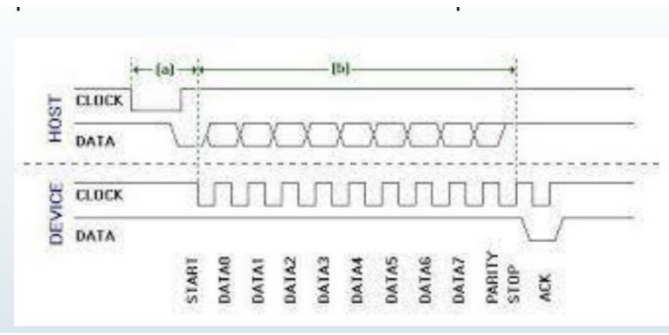

Figure 2.3: Timing diagram for mouse interface with FPGA

When the device detects this state. It will begin generating clock signals and clock in eight data bits and one stop bit. The host changes the data line only when the clock line is low, and data is ready by the device when clock is high.
After the stop bit is received, the device will acknowledge the received byte by bringing the data line low generating one last clock pulse

III. EXPERIMENTAL RESULTS FOR THE INTERFACED PS/2 MOUSE WITH VGA

The designed VGA controller is implemented on our FPGA using Vivado 2015.2. design suite. Two type of shaped structures ball and squares are designed using VHDL and implemented on Artix7 FPGA board[6] for displaying them on VGA monitor[7]. Initially ball ia located at x-position=300, and y-position=300. And when the mouse is either clcked or scrolled then it moved in VGA monitor in either upward, downwards, left wards and right ward movements. The radius of ball is 5. Initially square is located at x-position=400, and y-position=400. And when the mouse is either clcked or scrolled then it moved in VGA monitor in either upward, downwards, left wards and right ward movements. The length and width of the square is 50.A predefined constant value is added to x&y position of square and ball if mouse is either right clicked, left clicked or scrolled. Fig 3.1 represents complete experimental setup diagram for the interfacing PS/2 mouse and VGA using Artix7 FPGA board. Fig 3.2 represents FPGA diagram when mouse is right clicked and LED(7) is ON in this case. Fig 3.3 represents FPGA diagram when mouse is left clicked and LED(0) is ON in this case. Fig 3.4 represents FPGA diagram when mouse is scrolled and LED(1-6) will be ON in this case.
A ball of radius 5 is displayed on VGA monitor by interfacing VGA with FPGA board is shown in Fig 3.5. A square of length and width of 50 is displayed on VGA monitor as shown in Fig 3.6. in Fig 3.7 represents ball and a square movement in VGA monitor when mouse is left clicked in this case a predefined constant value is added to x positions of ball and square from their x positions values. Fig 3.8 represents movement of ball and square in VGA monitor when mouse is scrolled. Fig 3.9 represents ball and a square movement in VGA monitor when mouse is right clicked in this case a predefined constant value is added to y positions of ball and square from their y positions values. Fig 3.10 represents RTL Schematic diagram for the implemented protype for interfacing PS/2 mouse and VGA monitor. Table 3.1 represents synthesis results for interfacing PS/2 mouse and VGA monitor by using Artix7 FPGA board. Table 3.2 shows total on chip power consumption and delay for the implemented system to interface PS/2 mouse and VGA monitor.

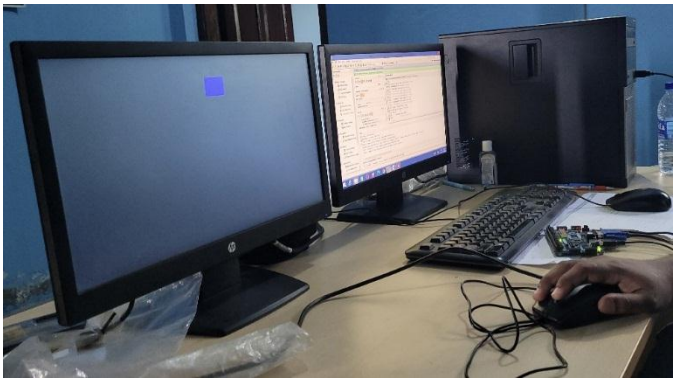

Figure 3.1: Experimental setup diagram for interfacing PS/2 mouse with Artix7 FPGA board

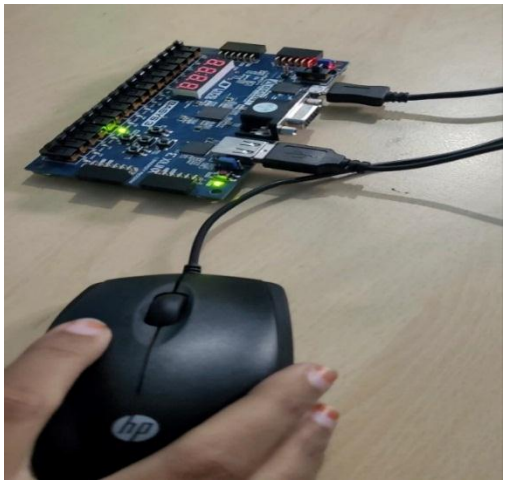

Figure 3.2 Mouse interface with Artix7 FPGA board for left click

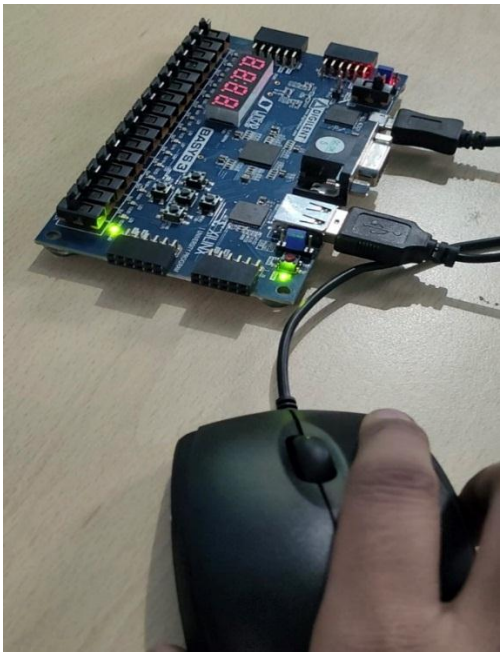

Figure 3.3 Mouse interface with Artix7 FPGA board for right click

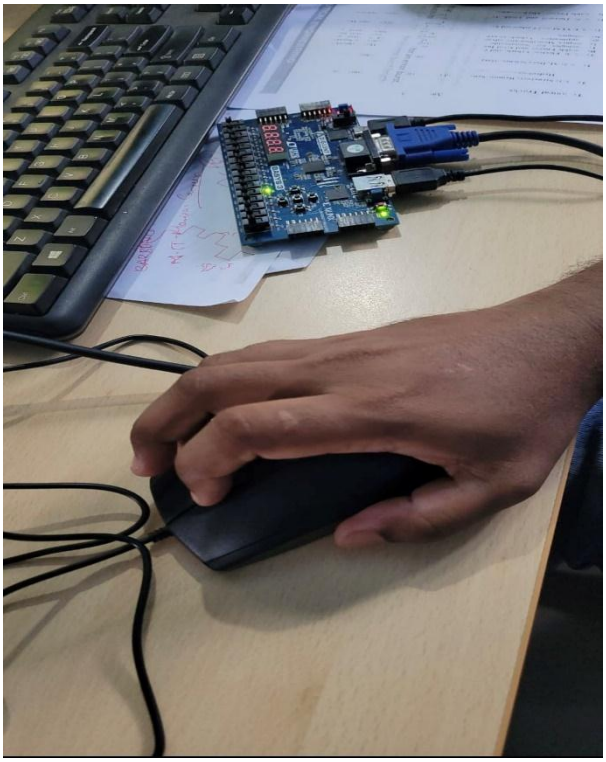

Figure 3.4: Mouse interface with Artix7 FPGA board for scroll

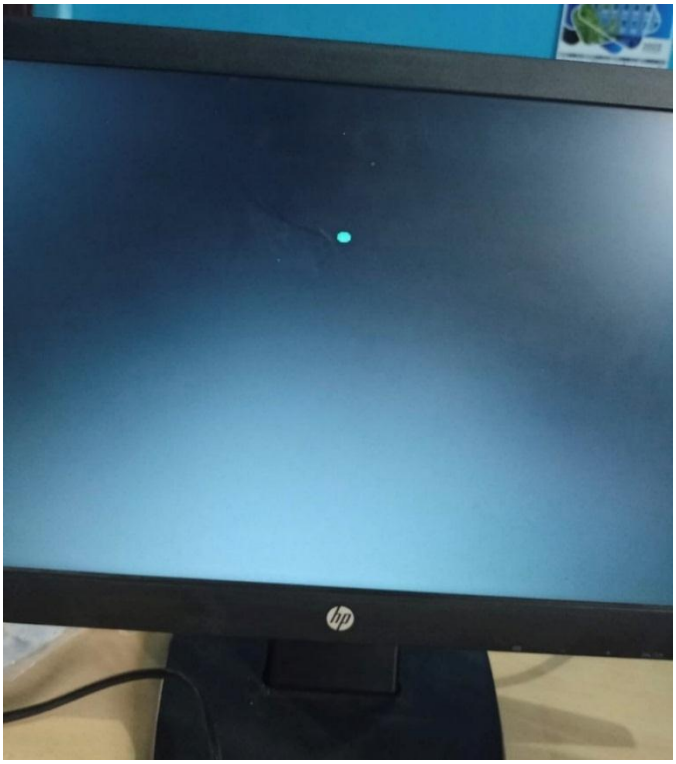

Figure 3.5: VGA monitor output for displaying ball

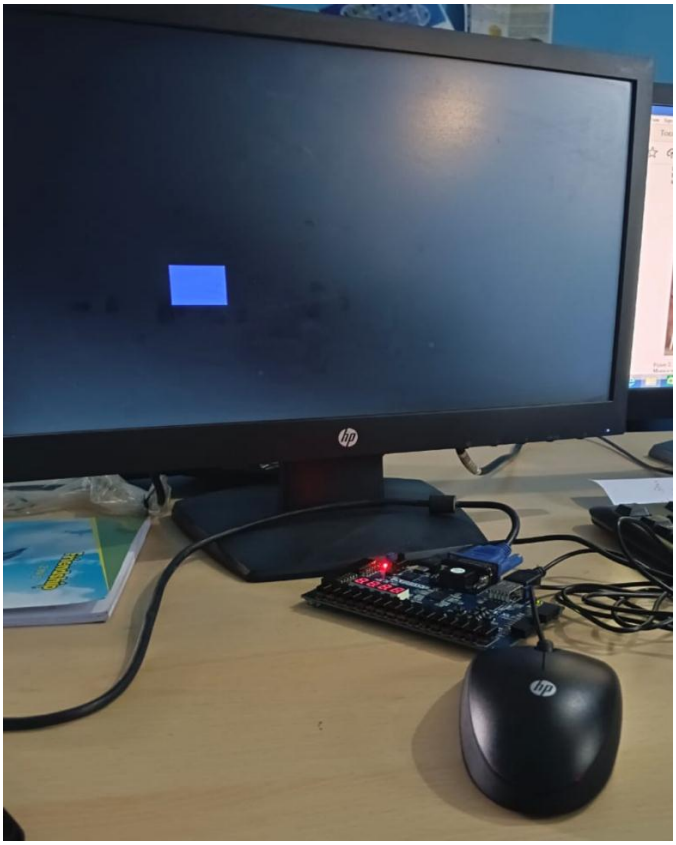

Figure 3.6: VGA monitor output for displaying square

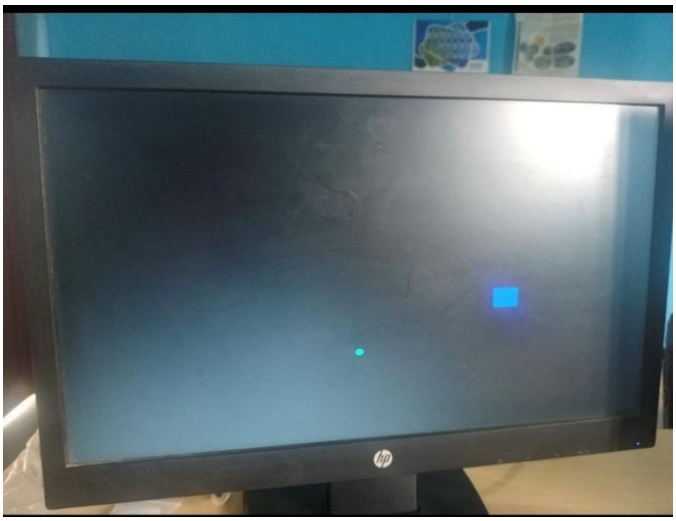

Figure 3.7: VGA monitor output when mouse is left clicked.

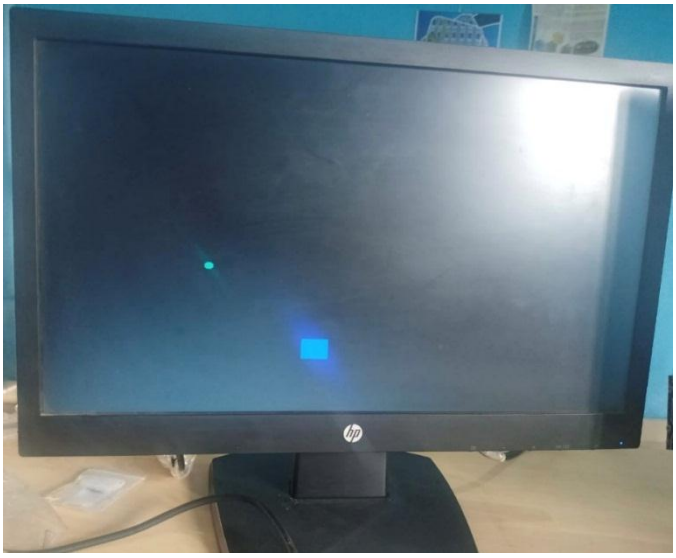

Figure 3.: VGA monitor output when mouse is scrolled

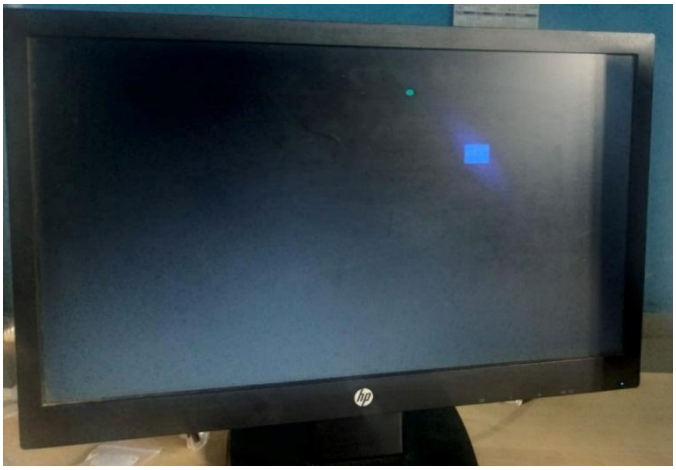

Figure 3.9: VGA monitor output when mouse is right clicked for upward movement.

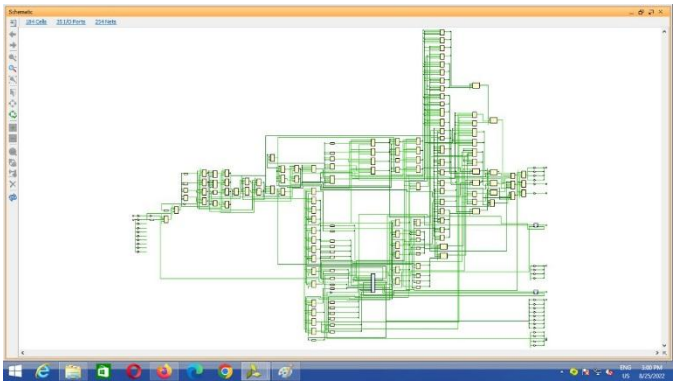

Figure 3.10: RTL Schematic diagram for the implemented protype for interfacing PS/2 mouse and VGA monitor

Table 3.1: Synthesis Results for the implemented prototype for interfacing PS/2 mouse and VGA monitor

Resource	Utilization	Available	Utilization %
FF	125	41600	0.30
LUT	173	20800	0.83
I/O	35	106	33.02
BUFG	2	32	6.25

Table 3.2: Delay and Power consumption results for interfacing PS/2 Mouse and VGA

	Power consumption(watt)	Delay(ns)
Proposed work	0.097 W	6.173

IV. CONCLUSION

In this paper experimental outputs are shown in VGA monitor for displaying movement of ball and square either in left, right, upward and downward movement. Movement of ball and square is controlled by mouse by clicking or scrolling. Total 173 LUTs and 125 FFs are utilized for implementing this system. Total on chip power consumption is 0.097W and delay is 6.173ns for interfacing ps/2 mouse and VGA monitor with FPGA. In future we can use this prototype to design any game or we can use in determining the position of robot.

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