International Journal of Computational Intelligence Research
ISSN 0973-1873 Volume 13, Number 5 (2017), pp. 841-849

http://www.ripublication.com

Designing of All Optical Two Bits Full Adder using TOAD, TMIN and Feynman Gate

Chinmoy Taraphdar
Bankura Christian College, Bankura, West Bengal, India.

Abstract

Now a day's Multi-valued logic (MVL) in the field of nonlinear optics is also positioned as a coming generation technology of Optical computing that can execute arithmetic functions faster and with less interconnects than binary logic. As photon is the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronics computing. In this domain of Optical computing which is constructed in the platform of Non Linear Optics (NLO), we have design all optical single full adder by using combination of a TOAD (Terahertz Optical Asymmetric Demultiplexer which is an ultrafast all-optical switch) based Ternary MIN Gate and Mach-Zehnder interferometer (MZI) based Feynman Gate where one of the three inputs is carried from the output of another all optical Half Adder, for photonic logic based information processing scheme in three-valued and reversible logic domain.

Keywords: Beam Combiner, Feynman Gate, MZI, TOAD, TMIN Gate

1. Introduction

A two bits full adder is a combination of a half adder and a single bits full adder. Basically in the logical operation of this two bits full adder, the operation of single bits full adder in 2nd stage will be guided by the operation of half adder in first stage. More clearly if we want to add A_1B_1 with A_2B_2 when each of them is binary byte then the addition will be like $A_2A_1 + B_2B_1 = C_2S_2S_1$where the whole operation is followed by the steps $A_1 + B_1 = C_1S_1$, $C_1 + B_2 = C_2S_o$, $S_o + A_2 = S_2$, and final the result will becomes $C_2S_2S_1$. So we see that the carry from the previous half adder operation will be carried out to one of the three inputs of the second stage single bits full adder and

finally we get the result after the operation of second stage single bits full adder operation.

Thus we see that the logical operation of a two bits full adder is performed on the basis of the operation of 1st stage half adder and then 2nd stage single bits full adder. A logic circuits with two inputs and two outputs that can add two binary digits at a time, producing a sum and a carry, is called a half adder. The addition process of two bits is shown in the form of a truth table [Table-1] where A (addend) and B (augend) are the two inputs, S (sum) and C (carry) are the two outputs.

Table 1: Truth Table of a Half Adder

A	B	S	C
0	**0**	**0**	**0**
1	**0**	**1**	**0**
0	**1**	**1**	**0**
1	**1**	**0**	**1**

On the other hand, a logic circuit with three inputs and two outputs that can add two binary digits at a time in the next stage with a third input carried from the carry output of previous half adder, producing a sum and a carry, is called a single bits full adder. This addition process of two bits is shown in the form of a truth table [Table-2] where A and B are the two inputs, C_{IN} is the 3rd input carried from the output 'Carry' from the previous half adder operation, S (sum) and C_{OUT} (carry) are the two outputs.

Table 2: Truth Table of a Single Bits Full Adder

A	B	C_{IN}	S	C_{OUT}
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**0**
0	**1**	**0**	**1**	**0**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**1**
1	**1**	**0**	**0**	**1**
1	**1**	**1**	**1**	**1**

Though the implementation of larger logic diagrams is possible with the above half adder and single bits full adder combined logic, a simpler schematic representation which is mostly used to represent the operation of two bits full adder is shown in Fig-1.

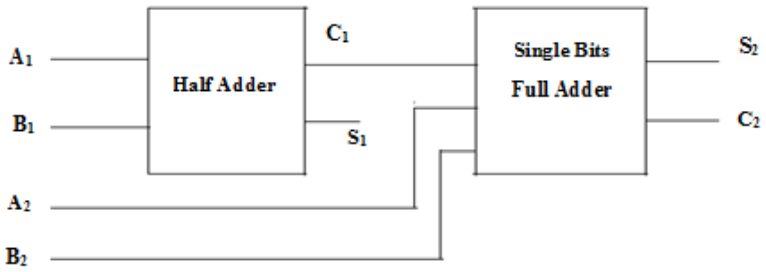

Fig-1: Block Diagram of a two bits Full Adder

In this work, all optical model of this two bits full adder is designed by taking the combination of four TOADs in first stage half adder and two Ternary MIN gates along with two MZI based Feynman Gates in second stage single bits full adder in addition with a few beam combiners (BC). Also in this design, the optical version of two binary digits 0 and 1 are considered as 0 → 'No Light' and 1 → 'Vertically Polarized Light'

2. TOAD based optical switch

TOAD is a device capable of demultiplexing Tb/s pulse trains that requires less than 1 pJ of switching energy. For proper operation of the TOAD as a demultiplexer, the timing between the control and signal pulses is critical. Assuming the NLE [2] (non-linear optical element) is located such that the clockwise signal pulse reaches it first, the control pulse must pass through the NLE after the clockwise signal pulse but before the counterclockwise signal pulse. If this happens, the clockwise signal pulse experiences the unsaturated gain of the amplifier, whereas the counterclockwise pulse sees the saturated gain. The latter also experiences an additional phase shift that arises due to gain saturation. Because of this asymmetry, the two halves of the signal pulse [5] do not completely destructively interfere with each other, and a part of the signal pulse emerges from the input coupler. Note that along with the signal pulse, the control pulse will also be present at the output. Another advantage of the TOAD [4] is that because of the short length of the fiber loop, the polarization state of the pulses is maintained even if standard single-mode fiber (nonpolarization-maintaining) is used. If the fiber loop is long, it must be constructed using polarization-maintaining fiber.

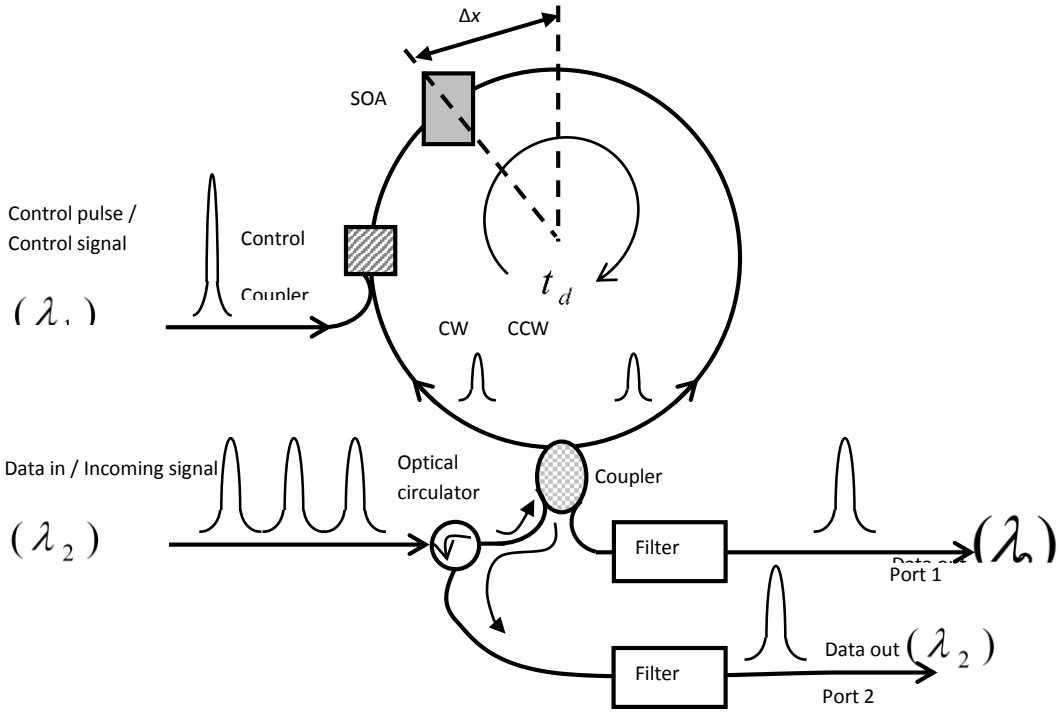

Fig-2: A TOAD based optical switch, where SOA: Semiconductor optical amplifier, CW: Clockwise pulse, CCW: Counterclockwise pulse, t_d : pulse trip time, Δx: Asymmetric distance.

The TOAD consists of a loop mirror with an additional, intra-loop 2 × 2 (ideally 50:50) coupler. The loop contains a control pulse (CP) of different wavelength than that of incoming pulse and a semiconductor optical amplifier (SOA) [3] that is offset from the loop's midpoint by a distance Δx as shown in Fig-2. A clock pulse enters the loop through the 3-dB coupler and is split into two counter-propagating pulses, the clockwise (CW) and counter clockwise (CCW). In the absence of a control signal, incoming signals enter the fiber loop, pass through the SOA at different times as they counter-propagate around the loop, and recombine interferometrically at the coupler. Since both signals see the same medium as they propagate around the loop, the data is reflected back toward the source. When a synchronized control pulse of different wavelength is injected into the loop, it saturates the SOA and as a consequence its refractive index and gain, can be altered so that a phase shift equal to π is induced between the CW and CCW pulses, which recombine constructively at the transmission port of the switch.

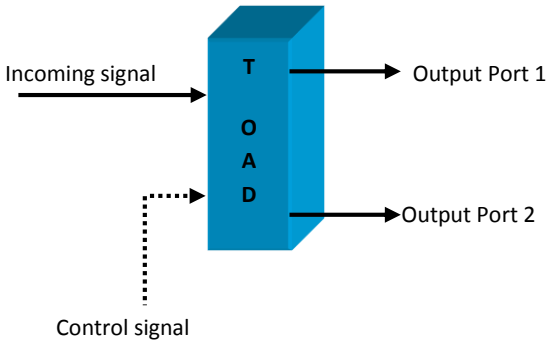

Fig-3: Schematic diagram of TOAD based optical switch

A schematic block diagram block [1] of TOAD based switch is shown in Fig- 2. The truth table of Fig- 2 is given in Table 3.

Table 3: Truth Table for TOAD

Incoming Signal	Control Signal	Output Port-1	Output Port-2
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

2. All-optical Two Inputs Ternary MIN Gate

Ternary MIN gate is equivalent AND gate in binary world. It is an important multi-valued logic function. The TMIN operation [6, 7] is given by $\mathrm{TMIN}(X, Y) = Y$ if $Y \leq X$

Table 4: Truth table of TMIN(X,Y) function

Y \ X	0	1	2
0	0	0	0
1	0	1	1
2	0	1	2

3. MZI based Feynman Gate

Feynman gate is a (2*2) one-through reversible logic gate. It has two inputs (A, B) and two outputs (X, Y) satisfy the relation as follows: $X = A$

$$Y = A \oplus B$$

Table 5: Truth table of Feynman Gate

Inputs		Outputs	
A	B	X	Y
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

And also block diagram of MZI (Mach-Zehnder Interferometer) based all optical reversible Feynman gate is given in Fig-4.

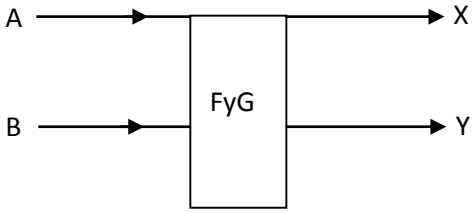

Fig-4: Block Diagram of Feynman Gate (FyG).

4. Design of All Optical Two Bits Full Adder by using TOAD, TMIN and Feynman Gate

Apart from the design of binary circuit for the logical operation of two bits full adder, here the design of all optical circuit for the logical operation is made by considering two bits 0 as no light signal and 1 as a vertically polarized light when applied at the inputs of both 1st stage half adder and 2nd stage single bits full adder. In this theoretical design, two inputs A_1 and B_1 are considered for 1st stage all optical half adder which gives two outputs C_1 and S_1. This carry out put C_1 is then fed back to one of three inputs of 2nd stage all optical single bits full adder which with other two inputs A_2 and B_2 gives two outputs C_2 and S_2 . Finally we get the total output $C_2S_2S_1$ from this all optical two bits full adder.

4.1. All Optical Logic Diagram for the Operation

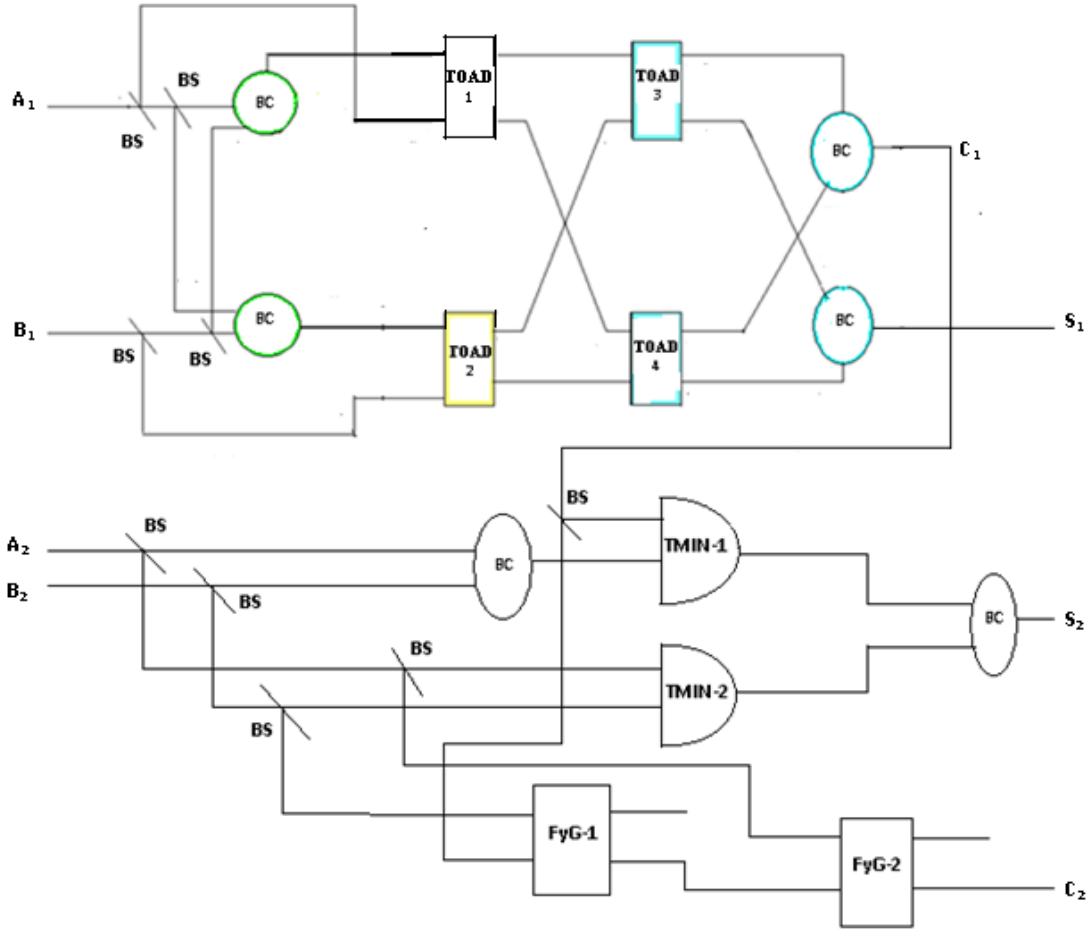

Fig-5: Logic Circuit for All Optical Two Bits Full Adder

4.2. Truth Table for Logical Operation

1st Stage Half Adder					2nd Stage Single Bits Full Adder					Result of Two Bits Full Adder
A_1	B_1	C_1	S_1		C_1	A_2	B_2	C_2	S_2	$C_2S_2S_1$
0	0	0	0		0	0	0	0	0	000
1	0	0	1		0	0	0	0	0	001

0	**0**	**0**	**0**		**0**	**1**	**0**	**0**	**1**	**010**
1	**0**	**0**	**1**		**0**	**1**	**0**	**0**	**1**	**011**
0	**1**	**0**	**1**		**0**	**0**	**0**	**0**	**0**	**001**
0	**0**	**0**	**0**		**0**	**0**	**1**	**0**	**1**	**010**
0	**1**	**0**	**1**		**0**	**0**	**1**	**0**	**1**	**011**
0	**1**	**0**	**1**		**0**	**1**	**0**	**0**	**1**	**011**
1	**1**	**1**	**0**		**1**	**0**	**0**	**0**	**1**	**010**
0	**0**	**0**	**0**		**0**	**1**	**1**	**1**	**0**	**100**
1	**1**	**1**	**0**		**1**	**1**	**1**	**1**	**1**	**110**

5. Conclusion

Similar to this work, different all-optical circuits can be presented in the domain of both two and three-valued and reversible logic system. Polarization encoded all-optical schemes of several binary logic gate can be developed and there is a future scope of Ternary addition in this manner where ternary numbers (0, 1, 2) are used by representing three discrete polarized state of light which are no light (0), vertically polarized light (1) and horizontally polarized light (2) respectively. The main building block in the different architectures is the TOAD based all-optical switch as it is a very promising candidate to implement all-optical logic gates because of its advantages of low energy requirements, compactness, high ER, regenerative capability and low chirp. Presence and absence of light have been taken as two logic states in designing of all-optical logic gate.

REFERENCES

1. J. Hardy and J. Shamir, "Optics inspired logic architecture", Optics Express, 15(1), (2007). Pp.150-165
2. G. P. Agarwal, Applications of nonlinear fiber optics (Academic press, India [an imprint of Elsevier, San Diego, USA, 2001]) Chapter 3.
3. T. Houbavlis and K. E. Zoiros, "Ultrafast pattern-operated all-optical Boolean XOR with semiconductor optical amplifier-assisted Sagnac switch," Optical Engineering, 42(12), (2003).pp. 3415-3416
4. D. K. Gayen and J. N. Roy, "All-optical arithmetic unit with the help of terahertz optical asymmetric demultiplexer (TOAD) based tree architecture", Applied Optics, 47(7), (2008). Pp. 933-943
5. Abhijit Sinha, Harihar Bhowmik, Puspendu Kuila, and Souranshu Mukhopadhyay, "New method of controlling the power of a Gaussian optical

pulse through an electro-optic modulator and a nonlinear waveguide for generation of soliton", Opt. Eng. Vol. 44(6), (2005).pp. 065003

6. C.Taraphdar, T. Chattopadhyay and J.N.Roy "Designing of an all-optical scheme for single input Ternary logical operations" Optik. Int.J. Light Electron. Opt 122(1) (2011) [Publisher: Elsevier].pp. 33-36
7. G.K.Maity,T. Chattopadhyay ,D.K.Gayen, C.Taraphdar, A.K.Maiti, S.P.Maity and J.N.Roy "All-optical Binary Flip-Flop with the help of Terahertz Optical Asymmetric Demultiplexer" Natural Computing 9 (4) (2010) [Publisher: Springer]pp. 903-916