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Design of an Accurate High Speed Carry Select Adder Using Encoder

Shaik Shakeelabi[1] *M.tech – Scholar*

Mohammed Nayeemuddin[2] *Assistant Professor*

R Sambasiva Nayak[3] *HOD*

[1,2,3]Department of E.C.E, Sri Chundi Ranganayakulu Engineering College Ganapavaram (Po), Nadendla (Md) Near Chilakaluripet, Guntur, Andhra Pradesh 522619, India.

Abstract

In this paper, Carry Select Adder (CSA) architectures are proposed using parallel adders. Instead of using dual Ripple Carry Adders (RCA) we design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit modified Linear CSA are designed. Memory used and delay of all these adder architectures are calculated at different input.

Keywords- Ripple Carry Adder (RCA), Regular Linear Carry Select Adder, Modified Linear Carry Select Adder.

I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IIR Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder is designed using dual Ripple Carry Adders and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by Decoder. As, RCA (for Cin= 0) and Decoder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced. Also the CSA are designed using Decoder in order to reduce the power and delay of adder. In this paper, Modified Carry select Adder using Decoder is proposed using single Decoder and BEC instead of dual RCAs in order to reduce the power consumption with small penalty in speed.

II. CARRY SKIP ADDER:

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented.

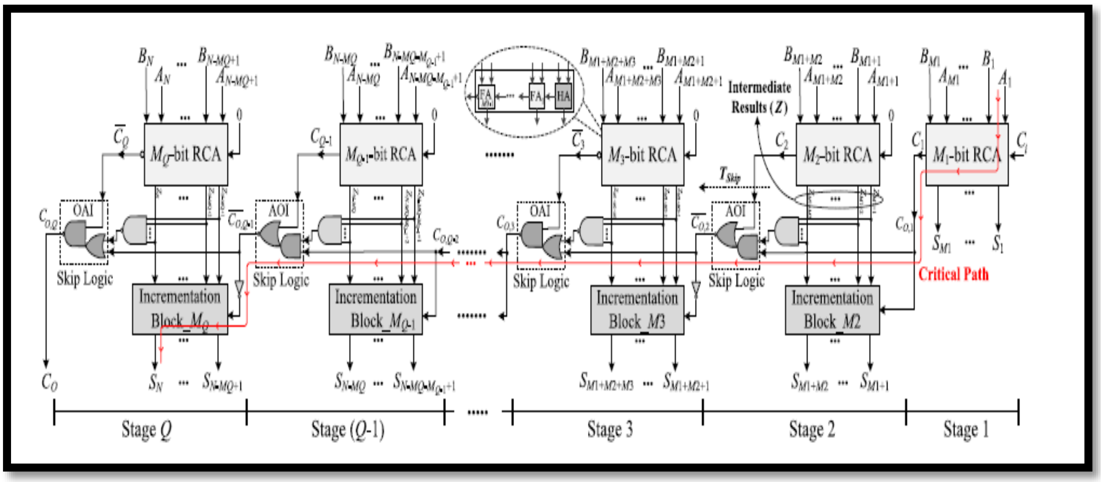

FIG. 1 CARRY SKIP ADDER

Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths). Now, we describe the internal structure of the proposed CI-CSKA shown in Fig. 1 in more detail. The adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size of Mj (j = 1, . . . , Q). In this structure, the carry input of all the RCA blocks, except for the first block which is Ci is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously.

III. CARRY SELECT ADDER SYSTEM

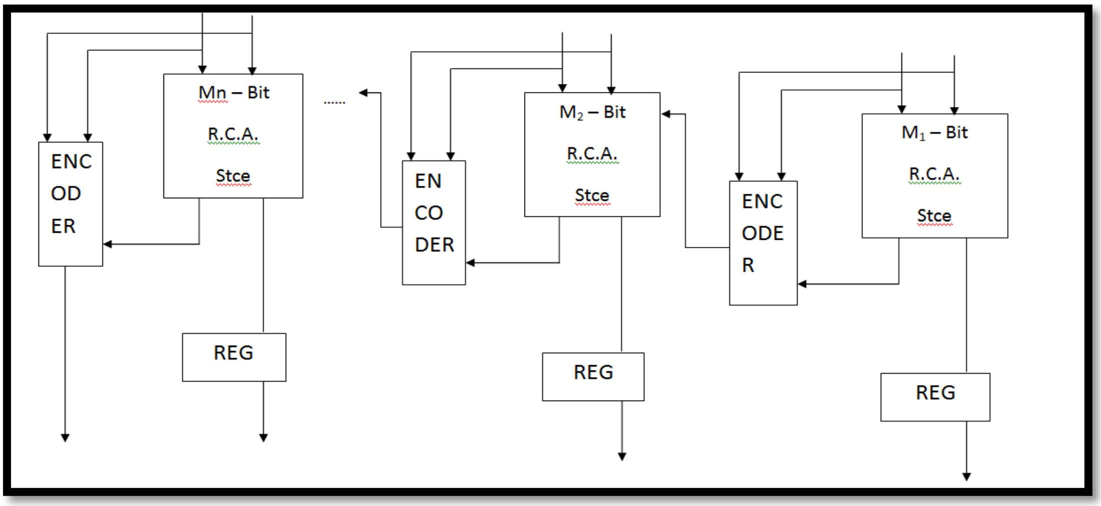

Fig. 2 CARRY SELECT ADDER SYSTEM

The total proposed system is depends on R.C.A Slice and encoder blocks. The register block is used to store the output. The R.C.A slide done the operations of generator and propagator along with sum generation. The encoder is used for carry generation and it is given to next RCA slice.

MUX based Register: A register consists of cascading a negative latch (master stage) with a positive one (slave stage). Fig. 1 shows a multiplexer-latch based implementation of register. On the low phase of the clock, the master stage is transparent, and the D input is passed to the master stage output, Q_M.

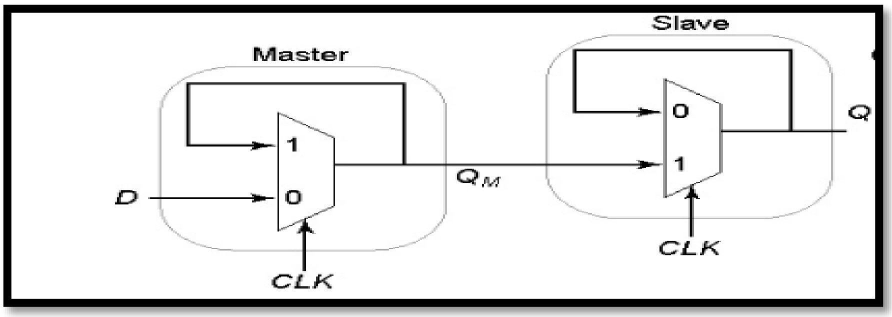

FIG 3 REGISTER BASED ON CONDITION

During this period, the slave stage is in the hold mode, keeping its previous value by using feedback. On the rising edge of the clock, the master stage stops sampling the input, and the slave stage starts sampling. During the high phase of the clock, the slave stage samples the output of the master stage (Q_M), while the master stage remains in a hold mode. Since Q_M is constant during the high phase of the clock, the output Q makes only one transition per cycle. The value of Q is the value of D right before the rising edge of the clock, achieving the positive edge-triggered effect.

IV. RESULTS

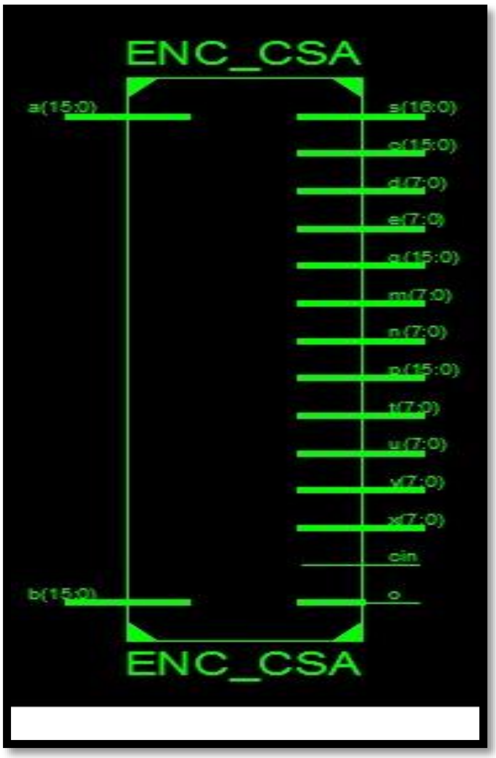

FIG 4 RTL SCHEMATIC

FIG 5 OUTPUT WAVEFORM

The CSLA has been developed using gate-level modification to significantly reduce the delay and increase the speed. This is implemented in VHDL using XILINX14.2 ISE tool and the results are compared in terms of accuracy and speed.

V. CONCLUSIONS:

In this work, a Modified Carry Select Adder is proposed which is designed using single Decoder for Cin=O and Ripple Carry Adder for Cin=l in order to reduce the delay and power consumption of the circuit. Here, the adder architectures like Regular Linear CSA, Modified Linear CSA and Regular CSA and Modified CSA are designed for 16-Bit word size only. This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Decoder is used. The synthesized results show that power consumption of Modified CSA is reduced in comparison to Regular Linear CSA but with small speed penalty. The calculated results conclude that Modified Carry Select Adder is better in terms of power consumption when compared with other adder architectures and can be used in different applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse Response etc.

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