International Journal of Electronic Networks, Devices and Fields.
ISSN 0974-2182 Volume 8, Number 1 (2016), pp. 19-25

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Design Approach For Implementation Of Bridge Between Mil-Std-1553 Bus And Gigabit Ethernet

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ABSTRACT

The objective of this research paper is to design a Bridge between the MIL-STD-1553B and Gigabit Ethernet (GE) Bus using an FPGA as a main device with protocol engines of both the buses and bridge the communication between both, without losing the advantages of both the buses.
The MIL-STD-1553B Bus is a widely used data bus in the avionics field. However, the contemporary applications such as high-speed digitized sensors, file transfers, processor clusters, and displays require much higher data rates than 1553's 1Mbps. The 1Mbps speed further goes down when the no. of sub-systems increased on the bus. The high speed Gigabit Ethernet (GE) Bus is becoming alternate choice to enhance the data transfer throughput from 1553 bus to Ethernet bus. The GE Bus has a bandwidth of 1000 Mbps, which is much faster than the 1553B Bus. In addition, its sophisticated protocol and multi-master capability can support distributed processing in advanced applications. Bridging both the buses i.e communication between both the buses using a bridge becoming essential.

Ethernet details

Ethernet is the dominant standard for commercial local area networking, with a vast ecosystem of operating systems and application software. Gigabit Ethernet derives from 10 and 100 Mb/ps Ethernet.

Gigabit Ethernet is being deployed on a significant number of military programs. Military/aerospace applications for Gigabit Ethernet includes Networking of Computers, data storage, sensors, displays, and bridging to IP-based wireless links and satellites for manned, unmanned air & ground vehicles, and soldiers

Ethernet, as standardized by IEEE 802.3, defines the two lowest layers of the OSI stack, the physical layer and the MAC (Media Access Control) portion of the data link layer. Ethernet frames consist of a start delimiter; 48-bit destination and source MAC addresses; a "length/type" field, which usually contains a value of 2048 ('08 00'h), designating IP protocol; a user payload of 46 to 1500 bytes; and a 4-byte frame check sequence.

A major ingredient in Ethernet's success is its simplicity, which enables low cost implementations for the lower layers' hardware, with higher-level functions typically mechanized by processor software. As the result of its success, Ethernet is used in offices, factories, personal computers, and medical applications. This enables Ethernet users to be able to leverage a vast COTS ecosystem of network interfaces and switches, cables, connectors, operating system stacks, application software, and test equipment.

Early Ethernet networks relied on the collision-oriented CSMA-CD (Carrier Sense Multiple Access – Collision Detect) protocol. While CSMA-CD provided adequate performance at low levels of overall network throughput, at higher throughput levels, the collision protocol was inefficient, due to increased access contention times. However, contemporary Ethernet is based on a switched fabric topology. In addition to eliminating collisions, switched networks enable all nodes to be able to send and receive simultaneously, and as a result provides great improvements not only in determinism, but also overall throughput and latency performance.

Ethernet Physical Layer

For Gigabit Ethernet, the most commonly used copper option is 1000BASE-T. This physical layer, which operates over four wire pairs, uses 4D-PAM5 (Pulse Amplitude Modulation) encoding to transmit in both directions simultaneously. Also 4D-PAM5 encoding transmits 8 bits of data simultaneously at any given time.

Separate symbols are transmitted simultaneously over each of the four wire pairs, with each symbol assuming one of 5 values: +2, +1, 0, -1, -2. There are therefore 625 possible symbol patterns, leaving 512 patterns to encode data, including extra bits for forward error correction; along with 113 that are used as control codes such as Idle (to maintain synchronization), start of packet, and end of packet. In this way, each wire pair transmits at 125 Mbaud, thereby transferring an aggregate data rate of 1Gb/s.

Advantages of 1000BASE-T derive from the fact that it operates over standard Cat 5 UTP (unshielded twisted pair) cable, which is widely and economically available. Further, since the symbol rate of 4D-PAM5 PAM is only 125 Mb, this enables operation over longer distances, up to 100 meters or more.

Ethernet Frames, Ethernet transmits variable length frames from 72 to 1518 bytes in length, each containing a header with the addresses of the source and destination stations and a trailer that contains error correction data. Higher-level protocols, such

as IP and IPX, fragment long messages into the frame size required by the Ethernet network being employed

Collision Detection Ethernet uses the CSMA/CD technology to broadcast each frame onto the physical medium (wire, fiber, etc.). All stations attached to the Ethernet are "listening," and the station with the matching destination address accepts the frame and checks for errors. Ethernet is a data link protocol (MAC layer protocol) and functions at layers 1 and 2 of the OSI model.

MIL-STD-1553 - Military Data Bus Details [A3]

The United States military standard (MIL-STD) 1553, "Aircraft Internal Time-Division Command / Response Multiplex Data Bus," was originally published in 1973. The primary use of this standard was to interconnect embedded, real-time mission critical subsystems within military equipment.

Although 1553 has been used for a number of years, it has several weaknesses that limit its use in future systems, including Speed of 1Mbps, High cost. As a result, next-generation systems are looking at GE as an alternative to 1553B or interface the legacy systems to high speed.

MIL-STD-1553 is a deterministic, reliable data bus, well suited for the interconnect of mission critical computing modules with real time sensors and controllers. Over the last 20 years it has become the most widely deployed communication backbone in military platforms, including aircraft, land based vehicles and naval platforms. Its' longevity is attributable to its positive

Perhaps the most compelling reason systems designers have chosen MIL-STD-1553 for mission critical systems is its command/response protocol which guarantees real-time determinism.

Despite these positive features, future adoption of '1553 in more demanding military systems is limited because the serial transmission rate of the bus is only 1 Mbit/sec. While this data transmission rate remains suitable for more rudimentary functions such as control of landing gear and munitions, it is too slow to serve the increased peer-to-peer communications needed by avionics and vetronics applications in support of data, audio and video information exchange.

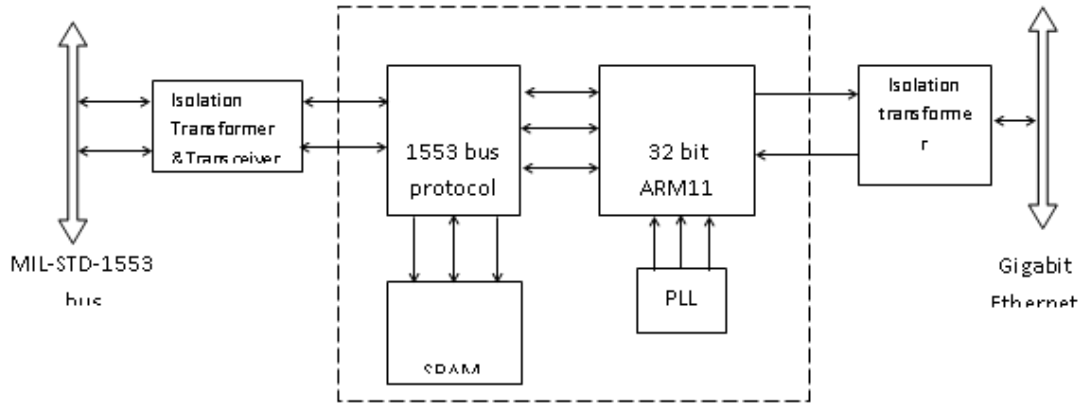
COMPARISION OF STANDARDS			
S.No	**Parameter**	**MIL-STD-1553B/**	**Gigabit Ethernet**
1	Transmission Rate	1Mbps	1Gbps
2	Media Access Control	Central Media Access Control	CSMA/CD
3	Range of Nodes	32	1024 (without bridges)
4	Environmental Specification	Military Avionics	Commercial
5	Topology	Linear Multi-drop Bus	Star
6	Data Formats	Up to 32 x (16bit + parity) messages	64-1518 bytes

7	Security of Service	Error detection at bit, word and message levels	32-bit CRC
8	Classes of Data	Single and multiple precision 16 bit words, single and multiple discrete, bytes etc.	Station to Station Multicast Broadcast & Burst Mode,1500 data bytes per frame
9	Physical Layers Supported	Shielded twisted pair, fiber optics possible	Various fiber optic and copper
10	Custodian	US Department of Defence (DoD) and UK Directorate of Standardization (Dstan)	IEEE 802 Local and Metropolitan Area Network Standards Committee

Design Approach:

It is proposed to implement the bridge using an FPGA as a main device and other supporting devices. A 1553 bus IP core will be used for implementing the 1553 protocol engine and ARM11 core for handling Ethernet protocol in a single FPGA.

Block diagram of MIL-STD-1553 to Gigabit Ethernet (GE) Bridge.



The basic functions of the bridge will be

1. Implementing the protocols of both buses.
2. Transfer of data and commends from one bus to another.
3. Matching the speed and message transfer without losing data.

The Implementing the protocols is achieved using IP Cores of both buses in a single FPGA.

The transfer of data & commands from one bus to another bus is achieved by implementing the algorithm in the ARM11 core. The speed matching without losing data is achieved by using shared memory which will be accessible to both the bus IP cores.

The hardware will be a single FPGA with 1553 Bus IP core & 32bit ARM11 IP core, with gigabit Ethernet interface, Shared memory of 128Kx16, PLL for generating

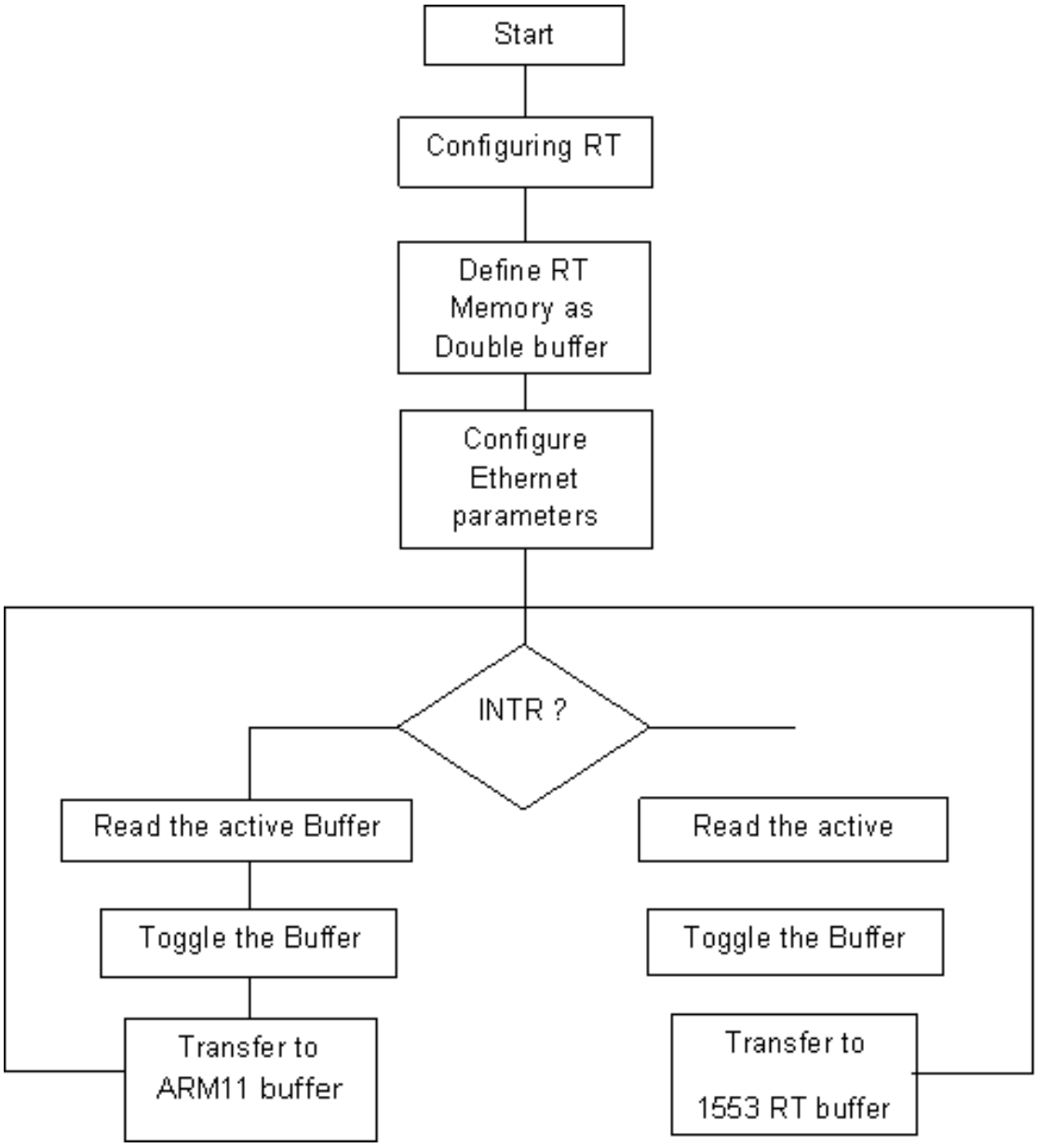
various peripheral clocks. The other devices are Isolation transformers on both buses and a JTAG interface for programming & debugging etc.
The matching of speeds of both buses is mainly by "Memory Management" i.e memory sharing will be a critical function to transfer data & commands from one bus to another bus. The data & commands are nothing but a set of messages and the messages transfer time will be critical parameter to manage the speeds.

Message transfer timings:
For a maximum time of single message (32 words) the time period will be 640µsec (1 word=20µsec). A 128K buffer is configured as part of 1553 RT. With a minimum inter message gap of 4µsec, the available memory can cater for 2048 messages.
i.e 128Kwords/2 and divided by 32words per message (i.e 64Kwords/32) will be 2048messages. OR in other words 2048x644nsec = 1.318 records for a 100% loading of 1553 bus, message transfer from Ethernet to 1553 can happen without any loss for 1.318sec whereas for messages transfer from 1553 bus to Ethernet, there is no restrictions for the duration of message transfer since output rate (1Gbps) is much more than the input rate (1Mbps). For the Ethernet to 1553Bus transfer, the congestion on 1553 bus can be reduced by configuring a bigger buffer on RT.

Memory management / Memory sharing:
The shared memory between 1553 bus and ARM11 controllers can be managed in one of the three ways as below:

i) Single Buffer: The available memory is divided into blocks of 32 words. Each block of 32 words is referred for a type of message, while this method occupies least of the Buffer before next message arrives failing which the older message gets over written.
ii) Double Buffer: Two buffers of identical size is maintained (A & B) while buffer A is being filled with a message, the buffer B is being read/cleared and vice versa. Thus one buffer period is the time available for clearing an already filled buffer. However effectively only half the memory is available for use. But loss of data can be prevented. Buffer time is to be selected based on the arrival rates of data packets from external source.
iii) Circular queue: Also called as circular FIFO, is the most efficient method for using the memory. The available memory is configured in such a fashion, on filling the available memory, further filling is done from the beginning of the memory. Thus time available to start cleaning the memory is equal to the time needed for complete filling of the memory.

All the three methods described above would work as long as the filling rate (writing rate) is less than the reading rate. For a given memory buffer size a defined mismatch in writing and reading rates can be handled to ensure loss free messages transfers.
For the current design it is propose to use double buffer shared memory, the operational flow chart is given below:



Conclusions:

The design can be further Optimized by retaining only the "Ethernet protocol engine" instead using the complete ARM11 core. This offers improvement in the performance and reduction in the FPGA logic usage.

Improvement in the hardware by including the Power Over Ethernet (POE) feature, so that the device can work with power derived from network port itself.

Since 1553 bus protocol is primarily a command/response based, there is a definite delay (response delay & inter message delay) involved. Theoretically a 1553 bus controller can transmit upto 20,000 messages per sec. The user application on Ethernet may need to send a reply packet for every packet received from 1553 bus,

this means for a packet rate of 20,000/sec on 1553 bus may results in 40,000/sec packets per sec on Ethernet bus. Most of the computers / LAN switches/Routers cannot process more than 50,000 packets per sec. This is due to protocol overheads and path delays, which may overload devices on the network. Hence the system designer has to address this critical issues while using the 1553 & Ethernet Bridge.

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