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Low-Power and Fast Adders Using New XOR and XNOR Gates

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Abstract

In this paper, novel circuits for XOR/XNOR and simultaneous XOR–XNOR functions are proposed. The proposed circuits are highly optimized in terms of the power consumption and delay, which are due to low output capacitance and low short-circuit power dissipation. We also propose six new hybrid 1-bit full-adder (FA) circuits and Ripple Carry Adder based on the novel full-swing XOR–XNOR or XOR/XNOR gates. Each of the proposed circuits has its own merits in terms of speed, power consumption, powerdelay product (PDP), driving ability, and so on. To investigate the performance of the proposed designs, extensive Mentorgraohics simulations are performed. The simulation results, based on the 130-nm CMOS process technology model, indicate that the proposed designs have superior speed and power against other Adder designs. A new transistor sizing method is presented to optimize the PDP of the circuits. In the proposed method, the numerical computation particle swarm optimization algorithm is used to achieve the desired value for optimum PDP with fewer iterations. The proposed circuits are investigated in terms of variations of the supply and threshold voltages, output capacitance, input noise immunity, and the size of transistors.

Keywords: Full adder (FA), Ripple Carry Adder, transistor sizing method, XOR–XNOR.

I. INTRODUCTION

Now-a-days, electronic systems are an inseparable part of everyday life. Digital circuits, like microprocessors, digital communication devices, and digital signal processors, comprise a large part of electronic systems. As the scale of integration increases, the usability of circuits is restricted by the augmenting amounts of power and area consumption. Therefore, with the growing popularity and demand for the battery-operated portable devices such as mobile phones, tablets, and laptops, the designers try to reduce power consumption and area of such systems while preserving their speed.

Optimizing the *W/L* ratio of transistors is one approach to decrease the power-delay product(PDP) of the circuit while preventing the problems resulted from reducing the supply voltage.

The efficiency of many digital applications relates to the performance of the arithmetic circuits, such as adders, multipliers, and dividers. Due to the fundamental role of addition in all the arithmetic operations, many efforts have been made to explore efficient adder structures, e.g., carry select, carry skip, conditional sum, and carry look-ahead adders. Full adder (FA) as the fundamental block of these structures is at the center of attention.

Based on the output voltage level, FA circuits can be divided into full-swing and nonfull-swing categories. Full Swing comprises of Standard CMOS, complementary pass-transistor logic (CPL), transmission gate (TG), transmission function, 14T (14 transistors), 16T, and hybrid pass logic with static CMOS output drive full adder. Nonfull-swing category comprises of 10T, 9T , and 8T.

In this paper, we evaluate several circuits for the XOR or XNOR (XOR/XNOR) and simultaneous XOR and XNOR (XOR–XNOR) gates and offer new circuits for each of them. Also, we try to remove the problems present in the investigated circuits. Afterward, with these new XOR/XNOR and XOR–XNOR circuits, we propose six new FA structures and a 4 bit ripple carry adder.

II. REVIEW OF XOR AND XNOR GATES

A. XOR/XNOR Circuits

XOR or Ex-OR and XNOR gates are special type of gates used in the adders and subtractor. These has n input (n>=2) and one output. To build the adders many logic gates can be used but the XOR/XNOR gates plays a efficient role. To design the adders we proposed XOR/XNOR circuits and simultaneous XOR-XNOR circuits. The XOR/XNOR gate is the major consumer of power in the Adders. Therefore, the power consumption of the Adders cell can be reduced by optimum designing of the XOR/XNOR gate. The XOR/XNOR gate has also many applications in digital circuits design.

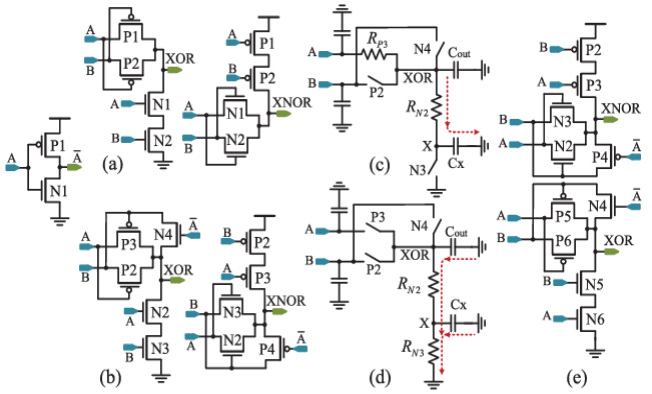

Fig. 1. (a) Nonfull-swing XOR/XNOR gate [24]. (b) Proposed full-swing XOR/XNOR gate. (c) *RC* model of proposed XOR for *AB* = 10. (d) *RC* model of proposed XOR for *AB* = 11. (e) Proposed XOR–XNOR gate.

The circuit design to implement the proposed circuit design of XOR-XNOR circuits is shown in Fig.1. The nonfull-swing XOR/XNOR circuit of Fig. 1(a) is efficient in terms of the power and delay. Furthermore, this structure has an output voltage drop problem for only one input logical value. To solve this problem and provide an optimum structure for the XOR/XNOR gate, we propose the circuit shown in Fig. 1(b). For all possible input combinations, the output of this structure is full swing. The proposed XOR/XNOR gate does not have NOT gates on the critical path of the circuit. Thus, it will have the lower delay and good driving capability.

The input A and B capacitances of the XOR circuit shown in Fig. 1(b) are not symmetric, because one of these two should be connected to the input of NOT gates and another should be connected to the diffusion of nMOS transistor. Furthermore, the input capacitances of transistors N2 and N3 are not equal in the optimal situation (minimum PDP). Also, the order of input connections to transistors N2 and N3 will not affect the function of the circuit. Thus, it is better to connect the input A, which is also connected to the NOT gates, to the transistor with smaller input capacitance. By doing this, the input capacitances are more symmetrical, and thus, the delay and power consumption of the circuit will be reduced. To clarify which transistor (N2 or N3) has larger input capacitance, let us consider the condition that the inputs change from AB = 00 to AB = 10. In this condition, as the RC model of XOR is shown in Fig. 1(c) and (d), the transistor N2 is driving only the capacitance of node X from GND to VDD − Vthn [Fig. 1(c)], so it will not require lower RN2. But, when the inputs change from

$$AB = 10 \text{ to } AB = 11.$$

Fig. 1(e) shows the proposed structure of the simultaneous XOR–XNOR gate consisting of 12 transistors. This structure is obtained by combining the two proposed XOR and XNOR circuits of Fig. 1(b). If the inputs of this circuit are connected as mentioned in Section II-A, the input A and B capacitances are not equal (the inputs A and B are connected to the same transistor count). Thus, to equal the input of capacitances, they are connected to the circuit, as shown in Fig. 1(e). In this case, the input capacitances are approximately equal and the power and delay are optimized. This structure does not have any NOT gates on the critical path and its output capacitance is very small. For this reason, it is very high speed and consumes low power. The delay of XOR and XNOR outputs of this circuit is almost identical, which reduces the glitch in the next stage. Other advantages of this circuit are good driving capability, full-swing output, as well as robustness against transistor sizing and supply voltage scaling.

The advantages of the XOR/XNOR circuits are full-swing output, good driving capability, smaller number of interconnecting wires, and straightforward circuit. These are designed for minimum power consumption.

TABLE 1: *SIMULATION RESULTS (POWER DISSIPATION, DELAY) FOR XOR/XNOR AND SIMULTANEOUS XOR-XNOR IN 130NM TECHNLOGY WITH 1.8VPOWER SUPPL AT 1GHz FREQUENCY*

XOR and XNOR Circuits	Power Dissipation	Delay
Fig.1a (XOR)	4.8432nW	49.994ns
(XNOR)	15.2477nW	49.825ns
Fig.1b (XOR)	17.2285nW	228.32ps
(XNOR)	1.6294nW	49.998ns
Fig.1e (XOR- XNOR)	17.2287nW	49.998ns

III. HYBRID FULL ADDER

We proposed six new FA circuits for various applications which have been shown in Fig. 2. These new FAs have are designed by using the proposed XOR/XNOR been employed with hybrid style and all of them or XOR–XNOR circuit. The well- known four-transistor 2-1-MUX structure [Fig. 3(a)] is used to implement the proposed hybrid FA cells. This 2-1-MUX is created with TG logic style that has no static and short-circuit power dissipation.

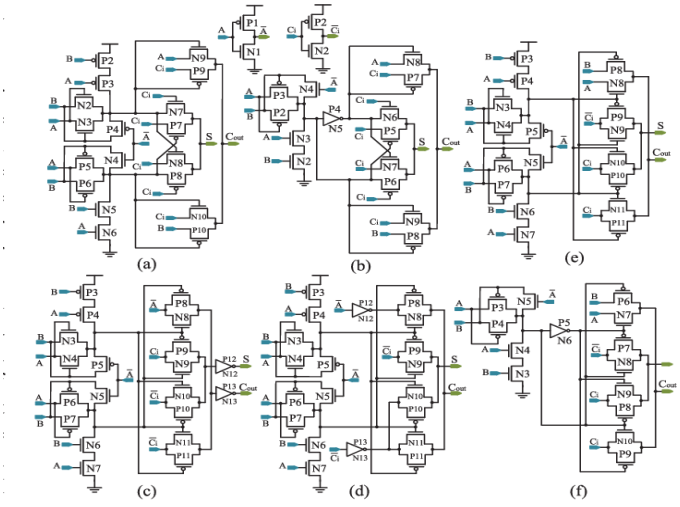

Fig. 2. Proposed six new hybrid FA circuits. (a) HFA-20T. (b) HFA-17T. (c) HFA-B-26T. (d) HFA-NB-26T. (e) HFA-22T. (f) HFA-19T.

Fig. 2(a) shows the circuit of first proposed hybrid FA (HFA-20T) which is made by two 2-to-1 MUX gates and the XOR–XNOR gate of Fig. 1(e). The circuit of HFA-20T has not high power consumption NOT gates on critical path and consists of 20 transistors. The advantages of this structure are full-swing output, low power dissipation and very high speed, robustness against supply voltage scaling, and transistor sizing.

The only problem of HFA-20T is reduction of the output driving capability when it is used in the chain structure applications, such as ripple carry adder. Of course, this problem exists in the circuits that use the transmission function theory in their implementation without buffering output.

One way to reduce the power consumption of the FA structures is to use a XOR/XNOR gate and a NOT gates to generate the other XOR or XNOR signal. The proposed hybrid FA cell (HFA-17T) shown in Fig. 2(b) is designed by using the XOR gate of Fig. 2(b). This structure is made by 17 transistors that has three transistors less than the HFA-20T. The delay of HFA-17T is higher than that of HFA-20T due to the addition of NOT gates on the critical path of the HFA-17T (for making the XNOR signal from the XOR signal). It may be expected that the power consumption of HFA-17T is less than that of HFA-20T due to the reduction in the number of transistors. But the NOT gate on the critical path of the circuit increases the short circuit power. So there is no HFA significant reduction in total power dissipation of the 17T. Also, the NOT gate will slightly improve the output driving capability of the circuit.

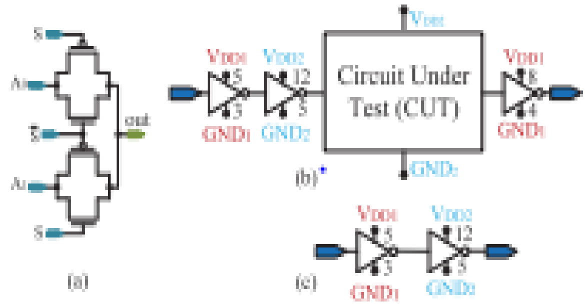

Fig. 3. (a) 2-1-MUX. (b) and (c) Simulation test bench to carry out the circuit parameters.

As mentioned earlier, using the buffer on the output of a circuit is almost mandatory, especially in applications that the output capacitance of each stage is high. In practice, the driving capability of VLSI circuits is degraded due to the creation of the parasitic capacitors and resistors during the fabrication, as well as increasing the threshold voltage of transistors over the time, but the output buffer improves this situation. Fig. 2(c) presents the third proposed hybrid FA with buffers on the Sum and Cout outputs (HFA-B-26T), and it is made with 26 transistors. There are XOR–XNOR gate, one 2-1-MUX gate, and NOT gates on the critical path of HFA-B-26T. The output NOT gates are used to prevent the driving output nodes by the inputs of the circuit and also reduce the resistance from the output node of the circuit to the sources (VDD and GND). The power consumption and delay of HFA-B-26T are more than that of HFA-20T and HFA-17T FAs.

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The circuits of HFA-20T and HFA-17T have been designed so that the less number of transistors has been used. To produce the output Sum signal, the XOR, XNOR, and C signals are only used so no additional NOT gates needs to generate the C signal, whereas if the C signal is also used to produce the Sum output, then XOR and XNOR signals will not drive the Sum output through the TG multiplexer, but only they will be connected to the data select lines of 2-1-MUX. So the capacitance of XOR and XNOR nodes become smaller, and the delay of the circuit will be improved. The circuits of Fig. 1(e) and (f) (named HFA-22T and HFA-19T, respectively) have been created by applying the above idea to HFA-20T and HFA-17T, respectively. It is expected that the power consumption and delay of the HFA-22T and HFA-19T FA circuits are less than that of HFA-20T and HFA-17T, respectively (despite having two more transistors), due to the less capacitance of XOR and XNOR nodes. Also, by adding the C signal, the driving capability of HFA-22T and HFA-19T will be better than that of HFA-20T and HFA-17T, respectively.

TABLE 2: *SIMULATION RESULTS (POWER DISSIPATION AND DELAY) FOR HYBRID FULL ADDER IN 130nm TECHNOLOGY WITH 1.8v POWER SUPPLY AT 1GHz FREQUENY*

Fig Name	Transistor Count	Power Dissipation	Delay
2a	20T	10.8531nW	194.03ps
2b	17T	18.1092nW	125.31ps
2c	26T	46.7421nW	196.72ps
2d	26T	41.3388nW	11.489ps
2e	22T	39.7970nW	16.915ps
2f	19T	89.7630nW	99.963fs

IV. RIPPLE CARRY ADDER

.Multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. A ripple carry adder is a logic circuit in which the carry-out of each full adder is the carry in of the succeeding next most significant full adder. It is called a ripple carry adder because each carry bit gets rippled into the next stage. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs.Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the corresponding output. Consider a NOT gate, When the input is “0” the output will be “1” and vice versa. The time taken for the NOT gate’s output to become “0” after the application of logic “1” to the NOT gate’s input is the propagation delay here. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurance of the carry out (Cout) signal. Circuit diagram of a 4-bit ripple carry adder is shown below.

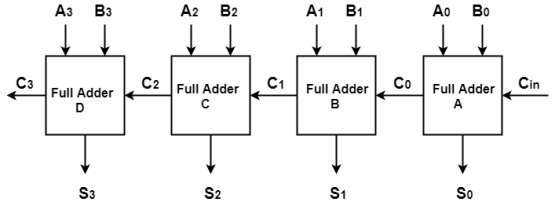

Fig.4: 4-bit ripple carry adder

Sum out S0 and carry out Cout of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propogation delays of all full adder circuits inside it.

V. PROPOSED RIPPLE CARRY ADDER

The proposed ripple carry adder is designed by using the hybrid full adder circuits [fig.2].We had designed ripple carry adder basing on the parameters of power consumption and delay. Table 2 predicts the values of various hybrid full adder circuit designs. We had taken the two circuit designs of Fig. 2 in terms of power dissipation and delay. Designing the ripple carry adder with Fig. 2a can reduce the power dissipation. And designing the ripple carry adder with Fig. 2f can reduce the delay.

The schematic circuit diagrams of ripple carry adder using Fig. 2a and 2f are shown below.

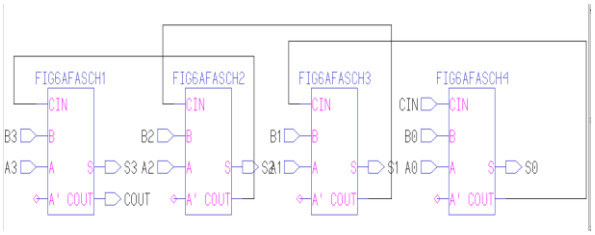

Fig.5a

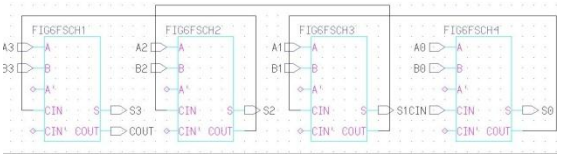

Fig. 5b

Fig.5: Schematic circuit diagrams for ripple adder. (a) ripple carry adder using Fig.2a (b).ripple carry adder using Fig. **2f.**

VI. SIMULATION RESULTS

All the circuits have been simulated using Mentorgraphics in the 130-nm CMOS process technology, and were supplied with 1.8 V as well as the maximum frequency for the inputs was 1 GHz.

THe simulated waveforms of ripple carry adder using hybrid full adder circuit is shown below.

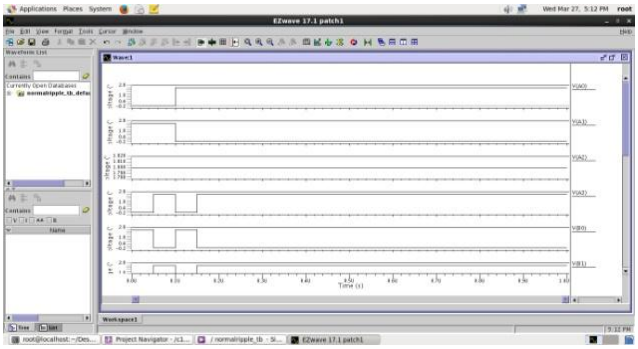

Fig.6a: Simulated waveform of normal ripple carry adder circuit input sequence 1

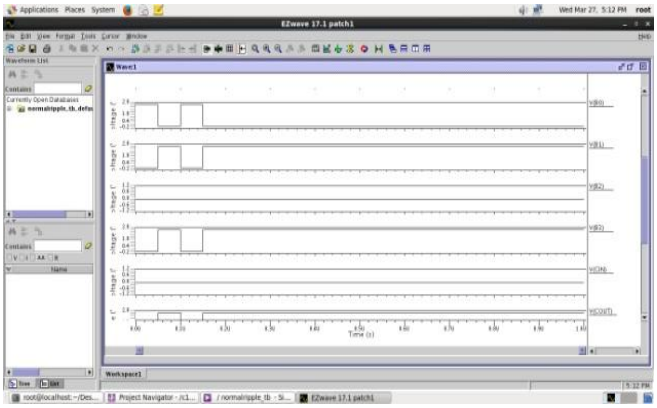

Fig. 6b: Simulated waveform of normal ripple carry adder circuit input sequence 2

Table 3 shows the simultaneous values for various adder circuits.

TABLE 3: *SIMULATION RESULTS (POWER DISSIPATION, DELAY) FOR ADDER CIRCUITS IN 130NM TECHNOLOGY WITH 1.8VPOWER SUPPL AT 1GHz FREQUENCY*

Full Adder	Power dissipation	Delay
Normal Full Adder	71.46nW	49.719ns
Normal Ripple Carry Adder	222.027nW	280.08ns
Ripple Carry Adder for Fig.5.1(a)	111.75nW	49.855ns
Ripple Carry Adder for Fig.5.1(b)	77.09nW	112.23ps

VII. CONCLUSION

In this paper by using the existed XOR/XNOR circuits and simultaneous XOR-XNOR circuits we designed the hybrid full adder. And also we designed ripple carry adder using hybrid full adder.

Finally, by using the proposed XOR and XOR–XNOR gates, we designed six new FA cells for various applications. The designed circuits has very good speed, accuracy, and convergence. On comparing hybrid full adder with ripple carry adder the power dissipation and delay are reduced. After simulating the ripple carry adder using different circuits of hybrid full adder , the results demonstrated that the proposed circuits have a very good performance in all simulated conditions.

Simulation results show that the proposed adder circuits saves delay upto 20%, compared with its best counterpart. Also, this circuits has better speed and energy at 1.8 v supply voltage when is compared with other adder circuit designs.

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